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Asymmetric DC Source Multilevel Inverter

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Abstract: An asymmetrical multilevel inverter with harmonic profile improvement and lower voltage stress is presented in this paper. The multilevel inverter is a power electronic circuit that produces sinusoidal output voltage waveform from several levels of dc input voltages, which reduces Electromagnetic Compatibility (EMC) and Total Harmonic Distortion (THD). Four modules are connected in series together with its dc source is configured in asymmetrical configuration to produce 31 output voltage levels. Asymmetrical Multilevel Inverter offers more advantages compared to the conventional multilevel (symmetrical Multilevel Inverter) and the two-level inverters itself. This work focuses on the cascaded multilevel inverter with it dc source configured in asymmetrical configuration. The proposed topology will be developed and simulated in MATLAB/Simulink software package. For comparison purposes, normal two-level inverter also developed. The results such as the output voltage, voltage stress across the power switch, the THD content have been analyzed and discussed.

Keywords: asymmetrical multilevel voltage source inverter; harmonic improvement; normal two-level voltage source inverter; power switch voltage stress.

1. INTRODUCTION

Multilevel Voltage Source Inverter (MLVSI) is a device or circuit that convert DC source to AC load in term of voltage that produce higher sinusoidal output voltage level compared to normal inverter [1,2]. MLVSI is a power electronic system that produces desired AC output voltage and frequency from DC input voltage [1]. MLVSI is an alternative to the normal two levels MVSI in high power application. There are various multilevel voltage source inverter topologies were reported. Figure.1 shown the overall summary of reported MLVSI. Cascaded Multilevel Inverter (CMI) have been recognized as the most popular topology among other multilevel inverter topology. CMI offer several advantages compared to normal inverter such as lower Electromagnetic Compatibility, lower Harmonic Profile, avoid unbalanced capacitor voltage problem and low switching losses. The normal two-level inverter is switching at high frequency which will make the location of harmonics cluster is very far from fundamental at the expend of very high frequency. However, as the CMI topology popularity increased among researcher, this lead to the development of asymmetrical multilevel voltage source inverter.

Asymmetrical Multilevel Voltage Source Inverter (AMLVSI) is proposed due to the ability to generates larger number of output levels. With larger number of output levels, the THD will be reduce that AMLVSI doesn't require any filter if the THD is less than 5%. AMLVSI is built from a series-connected full-bridge inverter module with its dc source is in binary or trinary configuration. Furthermore, AMLVSI binary DC configuration can reduces the voltage stress on the switching device compared to normal two-level voltage source inverter which the higher the output voltage needed the higher the voltage stress on the power switch that will result in switching losses and higher acoustic noise [1,3]. For the AMLVSI, the voltage stress of the power switch will be shared among other series-connected inverter module which will reduces the switching losses and acoustic noise at higher output voltage needed.

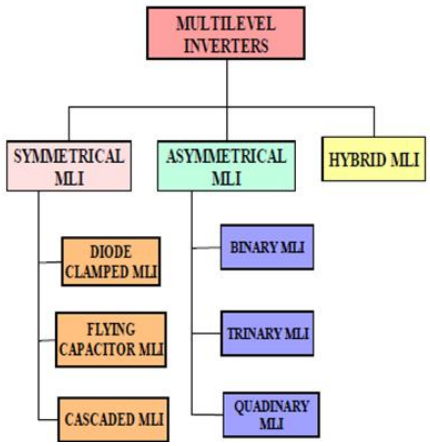

Figure 1. Overall Summary of reported Multilevel Voltage Source Inverter [4]

2. THE PROPOSED ASYMMETRIC MULTILEVEL VOLTAGE SOURCE INVERTER

Figure. 2 shows N modules of the proposed Asymmetrical Multilevel Voltage Source Inverter (MLVSI). The MLVSI is constructed of a series-connected full bridge normal inverter module with the dc voltage source in geometric progression (binary) [5].

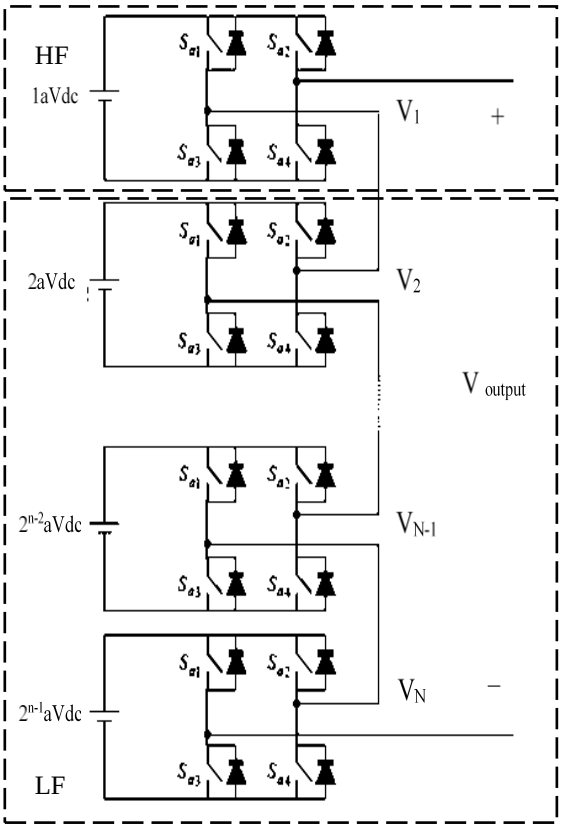

Figure 2. N modules of the proposed Asymmetrical Multilevel Voltage Source Inverter

techniques/scheme for the multilevel need to be determined. Based on the review the switching pattern or modulation scheme have been chosen. Then, the circuit and modulation scheme have been implemented in the MATLAB/Simulink.

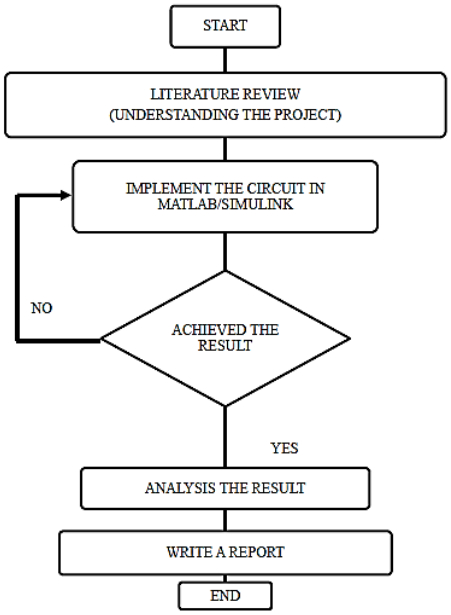

Figure 3. Flow Chart for completing the Proposed Topology

2.1 The dc source configuration of an Asymmetrical Multilevel Voltage Source Inverter

For the N number of modules was constructed in a series-connected, the configured asymmetrical dc source (binary) is given by (1):

$$V_{dc}=2^{n-1}a\ V \quad (1)$$

Where n: The N number of module cascaded in series-connected inverter

2.2 The number of voltage level produced in Asymmetrical Multilevel Voltage Source Inverter

For the N number of modules was constructed in a series-connected with configured asymmetrical dc source (binary), the M number of voltage level produced is given by (2):

$$M=2^{N+1}-1 \text{ levels} \quad (2)$$

Where N: the number of module cascaded in series-connected inverter

2.3 The Methodology to Obtain the Output of Asymmetrical Multilevel Voltage Source Inverter

To obtain the desired output of Asymmetrical Multilevel Voltage Source Inverter, the following flow chart (Figure 3.) need to be followed. To begin with the project, the overall concept of Multilevel Inverter need to be understand by collecting and reading all the sources that can be used to obtain desired output. The modulation

3. THE MODULATION SCHEME

There several modulation scheme have been presented by researcher and also the old PWM technique which is multi-career PWM scheme. But for the multi-career scheme, qualitatively look all of the inverter or switching will work at very high frequency which will result in high THD and also EMC. Therefore, a modulation strategy presented in Figure 4. and Figure 5. will be used for the Asymmetrical Multilevel Voltage Source Inverter.

The output waveform is a combination between stepped voltage waveform synthesized in low frequency (LF) inverter and a high frequency pulse width modulation (HFPWM) technique waveform produced in high frequency (HF) inverter Figure 4 and Figure 5 is the block diagram and control circuit for the modulation scheme implemented to produce command/switching signal for the inverter modules. The reference signal (sinusoidal waveform with frequency fs and amplitude As) of the Asymmetrical multilevel inverter was used as a command/switching signal of the module with highest dc voltage source which is for the 1st comparator block. The reference signal is compare to inverter DC voltage factor, which is if the command signal is greater than voltage factor, the output must be equal to the voltage factor, or else the output will be set to zero.

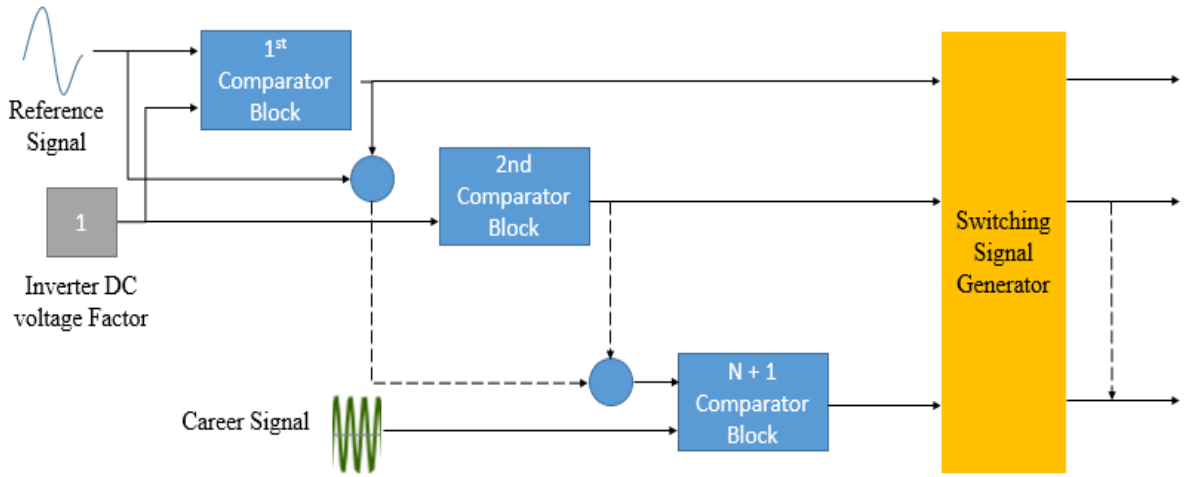

Figure 4. Block diagram of Switching/Gating Signal Generator

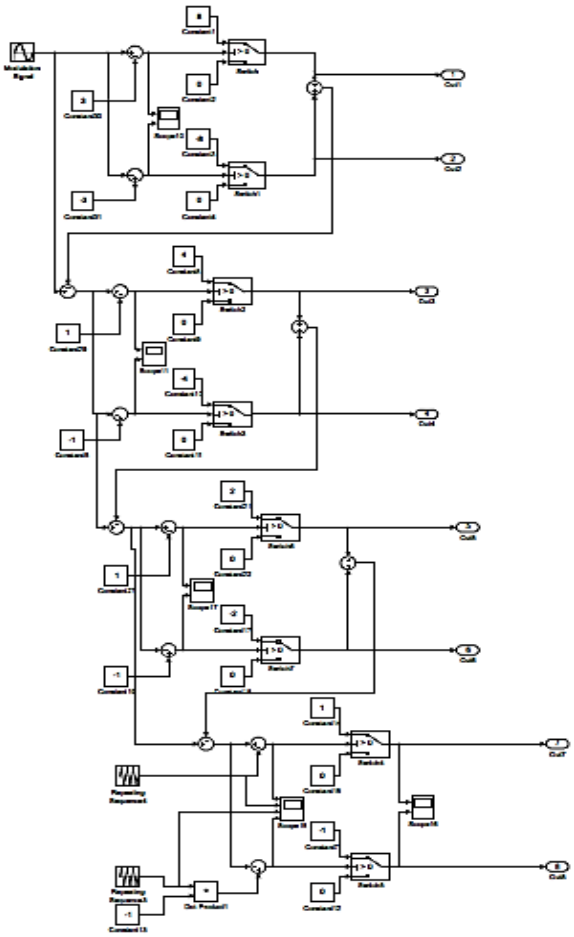

Figure 5. Control Circuit of Switching/Gating Signal Generator

The command signal of the 2nd comparator is the difference between the 1st comparator block command signal and the output signal/waveform of the 1st comparator. This switching/command signal then compared again with other inverter DC voltage factor and the output is synthesized from the difference/comparison of those two signals. This process will be repeated until it reach the (N+1)th comparator block. The command signal of the (N+1)th comparator block is compared with the career signal (repeated triangular waveform with frequency, fc), which resulting in HFPWM waveform.

The modulation index of the Control circuit can be determined by (3):

$$modulation\ index, Mi = \frac{fc}{fs} \quad (3)$$

And the modulation ration for the proposed modulation scheme can be given as (4):

$$modulation\ ratio, Mr = \frac{As}{N-1} \quad (4)$$

Finally, all of the output of the comparison block are fed forward to the switching signal generator block which is the addition/subtraction process. Here (Figure 6), the signal are manipulated to produce switching signal for each modules of Asymmetrical multilevel voltage source inverter.

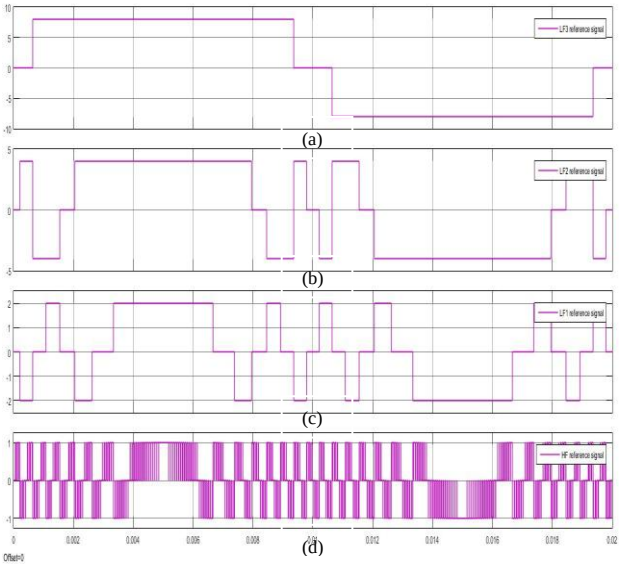

Figure 6. Reference Signal for 31 level with Asymmetrical dc source configuration (a) Reference Signal LF3 (b) Reference Signal LF2 (c) Reference Signal LF1 (d) Reference Signal HF

4. Simulation Result

Figure. 7 and 8 present output voltage waveform for the proposed topology with the dc source is configured in asymmetrical (binary) and the normal two-level inverter with their harmonic spectrum respectively. For

asymmetrical (binary) configuration, as can be seen from the figures, all of the level of the output waveform are high frequency modulated. But for the normal two-level inverter, only two level will be modulated at high frequency and with presence of low order in it waveform harmonic spectrum. As a result, Asymmetrical (binary) dc source obtained a better harmonic profile without low-order harmonic in it respective harmonics waveform spectrums.

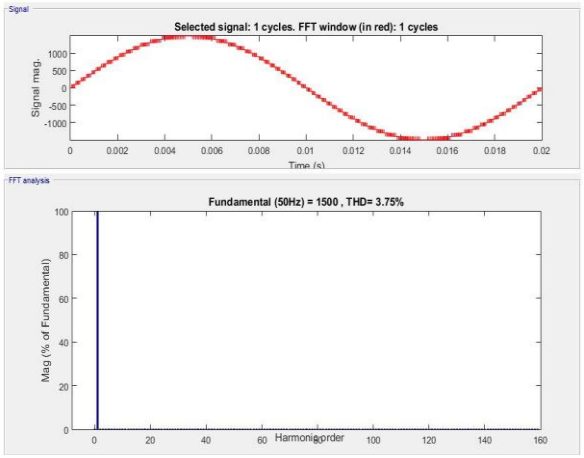

Figure 7. output voltage waveform for the dc source configured in asymmetrical (binary) and its harmonic

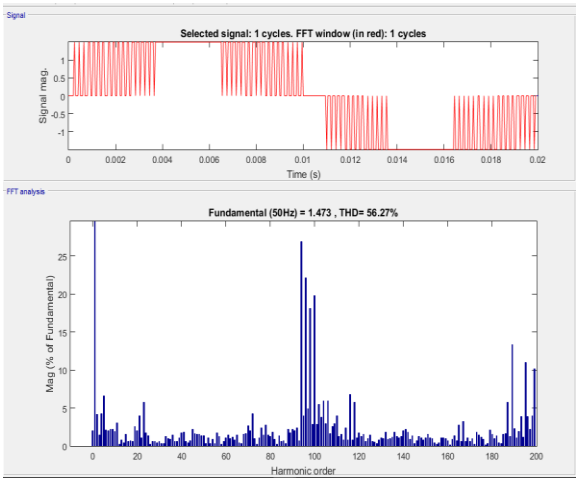

Figure 8. output voltage waveform for the two-level inverter and its harmonic spectrum

Furthermore, Table 1 shows the voltage stress that accumulated for power switch to block the voltage of the two-level inverter and AMVSI. It shows that to obtain a 1500 output voltage the AMVSI power switch is sharing their stress with the other series connected inverter module while for two-level inverter need to block all the voltage itself. Therefore, due to the higher voltage stress will result in switching losses.

Finally, it can be concluded that with the proposed topology, better harmonics profile can be obtained. Total harmonic Distortion for the proposed topology is below 5.00% which is 3.75% while with normal two-level inverter yields 56.27% THD. The voltage stress for the power switch of Normal two-level inverter is higher that the proposed topology.

Table 1. Voltage Stress for Asymmetrical Voltage Source MLI and Normal two-level inverter

Asymmetrical dc source configuration	**Voltage Stress (Volt)**
Module LF1 power switch	100
Module LF2 power switch	200
Module LF3 power switch	400
Module HF power switch	50
Normal 2 level inverter	
H-Bridge Power Switch	750

5. CONCLUSION

This paper present the Asymmetrical Multilevel Inverter topology for harmonic profile improvement, voltage stress reduction and reduction of Electromagmetic Compatibility. It is agreed that the proposed Asymmetrical Multilevel Inverter can present more output levels, smallest Total Harmonic Distortion (THD) percentage and the voltage stress for each module is lower than the normal two-level inverter. As a result for the proposed topology, the output voltage waveform presents better harmonic profile, the voltage stress is lower and higher level of output voltage was obtained.

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