International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 8, No. 1, March 2017, pp. 109~116
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v8i1.pp109-116

Seven Levels Symmetric H-bridge Multilevel Inverter with Less Number of Switching Devices

Megat Azahari Chulan[1], Mohd Junaidi Abdul Aziz[2], Abdul Halim Mohammed Yatim[3], Mohd Zaki Daud[4]
[1] Faculty of Electrical and Electronics Engineering, Universiti Tun Hussein Onn Malaysia (UTHM), Malaysia
[2,3,4] Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM), Malaysia

Article Info

Article history:

Received Sep 28, 2016
Revised Dec 04, 2016
Accepted Dec 14, 2016

Keyword:

APOD-PWM
Cascaded multilevel inverter
H-Bridge
SPWM
Total harmonic distortion

ABSTRACT

This paper proposes a new topology of a cascaded multilevel inverter that utilises less number of switches than the conventional topology. The proposed topology maintains the performance of conventional 7-levels output multilevel inverter while reducing the loss of power, installation area, converter size as well as development cost. The circuit development consists of six switches and one diode. With less number of switching devices in the circuit, there will be a reduction in the gate driver circuits and also in effect fewer switches required for specific intervals of time. Simulation works have been conducted to validate the proposed MLI topology. It is envisaged that the proposed topology can be applied for the system that requires high efficiency and a low electromagnetic interference.

Corresponding Author:

Megat Azahari Chulan,
Faculty of Electrical and Electronics Engineering,
Universiti Tun Hussein Onn Malaysia (UTHM),
Malaysia.
Email: megat@uthm.edu.my

1. INTRODUCTION

Multilevel inverters (MLI) are popular converter topologies due to the operational abilities of a high-voltage, high efficiency and a low electromagnetic interference [1]. Despite the many researches carried out in this configuration, MLI still evolves. Multilevel inverter is used to maintain a low harmonics in the operating system and reducing the switching stress and thus improving the converter efficiency. Normally, in order to achieve that objective, the number of the voltage source and switching operation are increased. However, the loss of power and the cost of converter development would significantly increase. Thus, there is a need for the current MLI topologies evolution to concentrate on those issues. Reducing the number of components, applying advance control strategies and switching algorithm to ensure the converter's output quality can be increased are some of the modifications made to tackle the issues.

Although THD performance is enhanced, the complexity in its control circuit due to the high number of semiconductor switches introduces high switching and conduction losses. Considering these issues, several new and improved multilevel inverter topologies have been introduced as discussed in [2],[3]. The authors have suggested a design methodology to synthesize multilevel inverter output with a large number of levels with good spectral performance but with a reduced number of switches. Various topologies of multilevel inverter have also been proposed focusing on the reduced number of switches and components and at the same time maintaining the quality of the converter output voltage as well as cost of installation reduction.

Conventional 7 levels Cascaded Multilevel Inverters (CMLI) requires 12 switches and three DC sources. In fact, early research in [5] has managed to reduce the number of switches to 9 with the desired

output voltage for seven levels. In addition the harmonics content is still remained low while reducing the cost of installation and at the same the H-bridge concept is still retained. Then, other researchers only considered 3 DC sources and it needs only 5 switches to be controlled in the high frequency side in producing of 7 levels output voltage. After that, other works introduced 3 DC sources with 8 switches topology [4]. Then, the number of switches is further reduced by 4 compared to the conventional CMLI [5]. In this topology, a modulation technique of POD-SPWM is utilized in order to produces the seven levels output voltage. The implementation of the various carrier PWM techniques is possible for multilevel inverters. Other than the POD-SPWM, there are two more Alternative Carrier Disposition SPWM strategies commonly used in switching technique that applied in control strategy. These are (i) Phase Disposition (PD), where all carriers are in phase [6] and (ii) Alternate Phase Opposition Disposition (APOD), where each carrier is phase shifted by π from its adjacent carrier. In addition, abundant modulation techniques and control paradigm have been developed for various levels of pulse width modulation converters other than sinus (SPWM). They are selected harmonic elimination (SHE-PWM), Space vector modulation (SVM) and others [7],[8].

The following topology as in [9] has successfully produced 7 levels MLI configured using 4 sources dc supply and only 6 switches. However, as this configuration does not utilize the concept of H-Bridge, switching control techniques are still complicated. Additionally, this approach uses more number of DC sources causing ineffective development cost. The latest topology uses only 6 switches to produce 7 level output [10]. This topology has successfully reduced the cost up to 50% from the conventional topology but efficiency can be improved because the circuit consist two diodes.

Nevertheless, there are some weaknesses in the MLI. Among the most obvious is the high numbers of power semiconductor switches are required. Each switch needs a gate driver circuit, thus increasing the complexity and size of the entire circuit. Requirement a lot of gate drive circuit leads to great expense. Therefore, in practical applications, a reduction in the number of switches used is important. This paper presents a new topology of a cascaded multilevel inverter that has fewer semiconductor switches and gate driver circuits with higher number of steps in the output. The circuit development consists of six switches and one diode. However, the operation mode of the proposed topology has lower conduction and switching losses which consequently improving the converter's efficiency.

2. CONVENTIONAL CASCADED MULTILEVEL INVERTER TOPOLOGY

Figure 1 shows the circuit structure of a conventional cascaded H-bridge multilevel inverter. Typically this conventional cascaded H-Bridge structure consists of 3 series bridge-circuits. In addition, each H-bridge circuit has their independent DC source and from this arrangement it will generates three different voltage levels, i.e., +VDC voltage, 0 and –VDC voltage, respectively. Thus, this circuit structure requires 12 switches in order to produce seven levels output voltage [11]. Nevertheless, modulation technique need to be designed intensively, therefore the output voltage generated close to sinusoidal waveform. The voltage output is given by equation (1)

$$V_0 = V_{01} + V_{02} + V_n \quad (1)$$

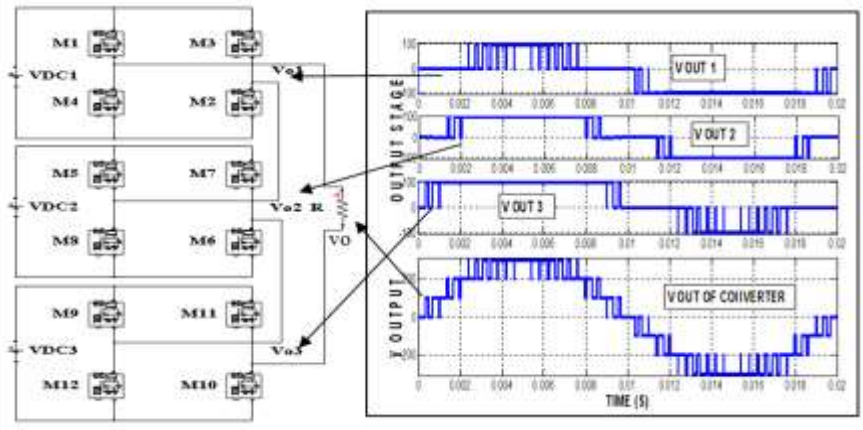


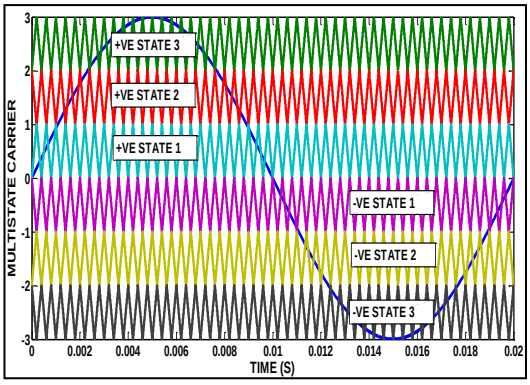
Figure 1. Construction of seven levels Conventional Cascaded MLI and output waveform of converter

As stated previously, the increment of output voltage levels require the additional semiconductor switches. As a result, the control of semiconductor switches becomes complex. The cost and converter size also will be increased. Generally, the modulation index change is obtained by comparing the amplitude of reference signal (sinusoidal) and the amplitude of multi-carrier–triangle signal [12]. The expression of modulation index, Ma as following,

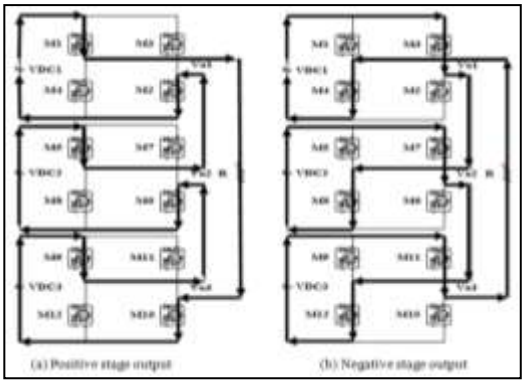
$$Ma = \frac{A_r}{A_c} \quad (2)$$

where , A_r *is* the amplitude of reference signals and A_c is the peak to peak value of the carrier signal.

In producing of seven levels output voltage, six saw-tooth carrier signals and a sinusoidal reference signal for a modulator are required as shown in Figure 2(a). Thus, six states are considered and the states are divided of two sections, i.e., (i) positive section, and (ii) negative section. The positive section consist of 3 states, i.e, +ve-state-1 is considered when the modulator signal is within the lowest carrier while the +ve-state-2 is considered when it is within the middle carrier. Finally, the +ve-state-3 is when it is within the highest carrier. It is similar states in negative section. In each state, certain switching patterns are adopted to cover the voltage requirements. The switching frequency is 2500 Hz, modulation index equals to 1 and APOD-PWM is applied to drive all the 12 switches. The switching sequence and the mode operation for conventional topology are shown in Figure 2(b).



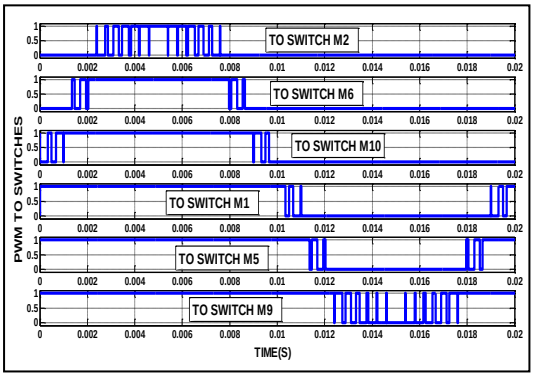
(a) Multistate carrier and a sinusoidal signal



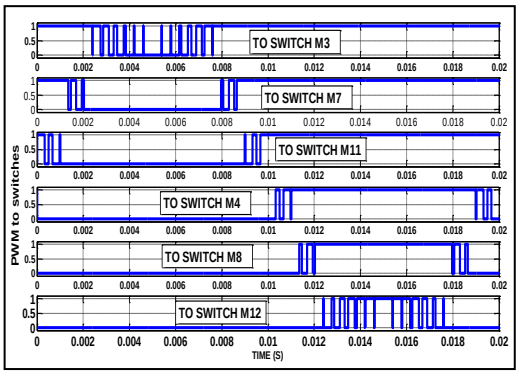
(b) mode operation for conventional topology

Figure 2. Multistage carrier APOD-PWM conventional and mode operation

The results of APOD-PWM signals for driving all 12 switches in one complete cycle are illustrated in Figure 3(a), while Figure 3(b) shows the inverted signal. A combination of all switching sequences mentioned is performed to complete the waveform the output of converter.



(a) Positive gate signal



(a) Negative gate signal

Figure 3. Complete gate signals all of l2 switches for seven levels in conventional topology

The switching sequences of the conventional topology are shown in Table 1. The number of output voltage levels is 2n+1, where n is the number of DC sources. Here the output voltage levels are at +3VDC, +2VDC, +VDC, 0, -VDC, -2VDC and -3VDC. When the switches M1, M2, M5, M6, M9 and M10 are turned on, the output voltage is +3VDC. However, when the switches M3, M4, M7, M8, M11 and M12 are turned on, the output voltage is -3VDC. Similar switching is also done for other voltage levels. The output voltage is, $Vout = Vo1 + Vo2 + Vo3$

Table 1. Full operation for seven levels output of the conventional MLI topology

Mode	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	V_{out}
4	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	+3VDC
3	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	+2VDC
2	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	ON	OFF	+VDC
1	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	0
5	OFF	OFF	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	OFF	-VDC
6	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	-2VDC
7	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	-3VDC

3. THE PROPOSED CASCADED MULTILEVEL INVERTER TOPOLOGY

Obviously, the main advantage of the proposed 7 levels single phase multilevel inverter topology is the significant reduction of semiconductor switches compared to the conventional 7 level cascaded H-Bridge multilevel inverter. The conventional topology uses 12 switches and three DC sources. However, with the new topology, about half of the semiconductor switches cost can be reduced. Figure 5 shows the proposed topology that consists of six switches and three DC sources. Switches M1, M2, M3 and M4 in the full bridge works in bidirectional operation whereas switches M5 and M6 are used to control the input voltage in order to obtain the desire output voltage level in unidirectional operation. The details description, operation and switching scheme for the proposed topology will be explained in the next section.

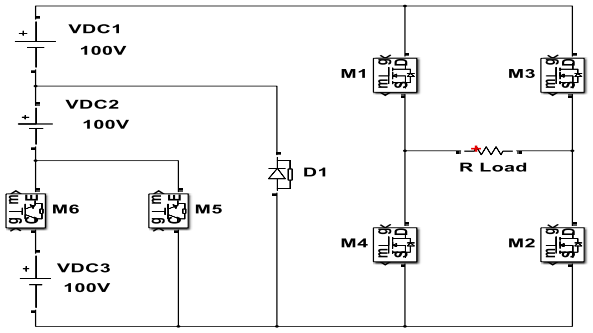
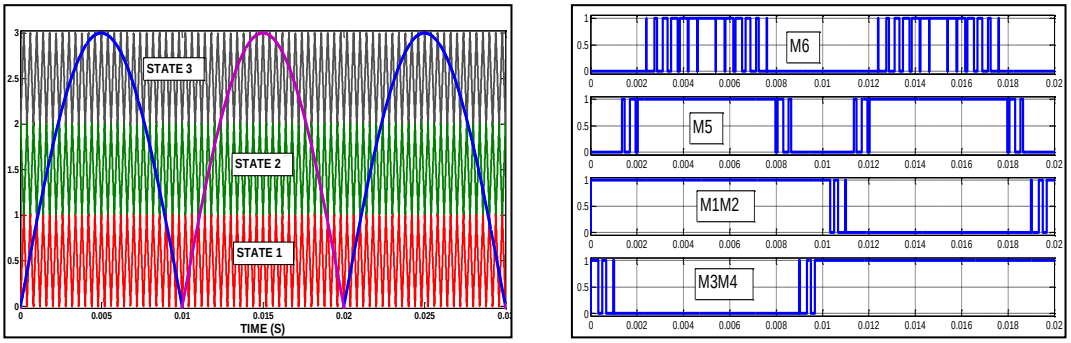


Figure 5. Proposed topology of a 7 levels single phase MLI

3.1. Switching Scheme and Mode of Operation

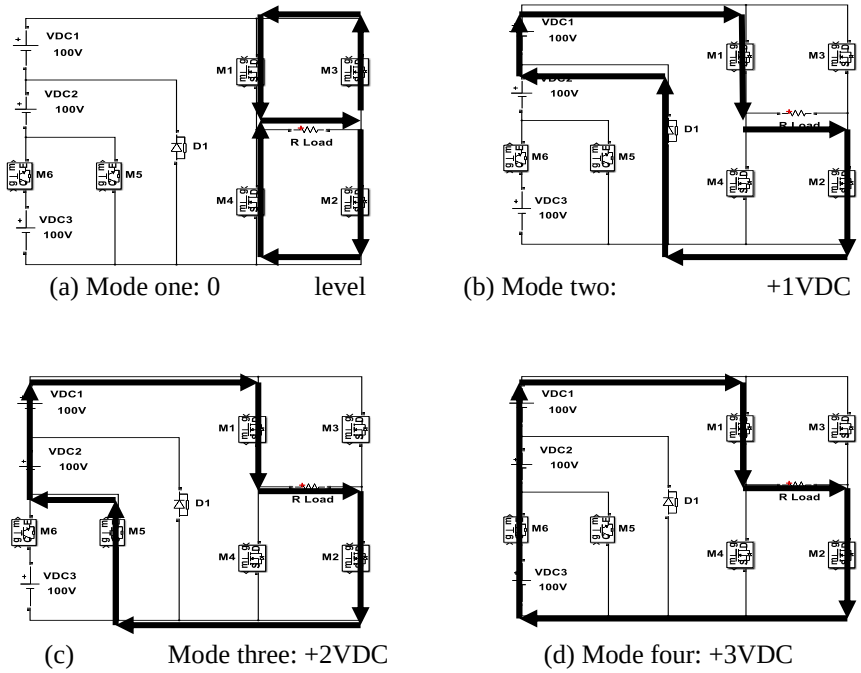
In the proposed topology, only three saw-tooth carrier signals and a sinusoidal reference signal for modulator are required in order to produce seven levels of the output voltage as shown in Figure 6 (a). In this paper, APOD-PWM switching scheme technique is adopted and simplified. Reduction in number of switches operated will reduce the total power dissipated in converter. With the proposed topology, the output voltage levels are produced only at positive polarity part. Figure 6 (b) shows the levels generation part for one complete cycle. In addition, APOD-PWM signal produced is used to drive the high-frequency switches M6 and M5 at the generated levels for one complete cycle as shown in Figure 6 (b). Meanwhile, the low-frequency signals used to drive switches M1, M2, M3 and M4 in the H-Bridge with a frequency of 50 Hz. The change in polarity occurs only at the zero voltage crossing. The details of switching operations of the positive and negative polarities are shown in Table 2.



(a) Three states Complete (b) Complete gate signals for level generation part

Figure 6. Three states carrier APOD-PWM, proposed MLI, Ma=1, switching frequency = 2500 Hz

Based on the proposed switching scheme as shown in Figure 6, the operation modes of the proposed converter are shown in Figure 7. The operating in mode 2 using only one diode in conduction to produce of level +VDC and only one switch of high frequency switching in mode 3 and mode 4 operating to produces +2VDC and +3VDC compared to conventional topology that used 6 switches. The sequence switches operating of proposed topology are (M1-M2-M3-M4) in mode 1 operation, (M1-M2-D1) in mode 2 operation, (M1-M2-M5) in mode 3 operation and (M1-M2-M6) in mode 4 operation.



(a) Mode one: 0 level (b) Mode two: +1VDC

(c) Mode three: +2VDC (d) Mode four: +3VDC

Figure 7. Mode of operation for the proposed topology

Table 2. Full operation for seven levels output of the proposed MLI topology

Operating Mode	M1	M2	M3	M4	M5	M6	D1	V_{out}
1	ON	ON	OFF	OFF	OFF	ON	X	+3VDC
2	ON	ON	OFF	OFF	ON	OFF	X	+2VDC
3	ON	ON	OFF	OFF	OFF	OFF	✓	+1VDC
4	ON	ON	ON	ON	OFF	OFF	X	0
5	OFF	OFF	ON	ON	OFF	OFF	✓	-1VDC
6	OFF	OFF	ON	ON	ON	OFF	X	-2VDC
7	OFF	OFF	ON	ON	OFF	ON	X	-3VDC

4. SIMULATION RESULTS

MATLAB-Simulink simulator was used in order to confirm the proposed switching scheme and the proposed converter topology operations. In this simulation only resistive R load is considered. Thus, the output voltage waveform which consist of +VDC, 0 and –VDC are shown in Figure 8. Meanwhile the output current waveform is also shown in Figure 8. By using Fast Fourier Transform (FFT) analysis methods, percentage of the output voltage THD for both topologies is compared as shown in Figure 9. The proposed topology produced higher fundamental output voltage compared to the conventional topology despite maintains low harmonic distortion.

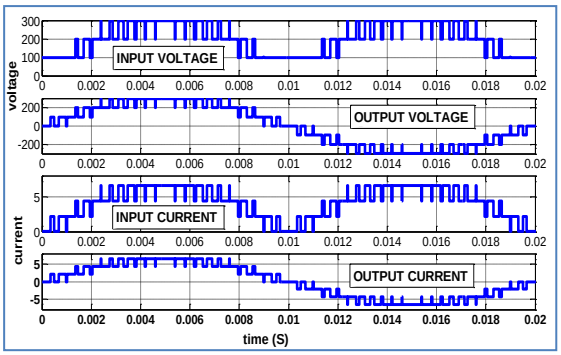
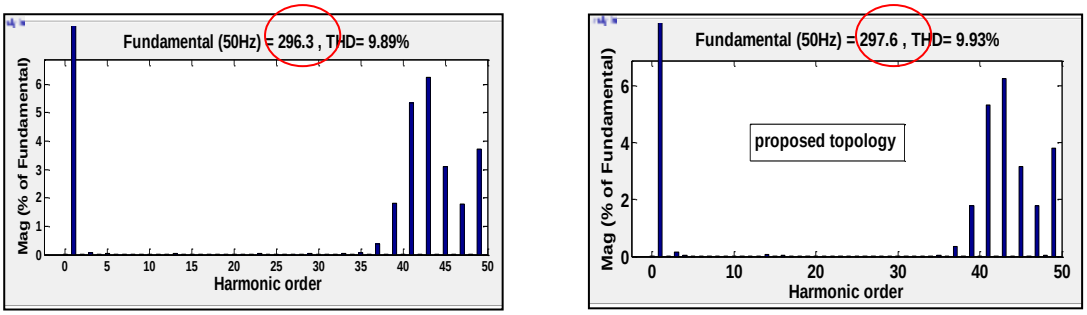


Figure 8. Input voltage and current of polarity generating part and output voltage/current



(a) Conventional topology (b) Proposed topology

Figure 9. percentage of THD and voltage fundamental for both proposed and conventional topologies

Figure 10 shows the comparison in term of number of semiconductor switches required according to number of level between the proposed and the conventional topologies. It is clearly shows that the number of semiconductor switches is reduced significantly, hence shrinking of the size and cost of the MLI can be considered.

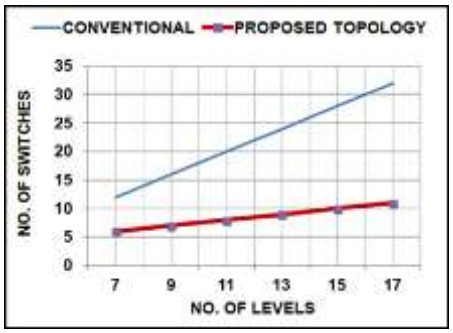


Figure 10. Required switches for multilevel inverter

5. CONCLUSION

This paper proposed a new topology of H-bridge multilevel inverter with less number of semiconductor switches compared to the conventional topology. The controlling of the switches become less complex due to less semiconductor switches required. Consequently, the installation area and size of the converter also reduced. The result shows that the proposed topology produces slightly higher fundamental output voltage compared to the conventional topology whereas the harmonics distortion performance is comparable to the conventional topology.

ACKNOWLEDGEMENTS

The authors wish to thank the Ministry of Higher Education Malaysia (MOHE). They also expressed appreciation to the funding provided Research University Grant with the vote 02G09, Universiti Teknologi Malaysia (UTM).

REFERENCES

[1] J. Rodriguez, *et al.*, "Multilevel inverters: a survey of topologies, controls, and applications," *Industrial Electronics, IEEE Transactions on*, vol. 49, pp. 724-738, 2002.
[2] T. H. M. Babaei E. and Hosseini S. H., "A novel structure for multilevel converters," *Proceeding of eighth international conference on electrical machines and systems China*, vol. II, pp. 1278–83, 2005.
[3] A. T. El-Naggar K., "Selective harmonic elimination of new family of multilevel inverters using genetic algorithms," *Elsevier J Energy Convers Manage*, vol. 49, pp. 89–95, 2008.
[4] K. S. S. a. M. V. Prasad, "Analysis and Simulation of New Seven Level Inverter Topology," *International Journal of Scientific and Research Publications*, vol. 2, 2012.
[5] N. G. T. V. V. S. Lakshmi, *et al.*, *"Cascaded seven level inverter with reduced number of switches using level shifting PWM technique,"* International Conference on Power, Energy and Control (ICPEC '13), pp. 676–680, 2013.
[6] D. G. Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters," *Industry Applications, IEEE Transactions on*, vol. 37, pp. 574-582, 2001.
[7] S. Mekhilef and M. N. A. Kadir, "Novel Vector Control Method for Three-Stage Hybrid Cascaded Multilevel Inverter," *Industrial Electronics, IEEE Transactions on*, vol. 58, pp. 1339-1349, 2011.
[8] S. Mekhilef, *et al.*, "Modeling of Three-Phase Uniform Symmetrical Sampling Digital PWM for Power Converter," *Industrial Electronics, IEEE Transactions on*, vol. 54, pp. 427-432, 2007.
[9] S. M. R. A. Ahmed and H. W. Ping, *"New multilevel inverter topology with minimum number of switches*," in Proceedings of the 14th International Middle East Power Systems Conference (MEPCON '10),Cairo University, Cairo, Egypt, pp. 1862–1867, 2010.
[10] M. A. Chulan and A. H. M. Yatim, *"Design and implementation of a new H-bridge multilevel inverter for 7-level symmetric with less number of switches,"* in Power and Energy (PECon), 2014 IEEE International Conference on, pp. 348-353, 2014.
[11] J. J. Nedumgatt, *et al.*, *"A multilevel inverter with reduced number of switches,"* in Electrical, Electronics and Computer Science (SCEECS), 2012 IEEE Students' Conference on, pp. 1-4, 2012.
[12] V. G. Agelidis and M. Calais, "*Application specific harmonic performance evaluation of multicarrier PWM techniques,"* in Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE, vol. 1, pp. 172-178, 1998.

BIOGRAPHIES OF AUTHORS

Megat Azahari Chulan received the B.Eng degree in Electrical Engineering from Universiti Teknologi Malaysia (UTM), Skudai, Malaysia in 1999 and the M.Eng. In Electrical Energy and Power System from Universiti Malaya (UM) Malaysia in 2007. Currently pursuing PhD in Electrical Engineering at Universiti Teknologi Malaysia.

Mohd Junaidi Abdul Aziz was born in Kuala Terengganu, Malaysia, in 1979. He received his B.S. and M.S. degrees in Electrical Engineering from the Universiti Teknologi Malaysia (UTM), Kuala Lumpur, Malaysia, in 2000 and 2002, respectively; and his Ph.D. in Electrical Engineering from The University of Nottingham, Nottingham, England, UK, in 2008. Since 2008, he has been with the Faculty of Electrical Engineering, UTM, where he is presently a Senior Lecturer. His current research interests include power electronics and electric vehicles with a special focus on battery management systems.

Abdul Halim Mohamed Yatim (M'89–SM'01) received the B.Sc. degree in electrical and electronic engineering from Portsmouth Polytechnic, Portsmouth, U.K., in 1981 and the M.Sc. and Ph.D. degrees in power electronics from Bradford University, Bradford, U.K., in 1984 and 1990, respectively. He is currently a Professor with the Universiti Teknologi Malaysia (UTM), Skudai, Malaysia. Dr. Yatim is a registered Professional Engineer with the Malaysian Board of Engineers.

Mohd Zaki Daud received his Bachelor of Engineering in Electrical Engineering from University of Southampton, U.K. in 1995. He then received his Master of Science in Electrical Power from University of Newcastle upon Tyne, U.K. in 1996. Since May 1997, he has been with the Faculty of Electrical Engineering, Universiti Teknologi Malaysia. His research interests are in the areas of estimation techniques in power electronics and electric drives, and also engineering education. He is also a Member of IEEE and an Executive Member of Power Electronics Malaysia Chapter of the IEEE Malaysia Section.