A HIGH SPEED GEIGER MODE PHOTODIODE GATING CIRCUIT MODELLING USING MATLAB

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ABSTRACT

Single photon avalanche diode (SPAD) is developing constantly in imaging detection area. SPAD device is very sensitive to the fabrication technique used. Different geometry, shape and size will result in devices with various current, voltage and also count rate performances. The development of new SPADs is a time and money consuming process where modelling or simulation tools will be able to help in shorten the development time and reduced the money involved. Currently, 130 nm SPAD model circuit is not available in Cadence electronic design automation (EDA) tools' library. Therefore, there is no promising device model of SPAD that can be utilized with integrated readout circuit to predict the performance of the photon counting circuit which is developed using Cadence EDA tool. This project has been carried out to model SPAD detectors for 130 nm technology which allows researchers to simulate the behaviour of the incoming detected photon. Moreover, this project is focused on the characterisation and optimisation the mathematical SPAD model on passive quenched circuit. Hence that, the performance of the passively quenched SPAD model is investigated at low and high photon counting rate by using MATLAB Simulink. The whole project is divided into three parts which are modelling SPAD, modelling passive quenching circuit as well as compare and optimize the performance of the quenching circuit. The effect of resistance and capacitance value of SPAD model is identified. On the other hand, SPAD simulation model circuit which have been used by the previous researchers is analyzed and applied in low voltage technology. The simulation analysis on the circuit modelling is performed using spice parameters of standard 180 nm and 130 nm complementary metal-oxide semiconductor (CMOS). In conclusion, modelling SPAD will able to help researchers to understand and predict the behaviour of the SPAD and future work can be implemented by using active quenching as it enabling SPAD to operate in higher frequency. At the end of this project, a dedicated SPAD model as photon detector simulation model in low voltage CMOS process is modeled with dead time 0.21 μs which is around 4.7 MHz.

ABSTRAK

Single photon avalanche diode (SPAD) terus berkembang di kawasan pengesanan imej. Peranti SPAD sangat sensitif terhadap teknik fabrikasi yang digunakan. Geometri, bentuk dan saiz yang berbeza akan menghasilkan peranti dengan pelbagai arus, voltan dan juga prestasi kadar mengira. Pembangunan SPAD yang baru adalah proses yang mengambil masa dan wang di mana pemodelan atau alat simulasi dapat membantu memendekkan masa pembangunan dan mengurangkan wang yang terlibat. Pada masa ini, litar model 130 nm SPAD tidak terdapat dalam kandungan Cadence EDA. Oleh itu, tidak ada model peranti yang baik bagi SPAD yang boleh digunakan dengan litar integrasi pembacaan untuk menjangkakan prestasi litar pengiraan foton yang dibangunkan menggunakan Cadence EDA. Projek ini telah dijalankan untuk model pengesan SPAD untuk teknologi 130 nm yang membolehkan para penyelidik mensimulasikan tingkah laku ketibaan foton. Projek ini juga mencirikan dan mengoptimumkan model SPAD matematik pada litar "*quenching*" pasif. Sehubungannya, prestasi model SPAD litar "*quenching*" pasif disiasat pada kadar pengiraan foton yang rendah dan tinggi dengan menggunakan MATLAB Simulink. Seluruh projek dibahagikan kepada tiga bahagian iaitu pemodelan SPAD, pemodelan litar "*quenching*" pasif serta membandingkan dan mengoptimumkan prestasi litar "*quenching*". Kesan nilai rintangan dan kapasitaan model SPAD telah dikenalpasti. Sebaliknya, litar model simulasi SPAD yang telah digunakan oleh penyelidik terdahulu telah dianalisis untuk digunakan dalam voltan rendah. Analisis simulasi pada pemodelan litar telah dilakukan dengan menggunakan parameter spice 180 nm dan 130 nm CMOS. Kesimpulannya, pemodelan SPAD membantu para penyelidik memahami dan meramalkan tingkah laku SPAD dan kerja masa depan dilaksanakan dengan menggunakan aktif "*quenching*" memandangkan ia membolehkan SPAD beroperasi dalam frekuensi yang lebih tinggi. Akhirnya, model SPAD yang berdedikasi sebagai model simulasi pengesan foton dalam voltan rendah proses CMOS direka bentuk dengan *dead time* sebanyak 0.21 μs iaitu hampir 4.7 MHz.

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LIST OF ABBREVIATIONS

AQC	-	Active Quenching Circuit
APD	-	Avalanche Photodiode
CMOS	-	Complementary Metal-Oxide Semiconductor
DCR	-	Dark Count Rate
EDA	-	Electronic Design Automation
FWHM	-	Full Width at Half Maximum
GUI	-	Graphical Use Interface
HDL	-	Hardware Description Language
Kp	-	Transconductance
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
PQC	-	Passive Quenching Circuit
Si	-	Silicon
SPAD	-	Single Photon Avalanche Diode

LIST OF SYMBOLS

Q_C	-	Avalanche Charge
I_D	-	Avalanche Current
V_A	-	Bias Voltage
V_B/V_{BD}	-	Breakdown Voltage
t_d	-	Dead Time
V_{EX}	-	Excess Voltage
C_D	-	Junction Capacitance
R_L	-	Quenching Circuit Ohmic Resistance
t_q	-	Quenching Time Constant
t_r	-	Recharge Time Constant
V_S	-	Sensing Voltage
R_D	-	SPAD Resistance
C_P	-	Stray Capacitance

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CHAPTER 1

INTRODUCTION

1.1 Project Background

Single photon avalanche diode (SPAD) are avalanche photodiodes that operate above the breakdown voltage which is also known as geiger mode so as to be sensitive to single photons. It is developing constantly and quickly where it is commonly involved in the area of image detecting and sensing. It is highly desirable due to the high sensitivity characteristic which enable the device to be used for imaging detection in an extreme low-level light conditions [1]. Recently, the small pixel sensitivity of SPAD is in demand. These detectors are capable of capturing individual photons with high time-of-arrival resolution [2].

Before the researchers focus on SPAD, photomultiplier tubes (PMTs) have been known as the best sensor technology in nuclear and biological imaging for a long while purely because of its low noise per unit area. SPAD offers several advantages over other image detection devices in terms of low fabrication costs, overall performance, portability and its suitability to buid the integrated systems [3]. Besides the high sensitivity, the ability of the device to operate under high speed is another highly in demand feature of the SPAD. A lot of the researches have been carried out to enhance the fast timing feature of the SPAD [1, 4]. Geiger mode megapixel CMOS imagers are still not available commercially [5], the focus of the SPAD's development is not limited to the fabrication but also the modelling area. This is because the SPAD device is very sensitive to the fabrication technique used where different geometry, shape and size will result in devices with different current voltage and also count rate performances, respectively. Development in modelling SPAD will be able to help

researchers to estimate the performance prior to fabrication. Currently, 130 nm SPAD model circuit is not available in Cadence EDA tools library and Mentor Graphics library. It requires the user to create cell or build a module using costly tools such as Agilent advanced design system (ADS). MATLAB has the ability to be used as an alternative tool to build the SPAD module and it is ready to be used with other EDA tools.

1.2 Problem Statement

The design of SPAD is very time and money consuming due to the fabrication process. There is a need of an accurate model for the researchers to understand the SPAD. Currently, 130 nm SPAD model circuit is not available in Cadence EDA tools library. There is no promising device model of SPAD that can be utilized with integrated readout circuits to predict the performance of the photon counting circuit which is developed using Cadence EDA tool which makes the development and research of the SPAD become harder for researchers [6]. There are a lot of on-going researches to model the behaviours of SPAD.

SPAD performance is mainly influenced by resistance and capacitance in SPAD thus the effect of resistance and capacitance value of the SPAD model will be identified and it will help to estimate the performance. SPAD simulation model circuits which have been used by the previous researchers on high voltage technology will be analyzed in order to improve the design of the proposed SPAD model which is suitable in low voltage technology.

Dead time of SPAD is an issue that is gating the high speed performance of SPAD. In previous researches, the frequency achieved is 200 kHz [7] with passive quenching. Passive quenching circuit is optimized in order for SPAD to operate in higher frequency which is in a range of Mega Hz.

1.3 Objectives

The aim of the project is to model SPAD detectors which adopts 130 nm CMOS technology utilizing thin gate technology devices. It allows researchers to simulate the behaviour of the SPAD by using MATLAB.

Below are the objectives which need to be achieved in order to realise the aim of the project:

1. To investigate SPAD quenching model which is suitable for low and high frequency.
2. To characterize and optimize the low voltage SPAD model on passive quenched SPAD circuit.
3. To identify the effect of resistance and capacitance value of SPAD model.

1.4 Project Scopes

The project scopes are described as below:

This project is focused on modelling SPAD. SPAD is found in two types which are thick and thin junction of SPAD[8]. Thin junction SPAD is the device considered and modeled in this project. Besides that, this project is focused on low voltage 130 nm Silicon (Si) avalanche photodiode. The modelling aspect of the project involves modelling the SPAD and the passive quenching circuit of SPAD. The relationship of voltage breakdown (V_B) to the output voltage and dead time (t_d) of the SPAD which affects the frequency response of the SPAD is studied. Furthermore, this project is performed using MATLAB Simulink and the result is analyzed by using MATLAB. TSMC parameter file from Pspice is implemented in the Simulink components. The parameter such as thickness of oxide, capacitance and threshold voltage is different in 130 nm and 180 nm CMOS process. These values are taken from TSMC parameter file from Spice and is applied in this project.

1.5 Thesis Outline

This thesis contains the research study of thin junction Silicon SPAD in low voltage technology. The main aim of this thesis is to model a high speed geiger mode photodiode by using MATLAB Simulink. Below are the outline for 5 chapters include in the thesis:

Chapter 1: This chapter contains the introduction of this research project and brief discussion on background, problem statement, aim, objectives and project scopes of this research project.

Chapter 2: This chapter covers the literature review of the project. It contain the concept of this project and reviewed on other related research work.

Chapter 3: This chapter defines the methodology used in the project, flow charts are included for better description. It explains the procedure to model and simulate the design. Performance parameters used to compare and analyze the SPAD system is also discussed.

Chapter 4: This chapter contains the results for this project. Simulation results using different parameters for high voltage and low voltage are analyzed and investigated.

Chapter 5: The chapter contains the summary of crucial results and findings. Besides that, this chapter also includes the directions and suggestions of future works for the current project.

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