OPTIMAL VOLTAGE SAG MONITOR PLACEMENT IN POWER SYSTEM BY ANALYZING MONITOR REACH AREA AND SAG SEVERITY INDEX

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Specially dedicated
to my supervisor and family who encouraged
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ABSTRACT

Voltage sag is one off severe power quality issues. Its effect can cause huge losses to industries which using sensitive equipment like microcontroller and computer. To minimize these losses, industrial customers need to understand how power quality is impacting their system and how to mitigate its effects. Voltage sag happens frequently and it causes by random and unpredictable factors. So, the voltage sag monitoring system should able to monitor the whole power system but to place voltage sag monitor at all buses is not economic. Objectives of this studied are to find the optimal number and placement of voltage sag monitors in IEEE 30-bus system. In proposed method, first, the concept of monitor reach area has been used. In this studied, voltage sag was represented by balance and unbalance fault with fault impedance, Z_f equal to 0Ω. IEEE 30 bus system was constructed on *PowerWorld* software in order obtained fault voltage on every bus. Then, monitor reach area matrix was formed by comparing fault voltage with selected voltage threshold,α. After that, monitor reach area was analyzed by using Branch and Bound method to find minimum number and all possible arrangements of VSM. Finally, to optimally place the identified number of VSM, all possible combinations of those VSM in the power system are evaluated using sag severity index. The proposed algorithm has been implemented and tested on the IEEE 30-bus test systems to show effectiveness of the proposed method in finding the optimal voltage sag monitor placement in power system. The proposed method has been tested with 2 different α which are 0.55 p.u. and 0.80 p.u. respectively. The proposed method successfully found the optimal number and its placement for monitoring the whole IEEE 30 bus system with respective α value. Based on result, for α equal to 0.55, VSM need to be installed on bus 6, 17, 25 and 30 to monitor voltage sag on IEEE 30 bus system and for α equal to 0.80 p.u., VSM only need to be place at bus 25 for monitoring voltage sag on the test system.

ABSTRAK

Voltan lendut (VL) adalah satu isu kualiti kuasa yang memudaratkan. Kesannya boleh menyebabkan kerugian besar kepada industri yang menggunakan peralatan sensitif seperti pengawal mikro dan komputer. Untuk mengurangkan kerugian, pihak industri perlu memahami bagaimana VL memberi kesan kepada sistem dan bagaimana untuk mengurangkan kesannya. VL berlaku dengan kerap dan disebabkan oleh faktor-faktor rawak dan tidak dapat diramal. Maka, sistem pemantau voltan lendut (PVL) harus dapat memantau keseluruhan sistem kuasa tetapi untuk meletakkan PVL di kesemua bas adalah tidak ekonomi. Objektif kajian ini ialah bagi mencari bilangan dan penempatan optimum PVL dalam sistem IEEE 30 bas. Dalam kaedah dicadangkan, konsep pemantau jangkauan kawasan (PJK) digunakan. Dalam kajian ini, VL diwakili oleh kerosakan seimbang dan tidak seimbang dengan impedan kerosakan, Z_f adalah 0Ω. Sistem IEEE 30 bas telah dibina menggunakan perisian *PowerWorld* untuk mendapatan voltan kerosakan. Kemudian, matriks PJK dibentuk dengan membandingkan voltan kerosakan dengan voltan ambang dipilih, α. Selepas itu, matriks PJK dianalisa menggunakan kaedah Branch dan Bound untuk mencari bilangan minimum dan semua kemungkinan aturan PVL. Akhir sekali, untuk meletakkan PVL secara optimum, semua kemungkinan kombinasi PVL dalam sistem kuasa adalah dinilai menggunakan indeks keterukan mengendur. Algoritma yang dicadangkan telah dilaksanakan dan diuji pada sistem IEEE 30-bas untuk menunjukkan keberkesanan kaedah yang dicadangkan dalam mencari penempatan PVL yang optimum. Kaedah yang dicadangkan telah diuji dengan 2 nilai α berbeza iaitu 0.55 p.u. dan 0.80 p.u.. Kaedah yang dicadangkan berjaya menemui bilangan dan penempatan optimum untuk memantau keseluruhan IEEE 30 sistem bas untuk nilai α masing-masing. Berdasarkan keputusan, untuk α bernilai 0.55 p.u., PVL perlu dipasang pada bas 6, 17, 25 dan 30 untuk memantau voltan mengendur pada IEEE 30 sistem bas dan untuk α bernilai 0.80 p.u., PVL hanya perlu diletakkan di bas 25.

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LIST OF ABBREVIATIONS

SSI	-	Sag Severity Index
B&B	-	Branch and Bound
PQ	-	Power Quality
VSM	-	Voltage Sag Monitor
3LF	-	3 Phase Balance Fault
DLG	-	Double Line to Ground Fault
SLG	-	Single Line to Ground Fault
MRA	-	Monitor Reach Area
IEEE	-	Institute of Electrical and Electronics Engineer
rms	-	Root Mean Square
AC	-	Alternating Current
FV	-	Fault Voltage
TSP	-	Travelling Salesman Problem

LIST OF SYMBOLS

Z_f	-	Fault Impedance
Ω.	-	Ohm
p.u.	-	per unit
B	-	Susceptance
R	-	Resistance
X	-	Reactance
Y	-	Admittance
Z	-	Impedance
V	-	Volt
kV	-	kilovolt
MVAr	-	MegaVoltAmpere (reactive)
KVA	-	Kilo.Volt.Ampere
MW	-	MegaWatt

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CHAPTER 1

INTRODUCTION

1.1 Background of the study

When traditional method almost replaced by sophisticated and modern technology, power quality (PQ) issues become more crucial and ignorance of PQ issues will trigger a huge losses to industries [1]. Nowadays, almost everything will be controlled by computer and micro-controller. Transportation, manufacturing, military, telecommunication and etc. already integrated with computer to make it more reliable and efficient but this sophisticated equipment is expensive and very sensitive [2]. For electric companies, detecting and monitoring such disturbances in their whole electrical systems is a great challenge [3]. The development of the sophisticated man made machine need to be support by development of power quality means that modern and sophisticated equipment required a good quality of power supply [4].

One of the severe and critical power quality issues is voltage sag [5]. Voltage sag happens when the rms voltage decreases between 10 and 90 percent of nominal voltage for half cycle to one minute [6]. Voltage sag can cause huge damage to electronic equipment and bring big losses to industries [7]. Inrush current cause by voltage sag is high in magnitude since voltage varied in very short time [7].

Missile by military may strike a wrong place if the sensor gives a wrong signal and telecommunication may not be available for a week since equipment was damaged by voltage sag and need to be replaced.

1.2 Problem Statement

The costs cause by voltage sag show up in the forms of plant downtime, equipment replacement, lost work in process, additional labor and etc. Without the ability to monitor and gain a comprehensive understanding of the impact of voltage sag on industrial processes, these costs will continue to go unaddressed. However, with the knowledge to identify and mitigate voltage sag events, process reliability can be significantly improved. But to place power quality monitor in every bus on power system is not economic. So, optimal number and placement of voltage sag monitors need to be determine to reduce the voltage sag monitoring installation cost on power system.

Optimization problem:

- Objective/function: To determine minimum number of PQM and it locations.
- Constraint: Able to monitor voltage sags at all buses.

1.3 Objectives of Project

Objectives of this project are:

1. To determine the minimum number of voltage sag monitor on IEEE 30 bus system.

2. To identify the optimum placement of voltage sag monitor on IEEE 30 bus system.

1.4 Scope of Project

This project has been limited as below scopes:

1. Voltage sag represented by balance and unbalance fault on bus with fault impedance, Z_f, is 0Ω.
2. Proposed method tested on IEEE 30-bus system.
3. *PowerWorld* software was used for system bus analysis (fault voltage) and *Microsoft Excel* software was used to get the optimization of VSM number and location.

1.5 Thesis Outline

This project report consists of five main chapters which are introduction, literature review, methodology, results and discussion and conclusion.

Chapter 1 of this project report will be focused on the general briefing about the project which contains background of the project, project objectives, scopes of the project, problem statement and project report outline.

Chapter 2 will be more on the discussion about literature review on the voltage sag, monitor reach area method, Brach and Bound algorithm and sag severity index concept. This chapter also discussed on the related previous work done by other researcher on optimal voltage sag monitor placement.

Chapter 3 is the methodology for this project. In this chapter, the method proposed will be explained in further details on how to model, simulate and analyze the power system in order to obtain the optimal voltage sag monitor placement.

Chapter 4 focused on the results obtained in the chapter 3. The results will be analyzed using appropriate method. The analysis will verify the ability of result obtained in fulfill the objective of this study.

Chapter 5 is the main conclusion of this project, which will further discuss about the results of this project. This chapter also provides suggestion of future works.

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