DESIGN AND ANALYSIS OF A 2.5-GHz OPTICAL RECEIVER ANALOG FRONT-END USING GEIGER MODE PHOTODIODE IN A 0.13 μm CMOS PROCESS

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Specially dedicated
to my supervisor and family who encouraged
me throughout my journey of
education.

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ABSTRACT

The optical receiver analog front-end using geiger mode photodiode have several design challenges, especially in high-speed application. The parasitic capacitance (C_{PD}) of the geiger mode photodiode (PD) is large, can be several pico farads which significantly limits the bandwidth (BW) of the geiger mode photodiode. In addition, a very weak current signal which is generated by the geiger mode photodiode limits the number of photon count by the receiver circuit. To address this problem, the amplification stage followed the geiger mode photodiode must be designed to amplify the detected signal using a low voltage CMOS process device. Hence, low input impedance amplifier topologies such as common gate (CG) transimpedance amplifier (TIA) is usually employed. The applications of optical receiver are in high-speed optical communication system. Therefore, it is essential for the analog front-end (AFE) receiver (RX) which consists the PD and TIA to have a large bandwidth, usually in the range of several GHz. This project aims to design a 2.5 GHz optical AFE RX using PD in a 0.13 μm CMOS process. To comprehend the limitation of previous TIA topologies which have designed by the other researcher, these topologies are designed and simulated in lower supply voltage at 1.2 V and 0.13 μm CMOS process to assist the characterization of proposed TIA circuit for this project. Pre-layout simulation is performed and the circuit performance is analysed to define the topology that give the best performance to be used. Post layout simulation is performed on the chosen design. CG TIA is justified to be used in this project as the literature shows that it can achieve BW larger than 2.5 GHz compared to common source (CS) TIA. As a result, two TIAs which are the CG with common source active feedback (CSFB) and regulated cascode (RGC) are compared. With ideal resistor and ideal current source, the RGC outperformed CSFB in term of BW and gain. Hence, this project employed RGC topology to achieve the objective. The ideal circuit components are replaced with CMOS circuit to improve area and make the entire circuit fully on-chip. The BW achieved by the designed RGC TIA is 2.47 GHz with a TI gain of 53.8 dBΩ under large C_{PD} of 2 pF. It is proven by this work that the RGC TIA is capable operating in the GHz frequency range with large C_{PD} even the process shrink to 0.13 μm and the supply reduced to 1.2 V.

ABSTRAK

Penerima optik hadapan depan analog (RX AFE) menggunakan fotodiod mempunyai beberapa cabaran reka bentuk. Kapasitans parasit (paraCap) fotodiode (PD) yang besar menghadkan jalur lebar (BW) fotodiode. Di samping itu, isyarat arus yang sangat lemah yang dijana oleh fotodiode mengehadkan bilangan pengiraan foton oleh litar penerima. Untuk menangani masalah ini, tahap penguatan diikuti fotodiod mesti direka untuk menguatkan isyarat yang dikesan menggunakan peranti proses CMOS voltan rendah. Oleh itu, topologi penguat bagi impedans pemasukan yang rendah seperti penguat transimpedans (TIA) get sepunya (CG) biasanya digunakan. Aplikasi penerima optik berada dalam komunikasi optik berkecepatan tinggi. Oleh itu, adalah penting bagi penerima yang terdiri daripada PD dan TIA mempunyai jalur lebar yang besar, biasanya dalam pelbagai GHz. Projek ini bertujuan untuk merekabentuk AFE RX optik 2.5 GHz menggunakan PD dalam proses CMOS 0.13 μm. Untuk memahami batasan topologi TIA yang telah direka oleh para penyelidik yang lain sebelum ini, beberapa topologi TIA itu telah disimulasikan dalam voltan bekalan rendah pada 1.2 V dan 0.13 μm CMOS proses. Ini adalah untuk membantu pencirian litar TIA untuk projek ini. Simulasi pra-pelan reka bentuk dilakukan dan prestasi litar dianalisis bagi menentukan topologi yang memberikan prestasi terbaik dipilih untuk digunakan. Simulasi pasca pelan reka bentuk juga dilakukan. Akhirnya, penambahbaikan dibuat berdasarkan hasil poslay sim. CG TIA adalah wajar untuk digunakan dalam projek ini kerana sastera menunjukkan bahawa ia boleh mencapai BW lebih besar daripada 2.5 GHz berbanding dengan pemancar sepunya (CS) TIA. Akibatnya, dua CG TIA yang bername CG dengan maklum balas pemancar sepunya (CSFB) dan caskod terkawal (RCG) dibandingkan. Dengan perintang ideal dan sumber arus yang ideal, RGC mengatasi CSFB dari segi BW dan keuntungan. Oleh itu, projek ini mencadangkan CG dengan RGC diguna untuk mencapai matlamat projeck ini. Komponen litar yang ideal akan diganti dengan litar CMOS untuk mengurangkan kawasan permukaan cip dan menghasilkan seluruh litar bersepadu pada cip. BW yang dicapai oleh RGC TIA direka adalah 2.47 GHz di bawah CPD besar 2 pF.

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LIST OF ABBREVIATION

AFE	-	analog front end
APD	-	avalanche photodiode
BW	-	bandwidth
CD	-	common drain
CG	-	common gate
C_j	-	junction capacitance
CME	-	channel modulation effect
CS	-	common source
CSFB	-	common source feedback
DCPL	-	diode-connected pmos load
e-	-	electron
Gb/s	-	giga-bit per seconds
h+	-	hole
$I_{D(sat)}$	-	saturation current
I_{drk}	-	dark current
ImC	-	immitance converter
I_{PD}	-	photodiode current
IRCN	-	input referred current noise
IRNC	-	input referred noise current
IRVN	-	input refered voltage noise
I-V	-	current-voltage
KCL	-	Kirchhoff’s Current Law
LA	-	limiting amplifier
OC	-	optical communication
pCAP	-	parasitic capacitance
PD	-	photodiode
poslay	-	post-layout
pRC	-	parasitic resistance and capacitance
prelay	-	pre-layout

PVT	-	process, voltage supply and temperature
RCG	-	regulated cascode configuration
R_{IN}	-	input impedance
R_{ph}	-	responsivity
R_T	-	transimpedance gain
RX	-	receiver
sim	-	simulation
spec	-	specification
SSM	-	small signal model
TF	-	transfer function
TI	-	transimpedance
TIA	-	transimpedance amplifier
V_{BD}	-	breakdown voltage
V_{TH}	-	threshold voltage
Xtor	-	transistor

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter aims to provide the background knowledge, motivation, and objectives of this project. First, the background of the problem of optical receiver (RX) analog front end (AFE) using a geiger mode photodiode (PD) is presented. Second, the problem statement which clearly stated the problems that this project aims to solve is presented. Third, the objectives to address the problems are defined. Finally, the scope to make sure all objectives can be achieved within the project timeline is defined.

1.2 Problem background

The application of optical receiver is in the high-speed optical communication system. In the era of information, the volumes of data in a telecommunication network are growing rapidly. This drives and motivates the need for faster communication channels such as fiber optics. More than a century ago, the idea of using light as a carrier for signals already exists. Researchers able to demonstrate the utility of optical fiber as a medium for light propagation in the mid-1950s. Initially, fibers suffered from a high signal loss. Nevertheless, the prospect of fibre as a channel for optical signal transmission ignited extensive research in the field of optical communications. The

optical communication system using optic fiber is practically realized in the 1970s (Razavi, 2012).

A generic optical communication (OC) system consists three components, just like a typical communication system. These components are the transmitter (TX), transmission channel, and the receiver (RX). The TX is an electro-optical transducer, which converts the electrical signal to optical signal. Fiber is the transmission channel for the optical signal. The RX is a photodetector which senses the optical signal travelled through the fiber from TX end and converts it back to electrical signal. Essentially, the transmitting end includes laser driver and laser diode while the receiving end includes a geiger mode photodiode (PD) and transimpedance amplifier (TIA). Figure 1.1 shows the generic optical communication system. The optical signal will experience a considerable amount of attenuation as it travels from the TX site to RX site. Consequently, high light intensity laser must be used in TX; the PD must be highly sensitive to light; and the current signal from PD must be amplified with low noise and sufficiently wide bandwidth (BW), converting it to voltage domain.

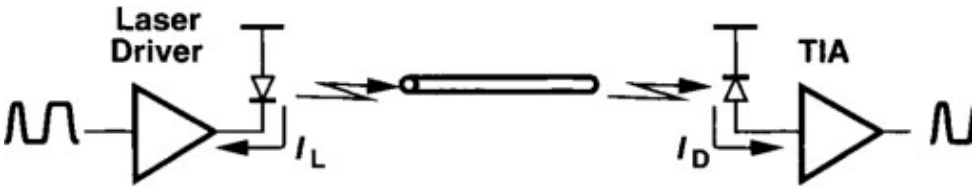

Figure 1.1 : Generic optical communication system(Razavi, 2012)

A practical OC system consists many blocks of both the transmitting site and receiving site as shown in Figure 1.2. In the transmitting site, blocks are included to convert low-speed parallel data stream to high-speed serial data stream and to deal with nonidealities behaviour such as jitter. In the receiving site, blocks are included to further improve the output signal swing of TIA and convert serial data stream back to the parallel data stream. The area of focus in the project is the analog front end (AFE) of the RX which consists the PD and TIA only.

The RX AFE presents many design challenges introduced by the demand for high performance. The noise, gain, and BW of the TIA impact the overall speed and sensitivity of the OC directly. As the trend of CMOS IC technologies is to scale down voltage supply to achieve low power requirement, raising the difficulty to design a TIA with low noise, high gain and high BW.

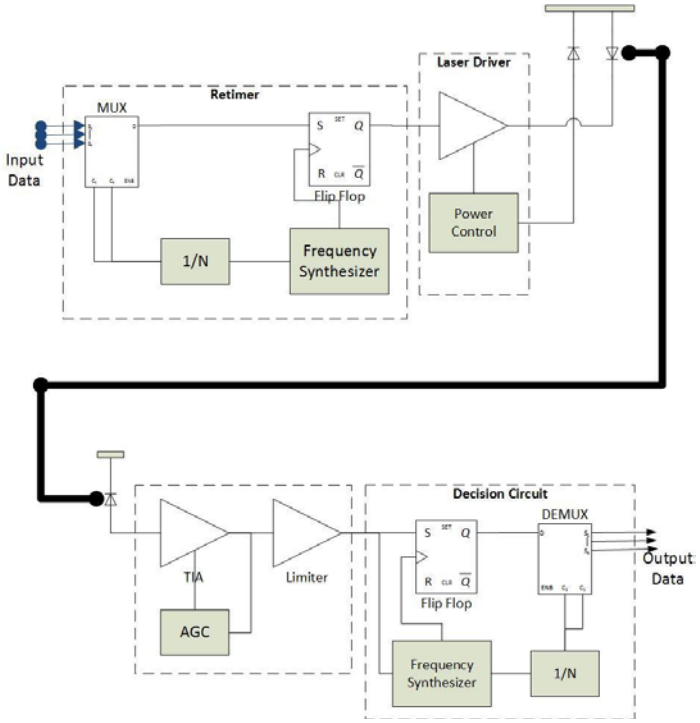

Figure 1.2 : Complete OC system(Razavi, 2012)

1.3 Problem statement

The RX AFE have two major problems. First, the parasitic capacitance (pCAP) of the PD is large, usually a few pico Farads. This pCAP is the dominant capacitance to the input of the TIA. Large pCAP means the input pole is small, in other words, the cutoff frequency due to input pole is small. This can be illustrated by the RC limited cut-off frequency equation in (1.1) where the cut-off frequency is inversely proportional to capacitance,C_d. The PD's pCAP effect significantly limited the BW of the entire system. Thus, this effect must be relaxed by designing the input impedance of the TIA to be as small as possible for the system to operate in GHz frequency range.

For example, if C_d is 1 pF and the BW is 2.5 GHz, then maximum R_L is 64 ohms which are a very small resistance value in CMOS circuit.

$$f_{RC} = \frac{1}{2\pi R_L C_d} \quad (1.1)$$

where f_{RC} is the RC limited cut-off frequency, R_L is resistance and C_d is capacitances.

The second problem is the current signal from PD usually is very weak, depending on the type of PD, the current magnitude can be as small as a few ten micro Ampere (μA) (Li, 2007). Therefore, it is very sensitive to noise. The large PD's pCAP will introduce considerable large amount of input referred noise current (IRNC) to the input of the TIA (Atef and Zimmermann, 2013). This poses a risk of data loss as the input current signal of the TIA is subjected to noise. To ensure the input current signal to be amplified and converted to voltage signal accurately, the noise and gain performance of the TIA must be designed to be sufficiently robust to separate the weak current signal from the noise. The problems mentioned above are addressed in this work by designing the RX AFE with 2.5 GHz BW with sufficiently large gain, good noise performance and low TIA input impedance.

1.4 Objectives

The objectives of this project are:

1. To design a 2.5 GHz optical analog front-end receiver using a Geiger mode photodiode and transimpedance amplifier (TIA) topology.
2. To analyze the performance of common gate TIA.
3. To optimize the performance of the design for very weak photon detection.

1.5 Scope

A scope is defined for this project in order to focus on achieving all the objectives stated above within the limited time frame given. First, the process, voltage supply and temperature (PVT) condition of the design are defined. Process technology used is Siltera 0.13 μm CMOS technology, supply voltage is 1.2 V and temperature is 300 K (27 ^{o}C). The variation of process, voltage supply and temperature is not covered. Second, the design of photodiode is not covered, realistic current and capacitance values will be used in simulation. Third, the common gate (CG) TIA topology is employed in the design. The decision of using CG TIA is justified by mathematical analysis based on literature reviews. Fourth, the layout of the design is drawn using "auto-layout" method of mentor graphic. Parasitic is extracted for post-layout simulation. Finally, this project did not cover the physical implementation of the design, hence that no physical circuit is fabricated.

1.6 Thesis outline

The following chapters of this thesis are chapter 2, 3 and 4. Chapter 2 presents the literature review on the PD and TIA. The focus on PD review is on the parameters such as current, dark current, parasitic capacitance (pCAP) and breakdown voltage. This provides insight on the realistic parameter value to be used in the modelling the

PD in circuit simulation. For TIA, various TIA topologies are studied and compared to identify research gap and justified the decision of using CG TIA topology. In chapter 3, the five major steps involved in this project are explained in detail. The result of each of the major steps is presented and discussed in chapter 4. Finally, chapter 5 concludes this work based on all the results obtained and suggestions on future work are provided.

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