REGISTER-TRANSFER LEVEL DESIGN OF SUM OF ABSOLUTE TRANSFORMED DIFFERENCE FOR HIGH EFFICIENCY VIDEO CODING

HEH WHIT NEY

UNIVERSITI TEKNOLOGI MALAYSIA

Replace this page with form PSZ 19:16 (Pind. 1/07), which can be obtained from SPS or your faculty.

REGISTER-TRANSFER LEVEL DESIGN OF SUM OF ABSOLUTE TRANSFORMED DIFFERENCE FOR HIGH EFFICIENCY VIDEO CODING

HEH WHIT NEY

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Computer and Microelectronic System)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JUNE 2018

This thesis is dedicated to my family members, lecturers and friends

ACKNOWLEDGEMENT

I would like to express my appreciation to God, in which without His blessings and graces, I would not have the perseverance, strength and wisdom to accomplish my final year project. Besides that, the completion of this thesis would not be possible without the generous assistance and support from the people around me. Hereby, I express my deepest gratitude and appreciation to the following individuals who have lend me a helping hand in times of need.

To my supervisor Dr. Ab Al-Hadi Ab Rahman, thank you for being patient, supportive and encouraging all the time. Apart from giving valuable suggestions, guidance and comments, he has continually believed and entrusted me to conduct the final year project. Despite being busy, he would always sacrifice his time to sit down with me and have a conversation over the problems I have met.

Last but not least, my appreciation goes to my family members and friends. Thank you for the continued support as it became the source of energy and motivation for me to complete my final year project. To my friends, and particularly Mr. Wong Yan Yin, thank you for being supportive and encouraging in times of difficulties.

ABSTRACT

High Efficiency Video Coding (HEVC) is the state-of-the-art video coding standard which offers 50% improvement in coding efficiency over its predecessor Advanced Video Coding (AVC). Compared to AVC, HEVC supports up to 33 angular modes, DC mode and planar mode. The significant rise in the number of intra prediction mode however has increased the computational complexity. Sum of Absolute Transformed Difference (SATD), a fast Rate Distortion Optimization (RDO) intra prediction algorithm in the HEVC standard, is one of the most complex and compute-intensive part of the encoding process. SATD alone can takes up to 40% of the total encoding time; hence off-loading it to dedicated hardware accelerators is necessary to address the increasing need for real-time video coding in accordance with the push for coding efficiency. This work proposes a Verilog-described $N \times N$ SATD hardware architecture which is based on Hadamard Transform. The architecture would support a variable block size from 4×4 to 32×32 with 1-D horizontal and 1-D vertical Hadamard Transform. At the same time, it is designed to achieve throughput optimization by pipelining and feedthrough control. The performance of the implemented SATD is then evaluated in terms of utilization, timing and power.

ABSTRAK

High Efficiency Video Coding (HEVC) merupakan standard pengekodan video terkini yang menawarkan 50% peningkatan dalam kecekapan pengekodan berbanding dengan Advanced Video Coding (AVC) yang wujud sebelumnya. Berbanding dengan AVC, HEVC menyokong 33 mod ramalan intra, mod DC dan mod planar. Walau bagaimanapun, peningkatan yang ketara dalam bilangan mod ramalan intra telah meningkatkan kerumitan komputasi tersebut. Sum of Absolute Transformed Difference (SATD) merupakan salah satu algoritma ramalan intra yang tertara dalam algoritma Rate Distortion Optimization (RDO) dalam piawaian HEVC. Memandangkan algoritma tersebut merupakan salah satu bahagian pengekodan yang paling rumit, ia mampu mengambil masa sebanyak 40% daripada jumlah masa pengekodan. Oleh demikian, komputasi tersebut perlu dilaksanakan di perkakasan yang dedikasi untuk menangani keperluan yang semakin meningkat susulan dorongan untuk kecekapan pengekodan. Dalam projek ini, satu perkakasan yang berdedikasi telah direka dalam bahasa Verilog bagi menyokong operasi $N \times N$ SATD yang berdasarkan Hadamard Transform. Rekaan tersebut menyokong saiz-saiz blok dari 4×4 hingga 32×32 dengan 1-D mendatar dan 1-D menegak Hadamard Transform. Pada masa yang sama, ia direka untuk mencapai pengoptimuman throughput dengan pengaliran paip dan pengawalan feedthrough. Perkakasan SATD tersebut akan disintesis, dinilai dan ditanda araskan dari segi penggunaan, kuasa dan masa.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AVC	-	Advanced Video Coding
BMA	-	Block Matching Algorithm
CTU	-	Coding Tree Unit
CU	-	Coding Unit
FHT	-	Fast Hadamard Transform
FSM	-	Finite State Machine
HEVC	-	High Efficiency Video Coding
HT	-	Hadamard Transform
JCT-VC	-	Joint Collaborative Team on Video Coding
LB	-	Linear Buffer
MPEG	-	ISO/IEC Moving Picture Experts Group
MPM	-	Most Probable Mode
PU	-	Prediction Unit
RDO	-	Rate Distortion Optimization
RTL	-	Register Transfer Level
SATD	-	Sum of Absolute Transformed Difference
SAV	-	Sum of Absolute Value
TB	-	Transpose Buffer
TCL	-	Tool Command Language
TE-SATD	-	Transform-Exempted SATD
VCEG	-	ITU-T Video Coding Experts Group

LIST OF SYMBOLS

T_r	-	Throughput in sample/μs
$\otimes$	-	Kronecker product
λ	-	Lagrange multiplier

CHAPTER 1

INTRODUCTION

1.1 Problem Background

In accordance with the advancement of multimedia technology, the demand for higher video resolution is growing. High definition video has become a basic expectation among consumers and they continue to push for better and smoother viewing experience. In relation, video coding standard has evolved greatly from the early MPEG standard to the H26x family. High Efficiency Video Coding (HEVC) or H.265 is the latest standard from the H26x family. Being the state-of-the-art video coding standard, it offers an identical quality to the previous Advanced Video Coding (AVC) or H.264 standard, but only requires half the bitrate of AVC. This indicates a significant improvement of 50% in the coding efficiency. In fact, before HEVC, Full HD or 1080p was the height of technology and AVC alone is sufficient. As video resolution grows larger towards 4K and 8K, higher coding efficiency is required and this is achievable with HEVC [1].

The improvement in coding efficiency is contributed mainly by the advancement in the video compression method, i.e. intra-frame prediction. Intra-frame prediction compresses a frame by looking for redundant information in the same frame. While AVC only supports 9 prediction modes, HEVC is able to support a total of 35 prediction modes. With more prediction angles, the prediction is much more accurate, less redundant and hence massively reduce the size of bits required to encode each frame. Lesser bits means smaller file size and reduced bandwidth requirement, or in other terms, more information can now be transmitted using the same bandwidth. In addition, HEVC can handles a Coding Tree Unit (CTU) of 64×64 pixel. Previously,

AVC can only supports macroblocks with greatest size of 16×16. By increasing the range of block sizes, not only that this introduces more flexibility in partitioning, but it also boost the coding efficiency, especially when processing video with large resolution.

Every prediction unit has to go through all the prediction modes to determine which is the best suited prediction mode. These modes are evaluated by a cost function calculated by Sum of Absolute Transformed Difference (SATD), a mathematical method used in fast Rate Distortion Optimization (RDO). Although the increase in the number of prediction modes enhance the compression quality, at the same time, they came at a price: substantial computational complexity.

To overcome the limitation caused by the increased complexity, SATD must be accelerated in hardware with the capability of handling variable block size. From hardware perspective, the architectural design of the SATD and the control of the architecture determines the performance of the HEVC encoder.

1.2 Problem Statement

HEVC is first introduced in 2012 but until now it is still not being recognized as the universal standard. Despite being the state-of-the-art encoding standard, HEVC is still relatively unpopular compared to AVC. One of the reason for this is that the hardware for HEVC is significantly less common. As the load has doubled for 4K or higher resolution video, most of the existing system cannot encode or decode a 4K HEVC video efficiently. In other words, HEVC is not fully compatible with existing playback devices. Some software solution exist but they are inefficient to meet the real time constraints. Therefore, in order to make HEVC a universal standard, hardware acceleration is very important.

Although HEVC offers power streaming, it comes at a price - computing complexity [2]. The mode decision is very compute-intensive. Although only 26 modes are added in the intra prediction step, it costs almost $10\times$ of computing power

for HEVC to encode at the same speed as AVC. Hence, HEVC hardware development and optimization is definitely the upcoming trend in the new silicon of the main stakeholders like Apple, AMD or Intel.

Apart from that, researches have been looking into realizing SATD into hardware as well. However, despite the largest CTU size of 64×64, most of the proposed architectures still stay at 8×8 or even 4×4. Since forthcoming adoption of larger video resolutions beyond 8K UHD are expected, size of the prediction unit are correlated and transform block will be growing towards 64×64 as well. It is important for the SATD hardware to scale accordingly and supports larger size of Hadamard Transform [3].

1.3 Objectives

The objectives to be achieved in this project are:

1. To design a variable block size SATD hardware which can support SATD operation from 4×4 to 32×32
2. To achieve throughput optimization by pipelining and feedthrough control
3. To analyze utilization, timing and power when implemented on an FPGA

1.4 Scope

The main focus throughout the project is to realize the SATD hardware. The design will not include other components of the HEVC encoder. The input of SATD is the residual block which comes from the previous stage of HEVC hardware. SATD will perform the calculation and store the absolute transformed sum for each prediction mode, taking care of blocks with sizes ranging from 4×4 to 32×32. The mode decision hardware is not included as part of SATD as well.

Apart from that, the control logic is designed to maximize the re-usability of the sub modules and to focus on pipelining and feedthrough control to obtain higher throughput. The hardware is described using System Verilog and will be implemented on an FPGA. The design will not be implemented onto ASIC.

1.5 Thesis Outline

This thesis consists of five chapters which are introduction, literature review, research methodology, results and discussion, and conclusion. Chapter 1 explains the background of this project, raises the problem and formulates the objectives and scope of this project. In chapter 2, literature review are conducted to study and review the recent achievement and contribution conducted by the experts in field. Chapter 3 describes the design methodology of the hardware architecture. The results and discussion is then covered by chapter 4. Finally, chapter 5 summarize the overall findings and the achievement of this project. Some recommended future work will be discussed as well.

REFERENCES

1. Sze, V., Budagavi, M. and Sullivan, G. J. High efficiency video coding (HEVC). *Integrated Circuit and Systems, Algorithms and Architectures*, 2014: 1–375.

2. He, Y., Ostermann, J., Domański, M., Au, O. C. and Ling, N. Introduction to the Issue on Video Coding: HEVC and Beyond. *IEEE Journal of Selected Topics in Signal Processing*, 2013. 7(6): 931–933. ISSN 1932-4553 VO - 7. doi:10.1109/JSTSP.2013.2286851.

3. Dinh, V. N., Phuong, H. A., Duc, D. V., Ha, P. T. K., Tien, P. V. and Thang, N. V. High Speed SAD Architecture for Variable Block Size Motion Estimation in HEVC encoder. *2016 IEEE Sixth International Conference on Communications and Electronics (ICCE)*. 2016. ISBN VO -. 195–198. doi: 10.1109/CCE.2016.7562635.

4. Sullivan, G. J., Ohm, J.-R., Han, W.-J. and Wiegand, T. Overview of the High Efficiency Video Coding (HEVC) Standard. *IEEE Transactions on Circuits and Systems for Video Technology*, 2012. 22(12): 1649–1668. ISSN 1051-8215. doi:10.1109/TCSVT.2012.2221191. URL `http://ieeexplore.ieee.org/document/6316136/`.

5. Zhang, M., Liu, Y. and Liu, Z. A New Fast Algorithm Based on SATD for HEVC Intra Prediction. *2016 Visual Communications and Image Processing (VCIP)*. 2016. ISBN VO -. 1–4. doi:10.1109/VCIP.2016.7805475.

6. Lainema, J., Bossen, F., Han, W. J., Min, J. and Ugur, K. Intra coding of the HEVC standard. *IEEE Transactions on Circuits and Systems for Video Technology*, 2012. 22(12): 1792–1801. ISSN 10518215. doi:10.1109/TCSVT.2012.2221525. URL `http://ieeexplore.ieee.org/document/6317153/`.

7. Lu, W., Yu, N., Nan, J. and Wang, D. A Hardware Structure of HEVC Intra

Prediction. *2015 2nd International Conference on Information Science and Control Engineering*. 2015. ISBN VO -. 555–559. doi:10.1109/ICISCE.2015.129.

8. Seidel, I., Beims Brascher, A., Guntzel, J. L. and Agostini, L. Energy-efficient SATD for beyond HEVC. *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2016. ISBN 978-1-4799-5341-7. 802–805. doi:10.1109/ISCAS.2016.7527362. URL `http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7527362`.

9. Yi, H. and Qin, H. The Optimization of HEVC Intra Prediction Mode Selection. *2017 4th International Conference on Information Science and Control Engineering (ICISCE)*. IEEE. 2017. ISBN 978-1-5386-3013-6. 1743–1748. doi:10.1109/ICISCE.2017.364. URL `http://ieeexplore.ieee.org/document/8110591/`.

10. Gu, J., Tang, M., Wen, J. and Zhang, H. A Novel SATD Based Fast Intra Prediction for HEVC. *2017 IEEE International Conference on Image Processing (ICIP)*. 2017. ISBN VO -. 1667–1671. doi:10.1109/ICIP.2017.8296565.

11. Yusuf, M. S. U. and Ahmad, M. An Efficient Inter Mode Decision Algorithm for H.264/AVC Encoding Optimization. *2015 International Conference on Electrical Engineering and Information Communication Technology (ICEEICT)*. 2015. ISBN VO -. 1–6. doi:10.1109/ICEEICT.2015.7307421.

12. Cancellier, L. H., Seidel, I., Brascher, A. B., Guntzel, J. L. and Agostini, L. Exploring Optimized Hadamard Methods to Design Energy-Efficient SATD Architectures. 2015: 113–122.

13. Cancellier, L. H., Bräscher, A. B., Seidel, I. and Güntzel, J. L. Energy-Efficient Hadamard-Based SATD Architectures. *Proceedings of the 27th Symposium on Integrated Circuits and Systems Design - SBCCI '14*. New York, New York, USA: ACM Press. 2014. ISBN 9781450331562. 1–6. doi:10.1145/2660540.2661004. URL `http://dl.acm.org/citation.cfm?doid=2660540.2661004`.

14. Ce Zhu and Bing Xiong. Transform-Exempted Calculation of Sum of Absolute Hadamard Transformed Differences. *IEEE Transactions on Circuits and*

Systems for Video Technology, 2009. 19(8): 1183–1188. ISSN 1051-8215. doi:10.1109/TCSVT.2009.2020264. URL http://ieeexplore.ieee.org/document/4811987/.

15. Silveira, E., Diniz, C., Beck Fonseca, M. and Costa, E. SATD hardware architecture based on 8×8 Hadamard Transform for HEVC encoder. *2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*. IEEE. 2015. ISBN 978-1-5090-0246-7. 576–579. doi:10.1109/ICECS.2015.7440382. URL http://ieeexplore.ieee.org/document/7440382/.

16. Chen, J., Chen, Y., Karczewicz, M., Li, X., Liu, H., Zhang, L. and Zhao, X. Coding tools investigation for next generation video coding based on HEVC. International Society for Optics and Photonics. 2015, vol. 9599. 95991B. doi:10.1117/12.2193681. URL http://proceedings.spiedigitallibrary.org/proceeding.aspx?doi=10.1117/12.2193681.

17. Bräscher, A. B., Seidel, I. and Güntzel, J. L. Improving The Energy Efficiency of A Low-area SATD Hardware Architecture Using Fine Grain PDE. *2017 30th Symposium on Integrated Circuits and Systems Design (SBCCI)*. 2017. ISBN VO -. 155–161.

18. Silveira, B., Ferreira, R., Paim, G., Diniz, C. and Costa, E. Low power SATD architecture employing multiple sizes Hadamard Transforms and adder compressors. *2017 15th IEEE International New Circuits and Systems Conference (NEWCAS)*. IEEE. 2017. ISBN 978-1-5090-4991-2. 277–280. doi:10.1109/NEWCAS.2017.8010159. URL http://ieeexplore.ieee.org/document/8010159/.

19. Silveira, B., Abreu, B., Paim, G., Greller, M., Ferreira, R., Diniz, C., Costa, E. and Bampi, S. Using Adder and Subtractor Compressors to Sum of Absolute Transformed Differences Architecture for Low-power Video Encoding. *2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2017. ISBN VO -. 409–493. doi:10.1109/ICECS.2017.8292076.

20. Liu, Z., Wang, D. and Ikenaga, T. Hardware Optimizations of Variable Block Size Hadamard Transform for H.264/AVC FRExt. *2009 16th IEEE*

International Conference on Image Processing (ICIP). 2009. ISBN 1522-4880 VO -. 2701–2704. doi:10.1109/ICIP.2009.5414107.