REGISTER TRANSFER LEVEL DESIGN OF TRANSPOSE MEMORY FOR THE TWO-DIMENSIONINVERSE DISCRETE COSINE TRANSFORM FOR HIGH EFFICIENCY VIDEO CODING

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Specially dedicated
to my supervisor, friends and family who encouraged
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ABSTRACT

The rapid revolution in consumer devices have caused in a variety of emerging video coding applications which contribute the aggressive demands on video compression requirement. The requirement of video compression efficiency getting higher. Today, Advance Video Coding (AVC) standard was replaced by the new High Efficiency Video Coding (HEVC) video compression standard due to major advance in compression compare to former. However, optimizing coding efficiency in HEVC is the root of increased computational complexity. Thus, Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT) are absolute necessary accelerator in HEVC hardware implementation. However, the hardware design of these accelerator complexity become more complicated due to flexibility given by the new video compression standard. This project aimed to design Two-Dimension Inverse Discrete Cosine Transform (2D IDCT) hardware transpose memory using hardware description language. The first objective in this project was implemented transpose memory that support different transform block dimension (4x4, 8x8, 16x16 and 32x32 transform unit). Both register-based design and RAM-based design were implemented. Secondly, a test bench was designed to validate the functionality of RTL design. Third, the integration was done between 1D IDCT building block with designed transpose memory and overall system functionality was validated. Finally, analysis was done to find out trade-off in performance, resource and power between register-based and dedicate RAM based transpose memory. The results show that register-based 2D IDCT have 2.24 times better throughput and 35.6% less energy consumption compare to RAM-based 2D IDCT. However, register-based 2D IDCT have 30 times more resource utilization compare to RAM-based 2-D IDCT. Thus, RAM-based 2D IDCT is more suitable for small electronic device. If area expenses is negligible and performance is needed, register-based 2D IDCT can be considered.

ABSTRAK

Perkembangan teknologi dalam peranti pengguna telah menyebabkan kemunculan pelbagai aplikasi pengekodan video. Ini telah menyumbangkan permintaan resolusi video yang semakin tinggi terhadap keperluan dalam video rakaman dan video ulangan. Oleh itu, H.264/AVC standard mampatan video yang lama telah diganti dengan standard H.265/HEVC yang lebih ada kebolehan untuk memampat resolusi video yang tinggi dengan kualiti yang lebih tinggi. Sebagai salah satu langkah untuk melajukan pengekodan and penyahkodan video, reka bentuk algoritma melalui perkakasan adalah munasabah. Walau bagainmanapun, perubahan yang diperkenalkan oleh standard HEVC iaitu penggunaan saiz blok yang berbeza-beza daripada saiz 4x4 kepada 32x32 dengan fleksibel telah meningkat kerumitkan dalam reka bentuk perkakasan. Projek ini bertujuan untuk mereka dua-dimensi transformasi songsang (2D IDCT) transpose memori dengan menggunakan bahasa perhuraian perkakasan (HDL). Objektif pertama dalam projek init adalah mereka transpose memori yang boleh sokong saiz blok yang pelbagain dimensi. Reka bentuk kedua-dua transpose memori adalah berasaskan register and RAM. Keduanya, ujian untuk reka bentuk telah direka untuk menguji fungsi-fungsi transpose memori supaya perkakasan berfungsi seperti yang diharapkan. Ketiga, integrasi antara transpose memori dan blok 1D IDCT telah dilaksanakan untuk menghasilkan 2D IDCT dan fungsi keseluruhan sistem telah diuji. Akhir sekali, analisis telah dilaksanakan untuk mengetahui prestasi, pengunaan kawasan dan penggunaan kuasa di antara 2D IDCT yang menggunakan register dan RAM. Keputusan menunjukkan bahawa register 2D IDCT mempunyai 2.24 kali lebih baik prestasi dan 35.6% kurang pengguanna tenaga berbanding dengan RAM 2D IDCT. Walau bagaimanapun, register 2D IDCT mempunyai pengunaan kawasan sebanyak 30 kali lebih berbanding dengan RAM 2D IDCT. Oleh itu, RAM 2D IDCT lebih sesuai untuk peranti elektronik yang kecil. Sekiranya perbelanjaan dalam pengunnaan kawasan boleh diabaikan and prestasi lebih dipentingkan, register 2D IDCT boleh dipertimbangkan.

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LIST OF ABBREVIATIONS

AGM	-	Address Generator Module
DCT	-	Discrete Cosine Transform
RAM	-	Random Access Memory
IDCT	-	Inverse Discrete Cosine Transform
SRAM	-	Synchronous Random Access Memory
HD	-	High Definition
HEVC	-	High Efficiency Video Coding
TU	-	Transform Unit
MPEG	-	Moving Picture Experts Group
ITU	-	International Telecommunication Union
VCEG	-	Video Coding Experts Group
RCDM	-	Row Column Decomposition Method
HDL	-	Hardware Description Language
FPGA	-	Field-Programmable Gate Array
SAIF	-	Switching Activity Interface Format

CHAPTER 1

INTRODUCTION

1.1 Background of Study

In recent years, having electronic devices becoming a norm and emerging of variety video coding applications have contribute the aggressive demands on video compression requirement. With the increasing diversity of electronic devices supporting digital video, growing popularity of High Definition (HD) video and people tends to look for higher frame rate and resolution for video beyond HD-formats, the requirement on recording, coding, decoding and playback ability increased vigorously due to the wish for better user video experience [1].

In order to provide higher video coding and decoding efficiency, a new video standard which is H.265/High Efficiency Video Coding (HEVC) was proposed by the MPEG and the ITU bodies to substitute the older H.264/AVC video standard [2]. Transform Unit (TU) is a basic unit for HEVC transform thereby larger TU size can improve coding/decoding efficiency. The major introduction in HEVC is using four different TU block sizes from 4x4, 8x8, 16x16 and 32x32 with higher precision (16-bit precision) as compared to AVC's 4x4 and 8x8. Because of this, the implementation of new standard using hardware imposes more challenges, data exchange complexity increased significantly due to more varying TU block size are

required to perform Discrete Cosine Transform (DCT) and inverse Discrete Cosine Transform (IDCT) [3].

For hardware implementation of HEVC video standard, there are multiple block structures and parallelism features [1]. Over the past, 2-D DCT and IDCT has been widely used in the field of block based video coding and decoding standard due to its capability to concentrate the energy of video residual data into low frequency domain and vice versa [4]. 2-D DCT is use for video compression while 2-D IDCT is use for video decompression. What this project is looking into is 2-D IDCT block, and highly focusing on implementation of transpose memory. 2-D IDCT consist of two 1-D IDCT unit and a transpose memory, the details architecture of 2-D IDCT will be provided in next chapter.

1.2 Problem Statement

For higher video coding and decoding efficiency in digital video, there are performance limitation if only using software to implement. Therefore a dedicated hardware is needed for HEVC transform block to guaranteed performance. As previously stated, the introduction of larger TU sizes by the new standard and the flexibility of supporting 4 different TU sizes from 4x4 to 32x32 bring the hardware design complexity to a new level, internal building block also need redesign to support the requirement, including transpose memory. Previously published studies [6] – [11] on implementation of HEVC transform has tended to focus on optimizing 1-D IDCT block rather than transpose memory, mostly using RAM memory design, or avoid usage of transpose memory. The studies would have been more interesting if they had also included tradeoff analysis between different memory type designs of transpose memory. Due to insufficient data for tradeoff benchmark value for different memory type transpose memory, a more comprehensive study needed. Thus, this project aims to propose a transpose memory architecture to support the new requirement in HEVC transform with two different memory type and to identify

tradeoff performance between them at top level (2-D IDCT) by analyze the performance, resource and energy consumption.

1.3 Objectives of Project

Followings are the objectives proposed for this project: -

(1) To design transpose memory using register-based memory.

(2) To design transpose memory using RAM-based memory.

(3) To develop a test bench to validate the functionality of transpose memories.

(4) To integrate transpose memories with 1-D IDCT unit to form 2-D IDCT.

(5) To analyze and determine the tradeoff in performance, resource and energy consumption between register-based design and RAM-based design at integration level.

1.4 Scope of the Study

In this project, only 2-D IDCT components will be validate and analyze while other HEVCs components will not include. The transpose memory will be design based on two type of memory which is register-based memory and RAM-based memory. For the 2-D IDCT integration, the 1-D IDCT unit will reuse existing validated design in [5], thus design of 1-D IDCT unit is not needed. Redesign of control path in existing control logic in [5] is needed due to input is not always available for second IDCT unit because of transposition delay cause by different transform unit sizes. The design of transpose memory must compatible with the 1-D IDCT unit design in [5] which use pipeline architecture and support varies transform

unit size. The design and the test bench will be done using hardware description language (HDL).

1.5 Project Report Outline

Hereby the thesis consist of total of 5 Chapter. Chapter 1 consist of background of study, problem statement, objectives of project and project report outline of this thesis. Chapter 2 consist of literature review of HEVC video and design of 2-D IDCT from previous researchers. Chapter 3 consist of all project methodology that had been deployed. Chapter 4 consist of the results of project and analysis on results. Chapter 5 concluded the whole project and make recommendation for future work.

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