CLUSTERED TWO-DIMENSIONAL MESH TOPOLOGY FOR LARGE-SCALE NETWORK-ON-CHIP ARCHITECTURE

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A thesis submitted in fulfilment of the
requirements for the award of the degree of
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Dedication to my parents, my wife, and my kids.

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ABSTRACT

Driven by the continuous scaling of Moore's law, the number of processing cores in chip multiprocessors and systems-on-a-chip are expected to grow tremendously in the near future. Connecting the different components of a multiprocessor chip in a scalable and efficient way has become increasingly challenging. Current network-on-chip (NoC) topologies are adequate for small-size networks but are not optimized for large-scale networks. Transmitted packets inside a large NoC require longer route to reach their destinations, resulting in an increase in certain performance parameters such as latency and power consumption. Thus, it is necessary to develop a new topology appropriate for large-size NoCs. In this research, we proposed a cost-effective network topology for large-size NoCs that improves performance in terms of end-to-end latency. The topology, called RaMesh, consists of clusters of mesh networks. A routing algorithm suitable for this topology was also proposed. The RaMesh architecture together with mesh, torus, and clustered 2D-mesh were simulated using Noxim (NoC simulator), C for software NoC models, and Altera ModelSim for Verilog hardware models. Simulations were conducted under different network traffic and for a variety of network sizes. Experimental results showed that RaMesh performed better than equivalent 2D-mesh and torus topologies. RaMesh topology was also benchmarked against a clustered mesh topology. Average hop count in the proposed topology was at least 22.7% lower compared to the mesh and torus. Average latency was also decreased by at least 24.66% as compared to the mesh and torus. Finally, the saturation point for the proposed topology increased by at least 15% as compared to mesh and torus.

ABSTRAK

Didorong oleh peningkatan berterusan dalam Hukum Moore, bilangan teras pemprosesan dalam multiprosesor cip dan sistem dalam satu cip dijangka berkembang dengan pesat dalam masa terdekat. Menyambung komponen yang berlainan dalam multiprosesor cip dengan cara yang cekap dan berskala tinggi telah menjadi semakin mencabar. Topologi Rangkaian-atas-Cip (NoC) semasa adalah cukup untuk rangkaian saiz kecil tetapi bukan teroptimum untuk rangkaian berskala besar. Paket-paket yang dihantar di dalam NoC besar mungkin mempunyai laluan yang panjang untuk sampai ke destinasinya. Ini menyebabkan peningkatan dalam parameter tertentu seperti kependaman dan penggunaan kuasa. Oleh itu, adalah perlu untuk menghasilkan topologi baharu sesuai untuk NoC bersaiz besar. Dalam kajian ini, kami mencadangkan satu topologi rangkaian kos-berkesan untuk NoC bersaiz besar yang memperbaiki prestasi dari segi pendaman hujung-ke-hujung. Topologi yang dinamakan RaMesh, terdiri daripada kelompok rangkaian jejaring. Algoritma penghalaan yang sesuai untuk topologi ini juga dicadangkan. Seni bina RaMesh bersama-sama dengan jejaring dan torus disimulasi menggunakan Noxim (NoC Simulator), C untuk model NoC perisian, dan Altera ModelSim untuk model perkakasan Verilog. Simulasi dilakukan di bawah lalu lintas rangkaian yang berbeza dan untuk aneka saiz rangkaian. Hasil uji kaji menunjukkan prestasi RaMesh lebih baik daripada topologi jejaring-2D setara dan torus. Topologi RaMesh juga ditanda aras dengan topologi jejaring berkelomplok. Kiraan hop purata dalam topologi yang dicadangkan adalah sekurang-kurangnya 22.7% lebih rendah berbanding dengan jejaring dan torus. Kependaman purata juga diturunkan sekurang-kurangnya 24.66% berbanding dengan jejaring dan torus. Akhirnya, titik tepu bagi topologi yang dicadangkan bertambah sekurang-kurangnya 15% berbanding dengan jejaring dan torus.

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LIST OF ABBREVIATIONS

bps	-	Bit per second
BPSF	-	Bypass Forward
BPSR	-	Bypass Reverse
CMP	-	Chip multiprocessors
CPU	-	Central Processing Unit
DNLY	-	Down Layer
DOR	-	Dimension Ordered Routing
DyAD	-	Dynamical Adaptive and Deterministic routing
FPGA	-	Field Programmable Gate Array
FRWD	-	Forward
GAD	-	Global Average Delay
GAT	-	Global Average Throughput
GS	-	Global Switch
HDL	-	Hardware Description Languages
IC	-	Integrated Circuit
IDE	-	integrated development environment
IP	-	Intellectual Property
ISM	-	Interface Switch Master
ISO	-	International Organization for Standardization
ISS	-	Interface Switch Slave
IVC	-	Input Virtual Channel
LS	-	Local Switch
MPSoC	-	Multiprocessor System-on-Chip
NoC	-	Network on Chip
OVC	-	Output Virtual Channel
PE	-	Processor Element
QoS	-	Quality-of-service
RaMesh	-	Ring-based Mesh
ROMM	-	Randomized Oblivious Multi-phase Minimal routing
RTL	-	Register transfer level

RVRS	-	Reverse
SoC	-	System on Chip
UCDB	-	Unified Coverage Database
UPLY	-	Up Layer
VC	-	virtual channel
VHDL	-	VHSIC Hardware Description Language
XML	-	Extensible Markup Language

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CHAPTER 1

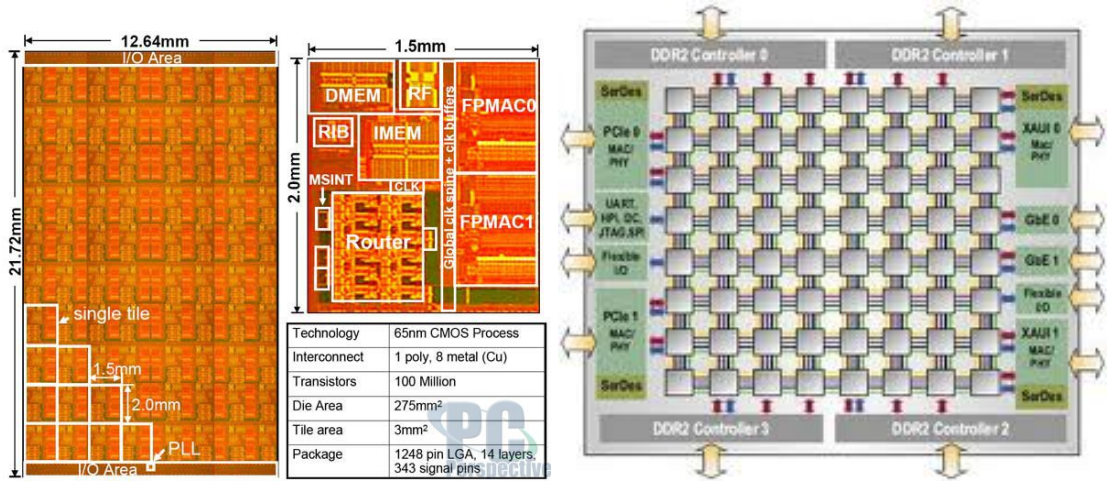
INTRODUCTION

1.1 Network-on-Chip

Multi-processor system-on-chip (MPSoC) is capable of accommodating many processing resources for high-performance computation [12, 13]. On-chip communication is the main bottleneck of MPSoC. Conventional bus-based on-chip interconnect cannot provide efficiency and scalability to connect many cores on one chip. Network-on-chip (NoC) has been proposed to meet on-chip interconnect challenges. NoC consists of interconnected routers based on certain topology (e.g., a mesh), that integrates memories, computational processors or the Intellectual Property (IP) components. The method of communication among IPs within an NoC-based system is through packet transmission via routers instead of circuit switching in bus-based interconnect.

Designing an efficient high performance and low latency NoC is still an open area of research. According to [14, 15], MPSoC size with hundreds or thousands of cores are likely to be common-place today. The increase of on-chip cores requires a high-bandwidth and scalable communication fabric [16, 17]. To satisfy these requirements, NoCs have been presented and has very quickly emerged as the preferred interconnection fabric.

As example, there exists real chips with 80 cores by Intel [1, 18], 100 cores by Tilera [19], and even a research prototype with 1000 cores by University of Glasgow [20]. While increased core count has allowed processor chips to scale without experiencing complexity and power dissipation problems inherent in larger individual cores, challenges still exist. NoC has been utilized to solve this problem. Figure 1.1 shows an example of a 80-core research prototype from Intel [1] (Figure 1.1a) and a commercial 64-core chip for embedded applications from Tilera (Figure 1.1b) that



(a) Intel Teraflops **(b)** Tilera TILE64

Figure 1.1: Examples of multi-core chips with on-chip networks [1, 2]

employs an on chip network for inter-tile communication [2].

1.2 Problem Statement

NoC topology defines how routers are connected together with network endpoints (i.e. IP cores). The performance and cost of NoC are greatly affected by the topology in large-scale MPSoC. Large-scale NoC topology is referred to as the one that has more than 100 IP cores [21]. An NoC topology is characterized by number of hop and network latency [22, 23]. The main issue with a large-scale NoC is the large number of hops that packets have to pass through to reach their final destination, hence creating significant network latency. A large number of hops also has a direct impact on the energy consumed in the interconnect for buffering, transmission, and control.

There are several critical outstanding problems of large-scale NoCs. Due to increasing number of the nodes inside the NoC and also the increase in the transaction between nodes, the rate of data transmission in the links rises. Thus, some links are used more excessively than other links which can lead to difficulty in load balancing inside the NoC. This imbalance makes some packets to take longer paths to reach the destination [24]. The long route results in increase latency, hop count, packet loss and power consumption, and decrease in throughput.

One of the ways to remove the aforementioned problems is to use routing

algorithm. Many routing algorithms were created to solve these problems, but perfect solution is still elusive. The topologies currently used are good for small size networks only. Thus it is necessary to design and develop a new topology which is appropriate for large size NoCs. Besides, an optimized routing algorithm suitable for the suggested topology must be developed. Nychis et al. in [25] have evaluated large NoCs of up to 4,096 cores, and they have shown two important issues with existing topologies in a large-scale NoC, which are high latency and low throughput.

Topologies are increasingly becoming the bottleneck that is limiting the performance of NoC [26, 27]. Indeed, for a large-scale NoC, the topology has a key impact on the performance and cost of the network [5, 7]. It is responsible for 60% to 75% of the miss latency [28].

The classical NoC topology is the two-dimensional mesh [17, 29]. It is preferred over other topologies. Since its simple implementation and the overall layout is very regular [22]. However, in spite of its advantage, the two-dimensional mesh topology is disadvantaged with congestion, high hop count, and high communication latency for large-scale NoC. Indeed, a significant disadvantage of the mesh topology is in its large communication radius which induces long path for packet delivery [7, 30, 24]. For small-scale network (up to 64 nodes [25]), mesh topology is proven to be efficient [23, 7, 25]. However, for large-scale NoC network, the performance of mesh topology degrades significantly [7, 31]. The performance of mesh topology does not scale well with network size.

The torus is also a favored topology for NoCs [32]. There are many long-range links in torus topology that may create problems in terms of performance and cost. A packet that uses a long-range link takes longer time to reach the next hop than when a packet uses a normal link [33]. In addition, each long link imposes a minimum latency and is a potential point of contention [3]. However, long-range links may improve performance by reducing number of hops [3].

Based on aforementioned disadvantages, there is a need to develop a topology with low network latency and hop count [3, 30]. The combination of mesh and ring topology have a potential to address latency and hop count and avoidance of congestion for large-scale networks [7, 8, 34].

1.3 Objective

The main goal of our research is to develop a topology with a suitable routing algorithm for large-scale NoC. The objectives in this thesis are:

- To propose a topology based on mesh clusters that reduces the number of switches, the number of hops, and latency in large-scale NoC. This thesis proposes a new NoC topology called RaMesh. RaMesh is designed based on clusters and it is suitable for large-scale NoCs that have more than 100 IP cores. Each cluster is a mesh topology. However, internal communication between IP cores inside the cluster uses the rule of ring topology. The target performance metric include a low hop count and low average network latency, and congestion avoidance.
- To propose a routing algorithm to cater for the proposed topology. The proposed routing algorithm is a combination of three existing routing algorithms, which are ring, XY, and TRANC [13] to avoid congestion and deadlock problems.

1.4 Scope

The proposed topology is a hierarchical network topology based on mesh clusters suitable for large scale NoCs with more than 100 IP cores. The structure of each cluster is the mesh topology, but the rule of the ring topology is used for internal communication among IP cores.

In this thesis, the proposed topology was evaluated for different NoC sizes, different traffic models, and different traffic ratios. The proposed topology is benchmarked in terms of average hop count and latency with clustered 2D-mesh [8], mesh, and torus under the same experimental conditions.

The proposed topology was implemented using Verilog and simulated using ModelSim. To characterize the proposed topology, we have used random, transpose, hotspot, and uniform distribution traffic models to obtain average hop count and average latency for four sizes of network with 144, 324, 576, and 900 IP cores.

The proposed routing algorithm is based on deterministic routing. We used XY

and TRANC [9] routing algorithms for mesh and torus topology respectively as they are deadlock free. The switching technique for these routing algorithms is wormhole switching.

The hardware evaluation to compare hardware cost (in terms of number of adaptive logic modules (ALM)) and estimate maximum hardware operating frequency was done based on Stratix V 5SEEBF45I4 FPGA using Quartus II software for 144 IP cores. The NoC code was written in C and translated to Verilog HDL and compiled using Quartus II version 13 software. The code was verified using Altera Modelsim. This process is explained in more detail in section 3.4.3.

1.5 Contribution of Study

This thesis proposed a topology called RaMesh, which is suitable for a large-scale NoC. A routing algorithm for RaMesh that minimizes congestion and deadlock is also proposed. The proposed topology is based on mesh clusters, is hierarchical, and has long-range links to help reduce the hop count. The performance of RaMesh is superior in terms of network latency compared to existing topologies such as clustered 2D-mesh, mesh and torus. In summary, the main contributions of this thesis are:

- The proposed NoC topology improves significantly the average hop count compared to clustered 2D-mesh, mesh and torus topologies. For example, RaMesh on average has 42.1% lower hop count compared to clustered 2D-mesh topology in tests done for various network sizes.
- In tests using RTL model for each topology, RaMesh also has superior end-to-end average latency compared to other topologies. Compared to clustered 2D-mesh, mesh, and torus topologies, Ramesh has 31.2%, 49.5%, and 41.5% lower average latency respectively.

1.6 Thesis Outline

The rest of the thesis is organized as follows.

- Chapter 2 contains literature survey on the studies of NoC, which includes topology and routing algorithm.
- Chapter 3 covers the methodology for the work done in this thesis. This also includes the general approach taken for the research done in this work, as well as tools and platform used.
- Chapter 4 presents the evaluation results of mesh topology. We also have simulated the topologies with appropriate routing algorithms under different ratios of traffic pattern.
- Chapter 5 describes the proposed topology that was designed based on hierarchical mesh topology for large-scale NoC called RaMesh. In addition, this chapter also presents a proposed routing algorithm for the proposed topology.
- Chapter 6 presents the results and analysis of the experimentations to compare average latency under different ratios of traffic and different traffic models, and hardware cost.
- Chapter 7 summarizes the thesis, re-stating contributions, and suggest directions for future research.

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