OPTIMIZATION OF N-CHANNEL SILICON NANOWIRE FIELD EFFECT TRANSISTOR USING TAGUCHI METHOD

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A project report submitted in partial fulfilment of the

requirements for the award of the Master of Engineering (Computer and Microelectronic Systems)

Faculty of Electrical Engineering

Universiti Teknologi Malaysia

JANUARY 2018

Dedicated to my beloved husband, Zulhilmi Faiz Bin Yaccob, to my respectful fathers, Wahab Bin Yaacob and Yaccob Bin Jahaja, to my beloved mothers, Noor Bitah Binti Omar and Leha Binti Lontok, and to all my family members who always there for me. Thank You.

ACKNOWLEDGEMENT

In preparing this report, I would like to express my sincere gratitude to Dr. Nurul Ezaila Binti Alias for her advice, guidance, support and encouragement over the period of this work.

My fellow postgraduate students should also be recognized for their support. My sincere appreciation also extends to all my co-workers and others who have aided at various occasions. Their views and tips are useful indeed. Unfortunately, it is not possible to list all of them in this limited space. Lastly, I am grateful to all my family members for their support and encouragement.

ABSTRACT

In the last few decades, the performance of electronics devices, especially the transistors have made tremendous progress thanks to the novel metal-oxide-semiconductor field-effect-transistor (MOSFET) devices structure like Silicon Nanowire FET (SNWFET). As the device is scaled down into nanometer regime, SNWFET is believed could overcome the short channel effects (SCEs). The complexity of SNWFET is influenced by its device geometry such as gate and width size, nanowire shape, nanowire radius, channel orientation, etc. Therefore, the thesis describes the optimization of n-channel SNWFET by using Taguchi method. Taguchi method is straightforward, easy to apply and has fast simulation run time. The dimension of the SNWFET device i.e. gate length (L_g), silicon nanowire radius (R_{nw}) and gate oxide thickness (T_{ox}) are altered for a range of sizes and dimensions by using Taguchi approach to get the most optimum dimensions of the device. The electrical properties of the SNWFET device which are threshold voltage (V_{th}), on/off current ratio ($I_{on}/I_{off}\ ratio$), Subthreshold Swing (SS), and Drain-Induced Barrier Lowering ($DIBL$) are extracted and analyzed based on the I-V characteristics. The general idea of the Taguchi technique is the set of electrical properties are statistically distributed into standard normal distribution and the mean and the standard deviation are determined. From the results obtained, with fixed thin T_{ox} , as the R_{nw} is reduces and L_g is increases, the electrical performance of the SNWFET device is better in terms of its subthreshold swing, switching speed and $DIBL$. Better threshold is observed in n-SNWFET device with smaller R_{nw}. The $I_{on}/I_{off}\ ratio$ also shows better result with longer L_g. Lastly, from the statistical analytic of the device's electrical characteristics, the most optimum device dimensions of n-channel SNWFET device structure has been successfully identified which are R_{nw} at 3nm, T_{ox} at 3nm, and L_g at 40nm with their electrical characteristics of V_{th}, $I_{on}/I_{off}\ ratio$, SS and $DIBL$ are 0.22V, 1.06x10^5, $64.69mV/dec$ and $= 80.27mV/V$ respectively.

ABSTRAK

Dalam beberapa dekad kebelakangan ini, kamajuan alat elektronik telah meningkat dengan mendadak terutama bagi transistor, terima kasih kepada struktur perangkat MOSFET seperti Wayar Nano Silikon Sirip Medan Arutahan Transistor. Apabila saiz transistor dikecilkan, Wayar Nano Silikon Sirip Medan Arutahan Transistor di reka bentuk kerana dipercayai mampu mengatasi efek saluran pendek. Wayar nano silicon dipengaruhi oleh saiz dan lebar gerbang, bentuk wayar nano, laluan orientasi dan sebagainya. Oleh itu, tesis ini menceritakan tentang penambahbaikan laluan-n Wayar Nano Silikon Sirip Medan Arutahan Transistor dengan menggunakan kaedah Taguchi. Kaedah Taguchi sangat mudah diaplikasikankan dan mempunyai tempoh simulasi yang singkat. Panjang gerbang alat elektronik, jejari wayar nano silikon dan ketebalan oksida di ubah untuk mendapatkan optimal dimensi bagi laluan-n Wayar Nano Silikon Sirip Medan Arutahan Transistor. Beza keupayaan halangan, nisbah arus pandu dan arus bocor, sub-ambang cerun dan saluran penghalang akibat penurunan dikaji berdasarkan ciri-ciri IV. Teknik Taguchi adalah daripada himpunan sifat elektrik secara statistik yang diterjemahkan ke dalam taburan piawai. Dari hasil yang diperoleh, dengan kenipisan oksida yang sama, selagi jejari wayar nano berkurang dan gerbang dipanjangkan, prestasi sifat elektrik bagi Wayar Nano Silikon Sirip Medan Arutahan Transistor adalah lebih baik dari segi sub-ambang cerun, kelajuan pertukaran dan saluran penghalang akibat penurunan. Halangan yang lebih baik dilihat dengan jejari wayar nano yang lebih kecil. Perbandingan arus pandu dan arus bocor juga menunjukkan keputusan yang lebih baik dengan gerbang yang lebih panjang. Akhir sekali, berdasarkan analisis statistik, ukuran dimensi yang paling optimal bagi laluan-n Wayar Nano Silikon Sirip Medan Arutahan Transistor adalah 3nm ketebalan oksida, 3nm jejari wayar nano silikon dan 40nm panjang gerbang dengan beza keupayaan halangan, nisbah arus pandu dan arus bocor, cerun sub-ambang dan saluran penghalang akibat penurunan dengan masing-masing sebanyak $0.2222V$, $1.06x10^5$, $64.69mV/dec$ dan $80.27mV/V$.

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LIST OF ABBREVIATIONS

FinFET	-	FIN Field Effect Transistor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
SOI	-	Silicon on Insultaor
GAA	-	Gate-All-Around
SCE	-	Short Channel Effect
TSNWFET	-	Twin Silicon Nanowire Field Efect Transistor
DIBL	-	Drain-Induced Barrier Lowering
TCAD	-	Technology Computer Aided Design
LDD	-	Lightly Doped Drain
ANOVA	-	Analysis of Variance
NTB	-	Nominal the Best Characteristics
LTB	-	Larger the Better Characteristics
STB	-	Smaller the Better Characteristics
CMOS	-	Complementary Metal-Oxide-Semiconductor
SS	-	Substreshold Slope
S/N	-	Signal-to-Noise Ratio
3D	-	Three Dimensional
I_{on}	-	ON current or drive current
I_{off}	-	OFF current or leakage current
V_{th}	-	Threshold Voltage
V_d	-	Drain Voltage
C_i	-	gate dielectrics capacitance per unit area
R_{nw}	-	silicon nanowire radius
T_{ox}	-	gate oxide thickness
I_g	-	Gate Current
W	-	Transistor Width
L_g	-	Transistor Length

V_G	-	Gate Voltage
V_{th}	-	Threshold Voltage
I_D	-	Drain Current
V_{GS}	-	Gate-to-Source Voltage
I_{DS}	-	Drain-to-Source Voltage
max	-	Maximum
t_{Si}	-	Critical Silicon Thickness

LIST OF SYMBOLS

mA/μm	-	milliampere/micrometer
mV/V	-	millivolts per Volts
nm	-	nanometer
mV/dec	-	millivolts per decade
cm^{-3}	-	cubic centimeter
Ω	-	ohm

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CHAPTER 1

INTRODUCTION

1.1 Project Background

Moore's Law stated that the number of transistor in a chip will double up every two years. Therefore, the transistor size is expected to be reduced in order to accommodate the same number of transistors in a same chip. Based on the Figure 1.1, in the year 2020, it is expected to have ten billion transistors in a similar chip size.

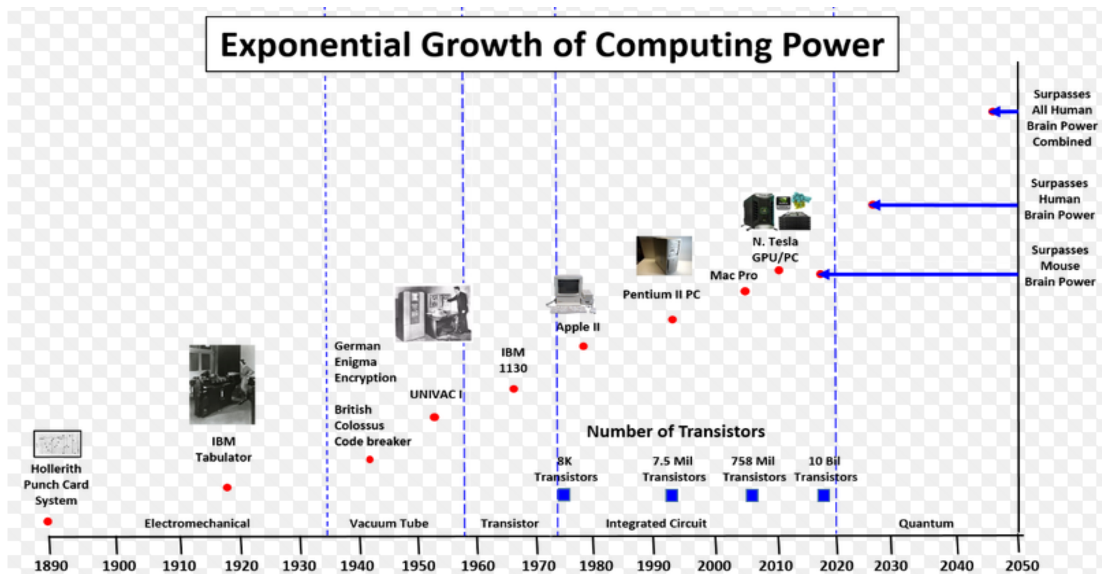

Figure 1.1: The exponential growth of computing power [1].

The reduction of transistor size into nanometer region will cause a problem known as a short channel effect (SCE). The effects can be divided into five which are drain-induced barrier lowering ($DIBL$), surface scattering, velocity saturation, impact

ionization, and hot electron effect. These effects can be distinguished by changing the device structure from planar MOSFET to a novel device.

Basically, there are many MOSFET novel devices like double-gate FinFET, FinFET on SOI, nanowires and twin silicon nanowire FET. All the structures have their own benefits. For silicon nanowire FET, it has a good structure towards SCEs. The cylindrical gate-all-around of silicon nanowire is believed to reduce the leakage current due to an effective gate control of silicon nanowire. Besides that, the GAA silicon nanowire is expected to operate in a fully depletion mode which improves the SCEs immunity.

In addition, there are a lot of optimization method that can be used to optimize the electrical properties of the transistor device. Some of the methods are Stochastic, Taguchi, and Simulated Annealing. Optimization using Taguchi method is carried out at early stage in a design. Therefore, it is believed to give an advantage to the designers. Basically, the purpose of Taguchi method is to identify the parameters or factors that significantly affect a product performance and compute appropriate settings of the parameters at the design level.

1.2 Problem Statement

Since the reduction of channel length causing ~~a~~ short channel effect, a novel structure like Silicon Nanowire FET (SNWFET) is believed to be designed to solve the problem. However, the analysis of silicon nanowire behavior specifically referring to the electrical properties is complex because it is influenced by the size, shape, channel orientation and other effects. Taguchi method is basically a statistical method, particularly by Taguchi's development of device designs for studying variation. A range of device dimensions is varied at the same time contribute to a fast simulation run time and give advantage to designers when compared to a conventional optimization method. Therefore, this research is mainly focuses on optimizing an n-channel SNWFET by using Taguchi method.

1.3 Objectives

According to the problem statement stated earlier, there are three objectives are planned to achieve in this project. The objectives of this project are:

1. To design a n-channel SNWFET by using 3D TCAD tools.
2. To characterize the electrical properties of n-channel SNWFET.
3. To determine the most optimum device dimensions of n-channel SNWFET device structure by using Taguchi approach.

1.4 Scope

This project related to device dimensions optimization using Taguchi method. The optimization is carried out on n-channel SNWFET device. The project covered the software analysis using TCAD tools. All the results will be discussed later.

The first stage of this project involves simulation of the SNWFET using TCAD tools. GAA SNWFET device with Polysilicon gate material will be simulated in order to produce the IV characteristics of device. Then, the electrical properties of the device are extracted based on the IV characteristic. The electrical properties that will be analyzed includes ON and OFF currents ratio ($I_{on}/I_{off}\ ratio$), threshold voltage (V_{th}), subthreshold slope (SS), and drain-induced barrier lowering ($DIBL$).

The second stage of the project involves the geometrical device dimensions optimization using Taguchi method. The Taguchi method will be explored more in the next semester in order to produce the most optimize n-channel SNWFET.

1.5 Thesis Outline

The thesis contains five chapters including an introduction, literature review, research methodology, result and discussion and lastly a conclusion.

Chapter 1 focuses on the background of the project, problem statement, objectives and scope of the project. Based on the project background and problem statement, the objectives of this project are acquired. The project flow is based on the project scope.

Chapter 2 focuses on the literature review. This chapter explains in detail about the project. The review about the project outcome is explained theoretically. Then, the previous related work is referred in order to collect the information related to the project.

Chapter 3 focuses on the method or procedure of the project. The project flow is explained systematically. Then, the project is designed based on the specifications needed.

Chapter 4 focuses on the results incurred. The results will be discussed based on the simulation results. The result will be tabulated in tables analyzed based on the graphs obtained.

Chapter 5 focuses on the conclusion of the project. The achievement of the objectives is based on the results obtained.

1.6 Summary of Work

Figure 1.2 shows the overview of the project. A right procedure is needed to complete the project. This project focuses on the optimization of n-channel silicon nanowire FET (SNWFET) using Taguchi method.

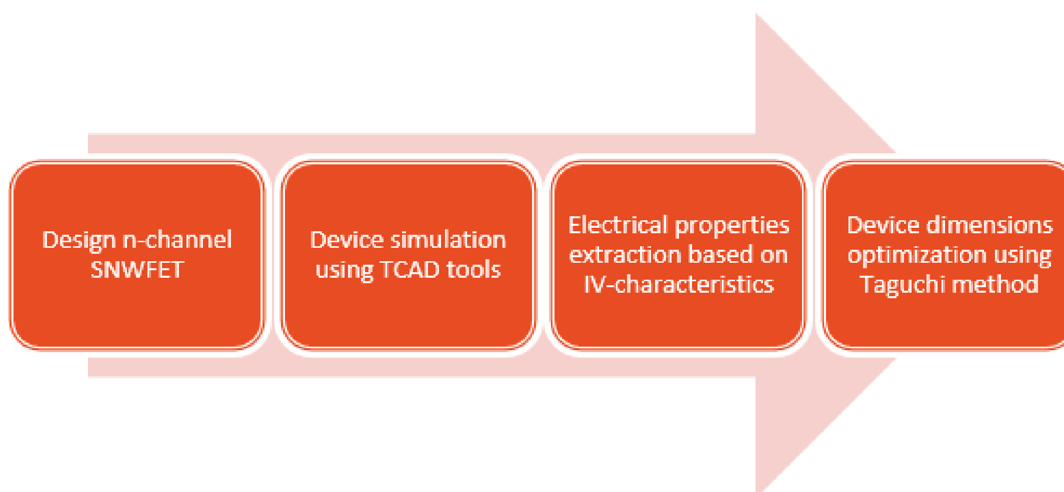

Figure 1.2: The overview of project.

1.7 Project Schedule

The final year project for postgraduate students is almost 1 years. The students are supervised in order to complete the project assigned. The project is assigned and will be evaluates eventually.

The project tasks for a 1 year are arranged every week. All the project works are conducted based on the schedules visualized in Figure 1.3 and planned as in figure 1.4. The tasks are divided into two semesters. The device simulation is covered in the first semester. Then, the project is continued to optimize the electrical properties of the device that will be done in the next semester. After that, the optimize results will be validates with other papers using different optimization method.

Based on the Figure 1.3, the project tasks are arranged for 15 weeks. The project works starting from literature review. Then, the progress of the project is discussed with the supervisor. The meeting held 4 times in the first semester. At the end of the semester, the project proposal is presented to other UTM lecturers for evaluation.

For the second semester, the schedule is illustrated as in Figure 1.4. All the project tasks are a continuation of previous tasks. In the next semester, the Taguchi optimization will be explored in order to simulate the device using TCAD tools. The results will be analyzed. Lastly, the project findings will be presented to the UTM lecturers for evaluation. Then, all the project findings will be recorded for a documentation and future reference.

Week / Task	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Literature Review	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Project Synopsis Preparation							■								
Submission of Project Synopsis								■							
Device simulation using TCAD Tools								■	■	■					
Seminar Material Preparation										■	■				
Submission of Seminar Material											■				
Presentation of Seminar												■			
Report Preparation and Submission												■	■	■	■

Figure 1.3: The project gantt chart for semester I.

Week / Task	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Project Report Writing	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Optimization of n-channel SNWFET using Taguchi method	■	■	■	■	■	■	■	■							
Seminar Material Preparation									■	■	■				
Submission of Seminar Material											■	■			
Presentation of Seminar													■		
Submission of Project Report														■	■

Figure 1.4: The project gantt chart for semester II.

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