DIGITAL LOGIC CIRCUIT DESIGN USING ADIABATIC APPROACH

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To my darling husband and my dear daughter.

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ABSTRACT

A major challenge for the circuit designers nowadays is to meet the demand for low power, especially those used in portable and wearable devices which have limited energy power supply. The reasons of designing low power consumption circuit are to reduce energy usage and minimize dissipation of heat. Adiabatic technique is an attractive approach to obtain power optimization where some of the charge in capacitance can be recycled instead of being dissipated as heat. In this thesis, a methodology for designing sequential adiabatic circuits employing a single-phase power clock was investigated. Initially, methods to simulate dynamic power were analysed by identifying a better and reliable method to simulate adiabatic dynamic power. In addition, a method to validate the output voltage swing was presented. The relationship between voltage swing and power dissipation was analysed. Then, several adiabatic sequential D flip flops (DFF) designs which make use of combinational adiabatic circuit design based on quasi-adiabatic were proposed and suitable types of alternating current power supply which influence dynamic power were analysed and selected. The functionality and performance of the proposed circuits were compared against other adiabatic and traditional Complimentary Metal-Oxide Semiconductor (CMOS) circuits and verified to function up to 1 GHz operating region. Besides the circuits, the layout of the proposed sequential adiabatic design was also produced. All simulations were carried out using 0.25 μm CMOS technology parameters using Tanner Electronic Design Aided and HSPICE tools. The findings showed that the proposed combinational circuit had less transistor count, lower power dissipation with lower voltage swing as compared to reference adiabatic circuits. Furthermore, the proposed sequential DFF circuit showed 25% less power dissipation compared to traditional CMOS.

ABSTRAK

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Cabaran utama bagi pereka bentuk litar pada masa kini adalah untuk memenuhi permintaan reka bentuk yang menggunakan kuasa minimum, terutamanya yang diguna pakai di dalam peranti mudah alih dan boleh pakai yang mempunyai bekalan kuasa bertenaga terhad. Tujuan untuk mereka bentuk litar dengan penggunaan tenaga yang rendah adalah untuk mengurangkan penggunaan tenaga dan pelesapan haba. Teknik adiabatik adalah satu pendekatan yang menarik untuk memperolehi pengoptimuman kuasa yakni sebahagian daripada cas di dalam kapasitor boleh dikitar semula dan bukannya dibebaskan sebagai haba. Dalam tesis ini, metodologi untuk mereka bentuk litar jujukan adiabatik dengan menggunakan bekalan kuasa fasa tunggal telah dikaji. Pertama, kaedah untuk simulasi kuasa dinamik bagi litar adiabatik telah dianalisis untuk mengenal pasti satu kaedah yang lebih baik dan boleh dipercayai untuk simulasi kuasa dinamik bagi litar adiabatik. Selain itu, kaedah untuk mengesahkan ayunan output voltan telah dibentangkan. Hubungan antara ayunan voltan dengan pelesapan kuasa telah dianalisis. Seterusnya, beberapa reka bentuk litar jujukan adiabatik D flip-flop (DFF) yang mengguna pakai reka bentuk litar gabungan adiabatik berdasarkan adiabatik kuasi telah dicadangkan dan jenis bekalan kuasa arus ulang-alik yang sesuai yang mempengaruhi kuasa dinamik telah dianalisis dan dipilih. Fungsi dan prestasi litar yang dicadangkan telah dibandingkan dengan litar adiabatik yang lain dan juga litar Semikonduktor Logam Oksida Pelengkap (CMOS) tradisional yang berupaya beroperasi sehingga 1 GHz. Selain litar, susunan reka bentuk litar jujukan adiabatik yang dicadangkan juga telah dihasilkan. Semua kerja simulasi telah dilakukan dengan menggunakan teknologi 0.25 μm CMOS mengguna pakai alatan Tanner Bantuan Reka Bentuk Elektronik dan HSPICE. Dapatan menunjukkan bahawan litar gabungan yang dicadangkan mempunyai bilangan transistor yang kurang, pelesapan kuasa yang lebih rendah tetapi ayunan voltan yang lebih rendah berbanding litar adiabatik yang dirujuk. Tambahan pula litar jujukan DFF yang dicadangkan menunjukkan 25% pengurangan pelesapan tenaga berbanding dengan reka bentuk CMOS tradisional.

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LIST OF ABBREVIATIONS

2PADCL	-	Two Phase Adiabatic Dynamic CMOS Logic
AC	-	Alternate Current
ADCL	-	Adiabatic Dynamic CMOS Logic
APFAL	-	Asymmetrical Positive Feedback Adiabatic Logic
CAL	-	Clocked Adiabatic Logic
CLK	-	Clock
CX	-	Auxiliary Clock
CMOS	-	Complimentary Metal-Oxide Semiconductor
CPAL	-	Complementary Pass Transistor Adiabatic Logic
DC	-	Direct Current
DFAL	-	Diode Free Adiabatic Logic
DRC	-	Design Check Rule
EACRL	-	Efficient Adiabatic Charge Recovery Logic.
ECRL	-	Efficient Charge Recovery Logic
EDA	-	Electronic Design Aided
EEAL	-	Energy Efficient Adiabatic Logic
LVS	-	Layout Versus Schematic
MECRL	-	Modified Energy Recovery Logic Circuit
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NAND	-	Not AND
NMOS	-	N-Channel MOSFET
NOR	-	Not NOR
PAL	-	Pass-Transistor Adiabatic Logic
PC	-	Power Clock
PFAL	-	Positive Feedback Adiabatic Logic

PMOS	-	P-Channel MOSFET
SAL	-	Subthreshold Adiabatic Logic
SPADL	-	Single Phase Adiabatic Dynamic Logic
SPICE	-	Simulation Program for Integrated Circuits Emphasis
TSEL	-	True Single Phase Energy Recovery Logic
VLSI	-	Very Large Scale Integration
W/L	-	Width to Length

LIST OF SYMBOLS

C	-	Capacitor
C_L	-	Load capacitor
E	-	Energy
$E_{dissipated}$	-	Dissipated energy
E_{sc}	-	Short circuit energy
E_{stored}	-	Stored energy
E_{total}	-	Total energy
f	-	Frequency
f_{in}	-	Input frequency
f_{pc}	-	Power clock frequency
$I_{leakage}$	-	Leakage current
I_{source}	-	Current source
I_D	-	Drain current
In	-	Input
k	-	Kilo
L	-	Length of transistor
L_n	-	Length of NMOS transistor
L_p	-	Length of PMOS transistor
M	-	Mega
m	-	Mili
m	-	Metre
Out	-	Output
P	-	Power
$P_{dynamic}$	-	Dynamic power
$P_{leakage}$	-	Leakage power

$P_{short\text{-}circuit}$	-	Short circuit power
P_{static}	-	Static power
$P_{subthtreshold}$	-	Subthreshold power
P_{total}	-	Total power
R	-	Resistance
T	-	Time
τ	-	Delay
V_{dd}	-	Supply voltage/drain to drain voltage
V_{GS}	-	Gate to source voltage
V_{th}	-	Threshold voltage
V_c	-	Capacitor voltage
V_{tn}	-	Threshold voltage of NMOS transistor
V_P, V_{PC}	-	Power supply
W	-	Width of transistor
W_n	-	Width of NMOS transistor
W_p	-	Width of PMOS transistor
α	-	Switching activity
β	-	Current gain parameter
Ω	-	Ohm
ΔVswing	-	Different between voltage swing
μ	-	Mobility

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

This chapter provides an introduction of this research which includes the background of the study, problem statement and the motivation for this work. The organization of the thesis is also briefly explained in this chapter.

1.1 Background of The Study

The classical approach to obtain low power design are mostly carried out by reducing supply voltage, decreasing loading capacitance and reducing switching activity to a certain extent. During discharging activity in traditional approach design style, the charge is fully thrown away to the ground and this is actually a waste. One alternative design style known as adiabatic, recycles the charge and leads to less power consumption from the power supply. The adiabatic technique uses alternating current (AC) power supply instead of direct current (DC) power supply and some of the adiabatic techniques even use multiple phases of AC power supply.

This research presents issues and challenges of the adiabatic design approach. At the end of this research, 4 combinational adiabatic circuits which are Inverter, NAND, NOR, and decoder are proposed up to 1 GHz and four D-Flip flop (DFF) adiabatic circuits are proposed up to 800 MHz operating frequency with lower power dissipation and powered up by a single power supply

This research project is focussed on transistor-based quasi-adiabatic design because it has lower power dissipation, simple structure, and no floating output which makes it more efficient compared to fully adiabatic design. The project is based on CMOS 0.25 μm process as the baseline of the process technology in this research. Please kindly note, that the technology chosen for this research does not reflect the latest technology as the main scope of this research is to focus on low power digital logic design. The design tools are Tanner EDA and HSPICE for circuit level design and L-EDIT of Tanner EDA for layout design

1.2 Problem Statement

Adiabatic circuit design method has been around since the 1990s [1][2] to reduce dynamic power dissipation that allows charge to be recycled. However, despite reports of its superiority in dynamic power saving over traditional circuit design, not much progress have been made to place its design style in the mainstream of low power design approach. As a result, it is only found in published papers [3]–[18] but not much in actual daily life applications. Adiabatic circuit has 3 main issues which hinder it to revolutionize the circuit design method.

It has been shown that the dynamic power of adiabatic circuits could be reduced if the charging time is extended. The significance of this fact is that power

consumption for the adiabatic circuit is governed by its operating speed. Thus, it is not surprising to note that almost all of the published works on the adiabatic circuit is limited to several MHz speeds of operation and not many of them even achieve 500 MHz. This is certainly too far behind of the present operating frequency of digital circuit which is in the region of several GHz. Although some of the published papers [3], [15]–[18] have claimed to have achieved in GHz range operating region but there is no evident to prove it. Frequency operation could only be proven in transient response and this is not available in those papers. In fact, it is very rare to find papers which claim the circuit could work at high frequency especially higher than 500 MHz and provide the evidence in transient response. As there is no evident offered in those papers, their claims are not taken serious consideration in this report.

The progress in adiabatic sequential circuit design is even more lagging behind the progress of combinational adiabatic circuit. This could be understood as the operation of sequential circuit is very much dependent on its frequency. As the basic cells of sequential circuit are made of combinational circuits, if there is not much progress in the development of combinational circuits, the progress of sequential circuits would be much worst. Thus, it is not a surprise to note that majority of published works concentrated on combinational circuit which leaves sequential circuit far behind.

The first issue of interest in this research is dynamic power measurement method that has never been properly addressed. The traditional approach of dynamic power measurement technique is carried out by introducing a power simulation meter with a dummy voltage controlled current source in parallel with a capacitor and a resistor. However, this dynamic power measurement method was developed for DC supply voltage. As the supply voltage of the adiabatic circuit is in AC mode rather than DC, there is a need to find out whether the traditional measurement method is still valid and useful in the adiabatic approach.

Another issue which could be looked into is the fact that power dissipation, P is highly dependent on the quadratic effect of the voltage, V as in equation (1.1). Where C is the capacitor and f is the operating frequency.

$$P = CV^2f \tag{1.1}$$

Reducing supply voltage is commonly used to reduce power dissipation. However, reducing supply voltage has been proven to cause performance degradation [9], [19]. The voltage swing of a conventional CMOS digital circuit is normally taken as almost equal to the DC supply voltage. As a result, the dynamic power is directly controlled by the supply voltage. Thus, if the voltage swing is made less than the supply voltage, there is a possibility that the dynamic power could be reduced as well. There is still no known research which studies power dissipation of adiabatic circuit with reduction of its voltage swing.

The third issue is that instead of using DC power supply, adiabatic circuit employs AC power supply which is called power clock (PC). Some of the popular options for PC are sine wave, triangular wave, and trapezoidal wave. Multiphase PCs have also been used in the previous work [4], [10], [13], [20]–[24] but they are not attractive due to the complexity and clock skew management problem. There is also no report on attempts to find out which is the best mode of PC to use which leads to reduction in dynamic power dissipation.

In summary, this research aims to study the following questions:

1. If the voltage swing of adiabatic circuit is reduced, would it help to reduce dynamic power dissipation?
2. What would be a reliable method to measure dynamic power in adiabatic circuit?
3. What would be the best mode of PC for adiabatic circuit which helps reduce dynamic power?

1.3 Significance of The Study

Demand for low dynamic power consumption circuit design technique is always on the rise. The majority of published works are mainly concentrated on adiabatic combinational circuit design [3], [5], [7]–[9], [11]–[14] which leave sequential circuit design far behind. This is due to their power consumption is governed by its operating speed. This research took up this challenge that highlights the limitation on the operating frequency of the adiabatic sequential circuit. This research investigated the low power dissipation method by reducing the voltage swing and explored the relationship of power supply frequency and signal input frequencies which have never been reported before. Several DFF adiabatic designs have been proposed in this research which is able to operate with extended operating frequency with lower dynamic power dissipation. Traditional approaches to measure dynamic power was developed for DC supply. This research verified the measurement methods to ensure they are reliable in the adiabatic circuit as well. The issue of adiabatic's mode of PC is still unresolved and design community has yet to agree on one particular choice. This research project awakens the significance of the PC mode used in low power design.

1.4 Contributions

This research work contributes on low power sequential adiabatic circuit design. Specifically, the contributions of the research are as follow:

1. Power meter simulation method has been identified as a reliable method to measure dynamic power in the adiabatic circuit.
2. Adiabatic inverter, NAND, NOR, and decoder are proposed based on reduced voltage swing which can operate up to 1 GHz.
3. Four adiabatic DFF circuits with low dynamic power dissipation are proposed which can operate up to 800 MHz.
4. Triangular PC mode has been identified as the suitable PC in adiabatic circuit.

1.5 Objectives

This research aims to achieve the following objectives:

1. Design basic combinational adiabatic circuits and use them in DFF circuits with operating frequency up to 800 MHz.
2. Determine which is more reliable to measure dynamic power between the power meter method and HSPICE approach.
3. Determine which is more suitable to be employed as a PC between sine wave, triangular wave, and trapezoidal wave.

1.6 Scope of Work

This research aimed to propose DFF circuit using the adiabatic technique based on quasi-adiabatic with extended operating frequency which includes layout design as well. The circuit is aimed to work in 800 MHz frequency region with acceptable voltage swing to ensure it can drive subsequent circuit. Dynamic power simulation method is also within the scope of this work. This project focussed on a single PC rather than multiple PCs. The scope also includes a comparative study to determine which one is better between sine wave, triangular wave, and trapezoidal signal to give lower dynamic power. The project utilized Tanner EDA and HSPICE for circuit level design and L-EDIT of Tanner EDA for layout design.

1.7 Structure of Thesis

This thesis consists of six chapters. Each chapter discusses the detail of the particular topic in order to provide a good understanding of this research work. The rest of the chapters are as follow.

Chapter 2 discusses the literature review of this research includes the challenges, advantages, and disadvantages of the adiabatic method reported in the previous work. This chapter also analyses low power design techniques, power measurement methods, and type of AC PCs that have been used in previous work.

Chapter 3 details the concept and method used to carry out this research from its initial phase until its completion. The detail includes the flow charts, and the tools used, as well as the description of the validation method.

Chapter 4 explains the simulation setup and examines reliable power measurement method specifically for the adiabatic circuit. The simulation setup includes the choice of suitable adiabatic circuit's design parameters.

Chapter 5 presents and discusses the simulation results of combinational and sequential circuits obtained from this research. The discussion is centred around the comparison between the results obtained with the traditional CMOS design and the reference design. The post-layout analysis of the proposed sequential adiabatic design is presented as well.

Chapter 6 provides the conclusion remark on the overall result and suggestion for future work.

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