PERFORMANCE ANALYSIS OF 22NM FINFET-BASED 8T SRAM CELL

NUR HASNIFA BINTI HASAN BASERI

UNIVERSITI TEKNOLOGI MALAYSIA

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NUR HASNIFA BINTI HASAN BASERI

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Faculty of Electrical Engineering

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To my beloved parents and family.

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First and foremost, I praise and thanks to The Almighty Allah SWT for the completion of this report. I would like to express my deepest thanks to Dr. Nurul Ezaila binti Alias for her guidance, consultation and suggestions throughout the project. Not to forget, people who always believe in me and never give up on me, my parents and family, I am grateful to have you guys beside me. To those who always motivate me to complete my master studies, I really appreciate it.

ABSTRACT

As CMOS devices are approaching nanometer regime, there are a lot of consequences found in scaling down CMOS devices such as short channel effects and process variations which affect the reliability and performance of the devices. Researchers have found that FinFET is one of the outstanding nominee to overcome this issue since FinFET has better control over the channel and the lower overall capacitance which will increase the performance of the 6T Static Random Access Memory (SRAM) circuit design. It will help in reducing bitline loading and hence improve SRAM performance. The conventional 6T SRAM cell suffers serious stability degradation issue due to access disturbance at low power mode. The major problem in 6T SRAM is that, when the output voltage reduced below the threshold voltage of the transistor, it will destroy the read operation of the 6T SRAM cell. The noises are easy to destruct the stored-data in the nodes of the 6T SRAM cell due to the direct path between storage nodes and bit lines. To overcome this issue, an 8T SRAM cell has been proposed where the read stability is expected to improve. The purpose of this study is to simulate and evaluate the performance of FinFET-based 6T SRAM and 8T SRAM cell and compare their results. In 8T SRAM, the two additional access transistors eliminate the discharging path from RBL to ground in 6T SRAM cell which in turn help in improving the stability of read operation in 8T SRAM. The stability of SRAM cell is determined by the butterfly curve which is obtained by combining the voltage transfer curve (VTC) of the two cross-coupled inverters of the SRAM cell. GTS Framework TCAD tool is used to design and simulate the FinFET device structure, the schematic and the layout of SRAM cell. From the findings, the FinFET gives better Vth, DIBL, SS and I_{ON} than MOSFET. In addition, 6T and 8T FinFET-based SRAM cell have shown a better stability than 6T and 8T MOSFET-based SRAM cell in retention mode, read mode and write mode. Compared to FinFET-based 6T SRAM cell, FinFET-based 8T SRAM cell improved the read stability by 68.5% and not causing any degradation on the write and retention noise margin.

ABSTRAK

Memandangkan peranti CMOS sedang menghampiri rejim nanometer, peranti CMOS menghadapi kesan saluran pendek dan variasi proses yang menjejaskan kebolehpercayaan dan prestasi peranti. Para penyelidik mendapati FinFET adalah salah satu pengganti terbaik untuk mengatasi masalah ini kerana FinFET mempunyai kawalan yang lebih baik ke atas saluran dan mempunyai kapasitans keseluruhan yang lebih rendah litar 6T SRAM. Ia akan membantu mengurangkan beban bitline dan meningkatkan prestasi SRAM. 6T SRAM sel mengalami masalah kemerosotan kestabilan serius disebabkan gangguan akses pada mod kuasa rendah. Masalah utama dalam SRAM 6T adalah, apabila voltan keluaran dikurangkan di bawah voltan ambang transistor, ia akan memusnahkan operasi bacaan sel SRAM 6T. Bunyi mudah merosakkan data yang tersimpan di nod sel SRAM 6T kerana sambungan yang sama antara nod penyimpanan dan garisan bit. Untuk mengatasi masalah ini, sel SRAM 8T telah dicadangkan di mana kestabilan membaca dijangka bertambah baik. Tujuan kajian ini adalah untuk mensimulasikan dan menilai prestasi sel 8T SRAM berasaskan FinFET dan bandingkan keputusannya. Dalam 8T SRAM, kedua-dua transistor akses tambahan menghapuskan jalan pelepasan dari RBL ke tanah di sel SRAM 6T yang seterusnya membantu dalam meningkatkan kestabilan operasi membaca dalam 8T SRAM. Kestabilan sel SRAM ditentukan oleh lengkung rama-rama yang diperolehi dengan menggabungkan lengkung pemindahan voltan (VTC) daripada dua penyongsang salib digabungkan sel SRAM. Dari penemuan, FinFET memberikan Vth, DIBL, SS dan ION yang lebih baik daripada MOSFET. Di samping itu, 6T dan 8T FinFET SRAM telah menunjukkan kestabilan yang lebih baik daripada 6T dan 8T MOSFET SRAM dalam mod retensi, mod membaca dan mod menulis. Berbanding dengan sel SRT 6T yang berasaskan FinFET, sel SRAM 8T berasaskan FinFET bertambah baik dengan kestabilan membaca sebanyak 68.5% dan tidak menyebabkan sebarang penurunan pada margin bunyi menulis dan pengekalan.

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LIST OF ABBREVIATIONS

CMOS	-	Complementary-metal-oxide-semiconductor
DIBL	-	Drain induced barrier lowering
GTS	-	Global TCAD Solution
IC	-	Integrated circuit
IG	-	Independent-gate
MOSFET	-	Metal-oxide semiconductor field effect transistor
NMOS	-	N-channel MOSFET
PMOS	-	P-channel MOSFET
PTM	-	Predictive technology model
SCE	-	Short channel effect
SG	-	Shorted-gate
SNM	-	Static noise margin
SRAM	-	Static Random Access Memory
SS	-	Subthreshold swing

LIST OF SYMBOLS

H_{fin}	-	Fin height
I_D	-	Drain current
L_g	-	Gate length
T_{fin}	-	Fin thickness
t_{ox}	-	Oxide thickness
V_g	-	Gate voltage
V_{DS}	-	Drain to source voltage

CHAPTER 1

INTRODUCTION

1.1 Project Background

Moore's law predicted that the size of transistor will be reduce by half every two years. As what being predicted by Moore's law, process technology tends to be scaled down continuously. The scaling process allowed more transistors to be packed in a smaller chip area and hence enhance the functionality of SoCs. The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is one of the transistors that is preferable to be used in industry due to its small size, and can be fabricated in a single integrated circuit with millions of numbers. However, the scaling of conventional planar transistor has reached its limit which lead to increase in short channel effects (SCEs) and sensitivity to process variation [1]. SCEs which comprise of drawback dictate on electron drift characteristics in the channel, increase in V_{th} variation, reduction in I_{ON}/I_{OFF} ratio and escalate production of leakage current which causing the scaling of conventional CMOS transistors in 22nm technologies almost futile. The reduction in I_{ON}/I_{OFF} ratio leads to device instability and hence limits subthreshold circuit design. Furthermore, increment in leakage current lead to increasing in static power consumption.

One way to reduce SCEs is by using thinner gate oxide. However, this will increase gate leakage current exponentially due to tunneling. In addition, device reliability will be reduced and the total power consumption will increased. In order to overcome these design challenges, new device structures have been proposed such as silicon-on-insulator (SOl) MOSFET, double gate (DG) MOSFET, SiGe MOSFET, carbon nanotube FET, low temperature CMOS, and even quantum dot device [2] for next-generation technology. Due to compatibility on process variation, SOI and DG are the most preferable among the proposed device structures. Besides that, SOI and DG provide ideal device characteristics under the electrical coupling of two gates [3]. To establish the control on SCE, the front and back gates are electrically coupled to essentially lowering both drain-induced barrier lowering (DIBL) and sub threshold slope (SS). Hence, DG devices are the most preferable candidate to be use in low-power designs due to significant reduction in the standby power while able to maintain better performance. Double-gate CMOS (DGCMOS) offers distinct advantages for scaling to very short gate lengths.

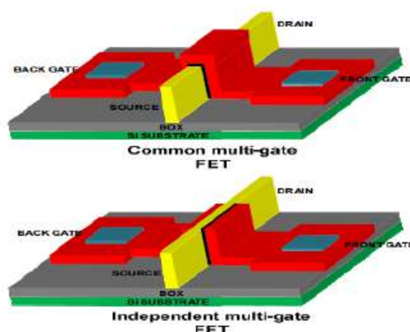

Figure 1.1: SG and IG FinFET structure [4]

There are few types of FinFET used in industry such as Single Gate FinFET and Independent Gate FinFET (Figure 1.1). As what being shown in Figure 1.1, in FinFET, gate is wrapped around channel which help to increase control over the channel. Due to good channel potential control by the double gate structure, it is not

required for FinFET to have high channel dopant concentration in order to suppress the SCE.

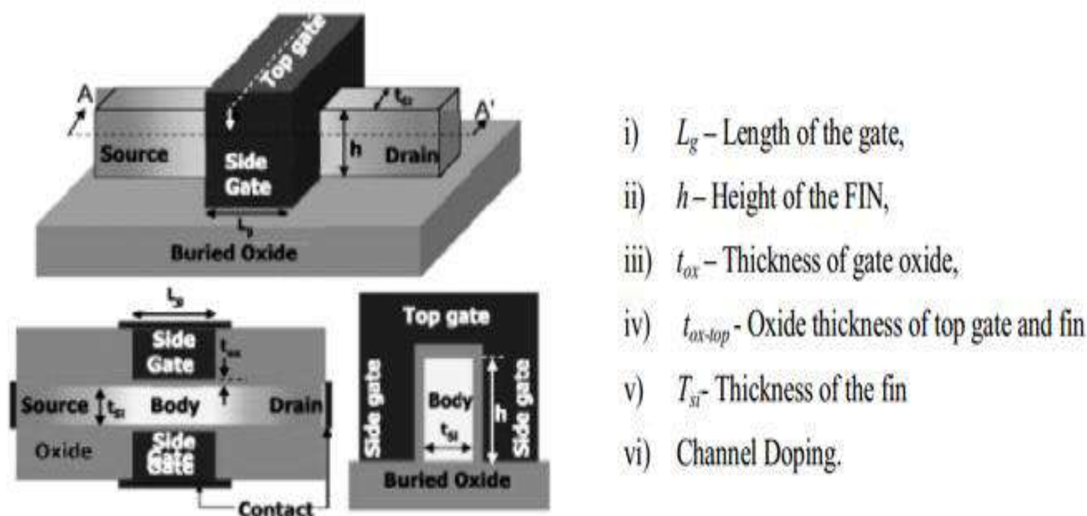

Figure 1. 2 : Parameter use in designing DG FinFET [3].

1.1.1 SRAM cell

SRAM is one of the most prevalent type of embedded memory used in modern SOCs. This is because SRAM provide better compatibility with logic circuits and quick random access compared to other technologies such as DRAM, ROM etc. Figure 1.3 shows the prediction of ITRS on the total memory size and the number of processing engine in a mobile SOC. The graph projected that both the number of processing engine and total memory size will increase by a factor of 18 during 2013-2025 [5]. Huge number of integrated transistors will probably lead to increase in dynamic and static power consumption and shorter in mobile battery life.

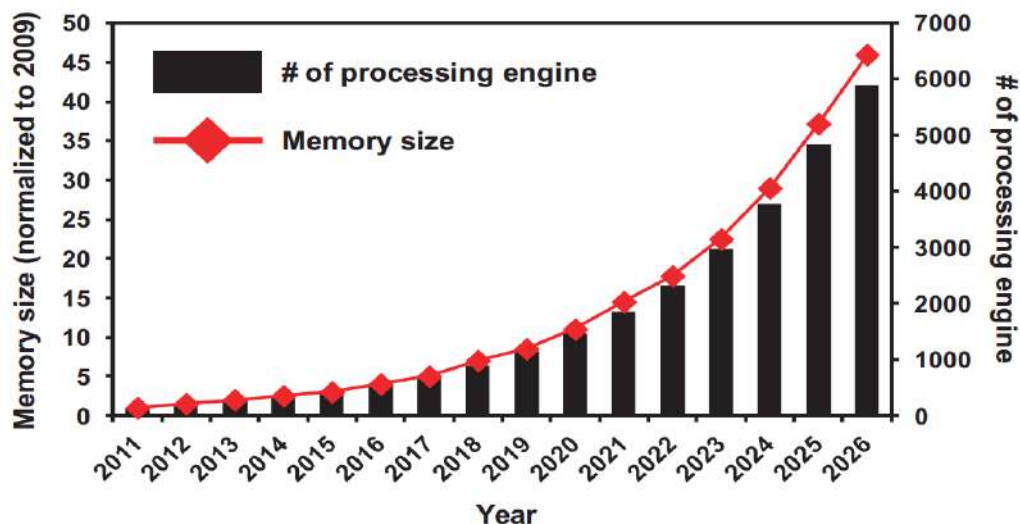

Figure 1. 3: Number of processing engine and overall memory cells trend in mobile SOC as predicted by ITRS 2011 [5].

1.1.2 Theoretical Background of SRAM cell

There are two common types of Random Access Memory (RAM) which are RAM (Static RAM) and DRAM (Dynamic RAM). Due to present of transistor and a capacitor in its structure, data stored in DRAM need to be refreshed regularly. Different from DRAM, data stored in SRAM do not need to refreshment since the cross-coupled transistors in SRAM will hold the data considering that the power supply is not cut off. Due to this, SRAM works at much faster speed in write and read operations [6]. Despite of this advantage, SRAM Array required more area of chip, since more transistors are required to store single bit of data. However, it is worth to sacrifice some area for a better performance [6]. The list of existing the conventional SRAM cells are shown I Figure 1.4 which include 4T, 6T, 7T, 8T and 9T SRAM cells.

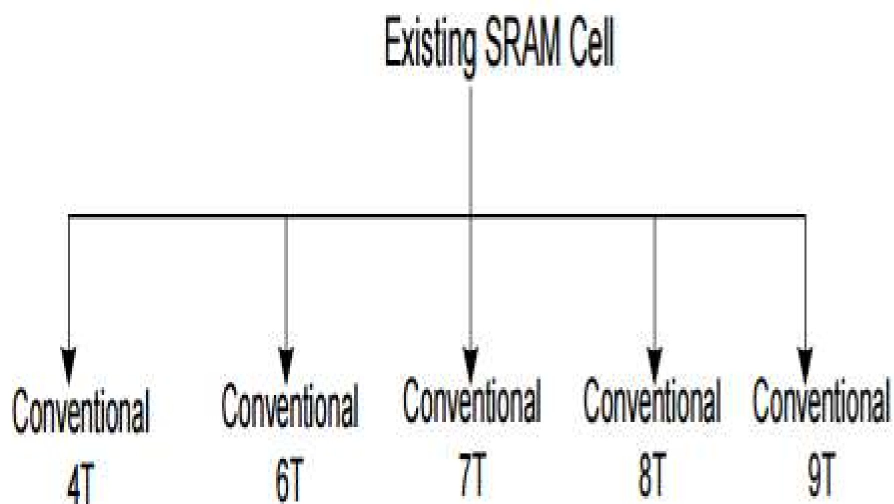

Figure 1. 4: Different types of SRAM cells [6]

The basic structure of SRAM cell is two cross-coupled of inverters that form a positive feedback (see Figure 1.5). The difference between 4T, 6T, 7T, 8T and 9T SRAM cells are the number of access of transistor connected to the two cross-couple inverter [7]. This study will focus more on 6T and 8T SRAM cell. SRAM operates in three modes; retention mode, read mode and write mode.

1.1.3 6T SRAM cell

Figure 1.5 shows the schematic for conventional 6T SRAM cell which consists of PMOS pull up transistors (PU1 and PU2), NMOS pull-down transistors (PD1 and PD2) and NMOS access transistors (AC1 and AC2). Two inverters (PU1, PD1 and PU2, PD2) acts as cross-coupled inverters that form positive feedback which is useful for data storage. Wordlines (WL) and Bitlines (BLs) are aligned in horizontal and vertical directions respectively. During standby mode, BLs are pre-charged to V_{DD} and WL is off. WL line which controls the state of access transistors will only activated during read and write operation. Since both read and write margins need to be take into account, designing 6T SRAM cell is tougher [8]. Besides that, SRAM cell is very much prone to noise during read operation [9].

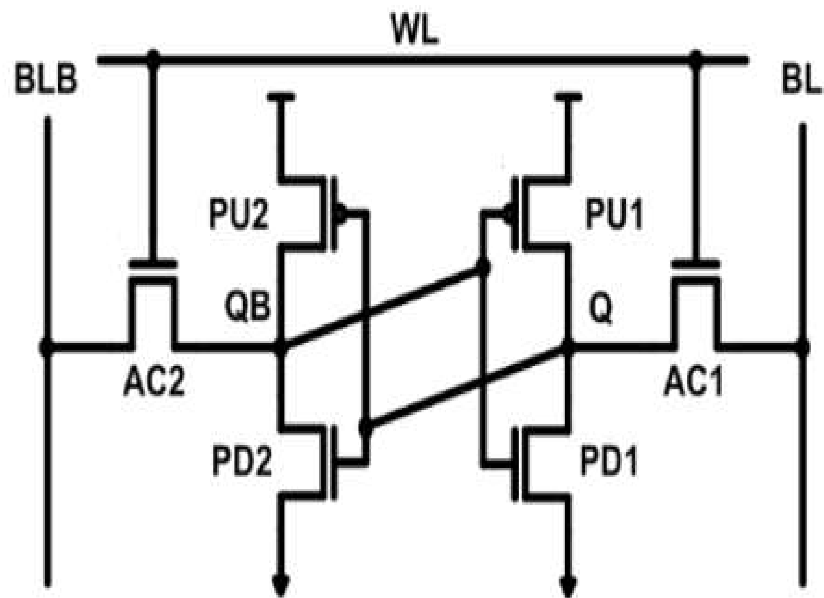

Figure 1. 5: Schematic diagram for 6T SRAM cell.

1.1.4 Operation of SRAM cell

A. Retention Mode

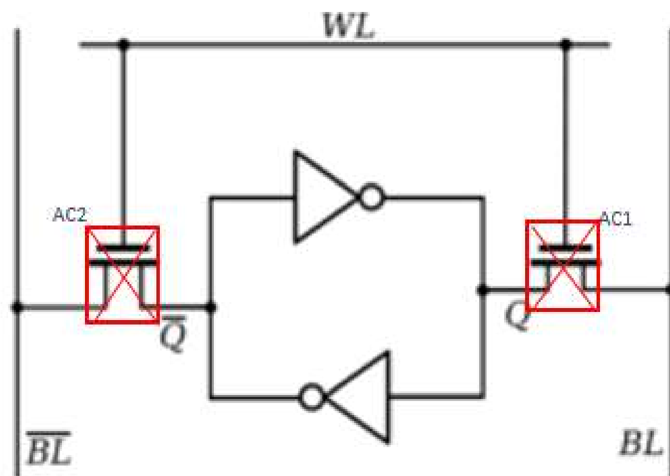

Figure 1. 6: 6T SRAM cell during retention mode

During retention mode, WL is deactivated which causing both AC1 and AC2 to turn off (as shown in Figure 1.6). The two cross coupled inverters form a feedback loop and data will be hold provided that the power is ON.

B. Read Mode

Theoretically, reading only requires the activation of WL and the read operation from SRAM cell state will be done by a single access transistor and a bit line (either BL and AC1 or BL' and AC2). However, in reality that is not the case since bit lines are relatively long and have large parasitic capacitance which in turn makes the read operation slower. Practically, in order to speed up reading operation, a more complex process is applied where both BL and BL' are pre-charge to HIGH. Then WL line will be activated which then causing AC1 and AC2 to turn ON which then causes the voltage at BL to drop slightly (PD is on and PU is off) or rise a bit (PU is on and PD is off). For example, if Q=0, Q'=1, BL discharges through AC1 -> PD1 -> GND and BL' stays HIGH. But Q bumps up slightly (see Figure 1.7). In order for Q not to not flip PD1 >> AC1.

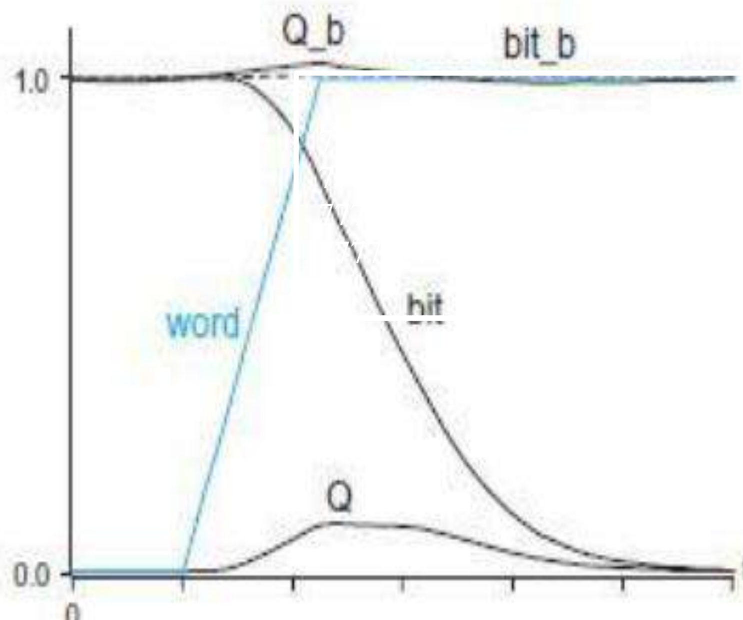

Figure 1.7: 6T SRAM cell during read [10].

C. Write Mode

During write operation, BL and BL' will be drive with necessary values. For instance, if a '0' wish to be written, '0' will be applied to the bit lines and the same approach is applied when we want to write '1'. After that, WL will be activated and bit lines overpower cell with new values. The concept of write operation is identical to the process of applying a reset pulse to SR latch. In order to ensure successful write operation, the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so that the new value can easily override the previous state of the cross-coupled inverters. For example, as shown in Figure 1.8, when Q=0, Q'=1 and BL=1, BL'=0. The value at Q' will be force to LOW and Q to HIGH. To overpower feedback inverter loop, drive strength of AC1 should be stronger than PU1, N2 >> P1.

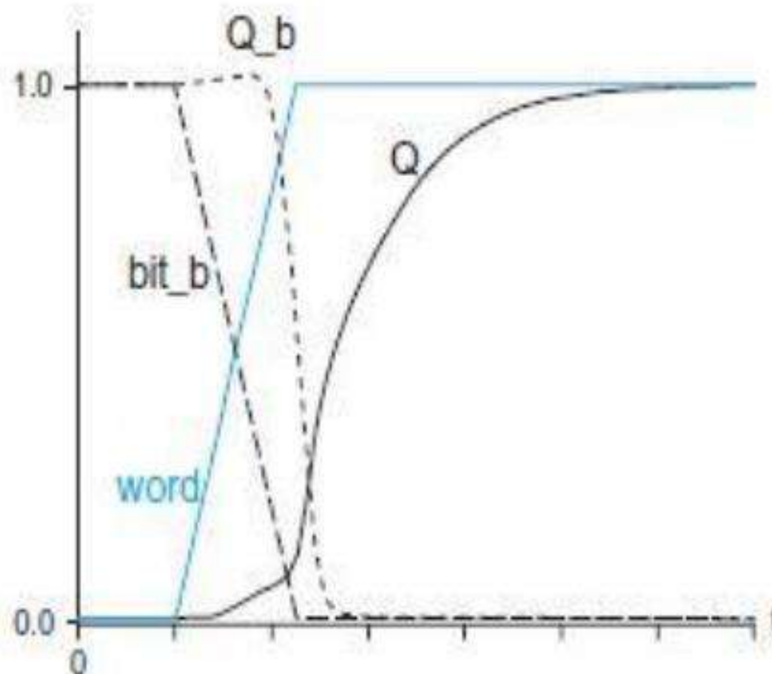

Figure 1. 8: 6T SRAM cell during write [10].

1.1.5 8T SRAM cell

1.1.5.1 Schematic

From Figure 1.9, it can be seen that 8T SRAM cell is made up of conventional 6T SRAM cell and two additional access transistors (RWL and RBL) which form dedicated port for read operation [11] and where the RBL and RWL connection are drawn clearly. The dedicated read ports provide disturb-free read operation and hence help in optimizing both read and write operation.

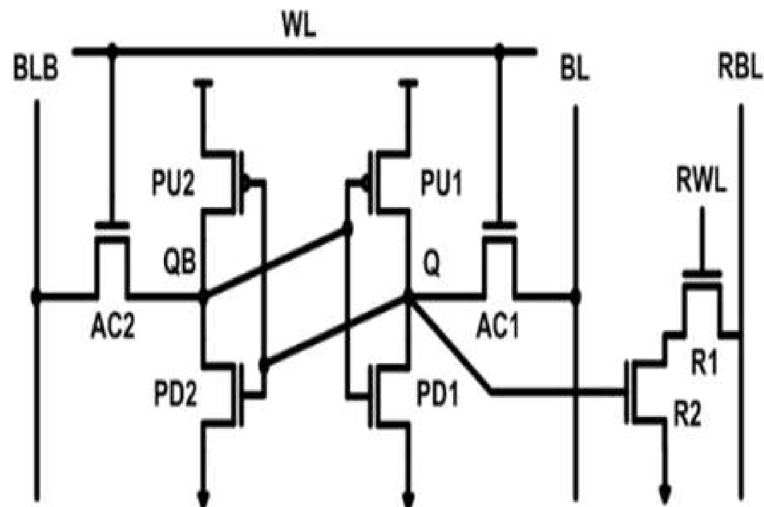

Figure 1. 9: 8T SRAM cell schematic

1.1.5.2 Operation

A. Retention Mode

Retention mode for 8T SRAM cells is similar to the operation of 6T SRAM in retention mode cell where access transistors, AC1 and AC2 are turn OFF and the

dedicated read port, R1 and R2 are also OFF. Data will hold by the two-cross couple inverter considering that the power is ON.

B. Read Mode

Read operation for 8T SRAM cell is entirely decoupled from the write operation by sensing the data through a dedicated read port controlled by an independent read world line (RWL). During read operation, the WL will be set to LOW which will turn OFF access transistors AC1 and AC2. On the other hand, R1 and R2 will be ON. And hence data can be read in from the two-cross couple of inverters.

C. Write Operation

Same as retention mode, write operation for 8T SRAM cell is the same as write operation for 6T SRAM cell since the dedicated read port, R1 and R2 are OFF and hence write operation is independent on those two additional transistors.

1.1.5.3 SRAM Cell Stability

The stability of the SRAM cell represents by Static Noise Margin (SNM). SNM is the maximum static noise that the cell can tolerate, while still maintaining reliable operation [12]. SNM can be determined graphically from a butterfly curve. Butterfly curve represents transfer characteristics of two cross-coupled inverter. For example, in Figure 1.10, the red curve represents the left side of inverter and the green curve represents the right side of inverter. The square area of the butterfly curve represents the stability of SRAM cell. The larger the area, the more stable the SRAM cell is. Unit for SNM is Volt.

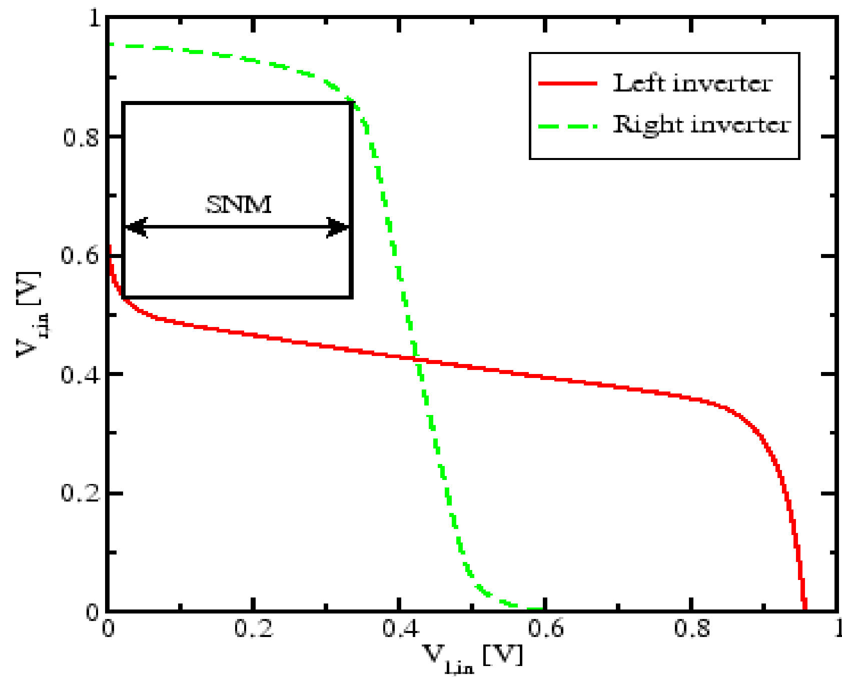

Figure 1. 10: Butterfly curve form by two cross coupled inverters [13].

1.1.6 Static Noise Margin of an SRAM cell

A. Hold Margin

Hold margin is SNM when the cell is at hold mode (holding its state and no read or write operation takes place). During hold operation, the inverters are symmetric. Hence the high and low static noise margins are equal.

B. Read Margin

During read operation, BLs are tight to V_{DD} and the access transistors tends to pull low node to high. This causing the voltage transfer characteristics, VTC to be distorted which then causing read margin to be smaller than hold margin (see Figure 1.11).

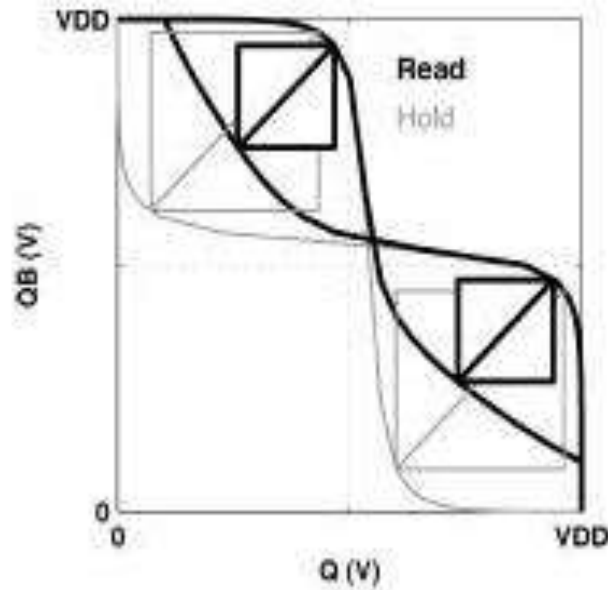

Figure 1.11: Butterfly curve for both read and hold mode [14].

C. Write Margin

During write operation, the cell is imbalanced intentionally. One BL is driven by V_{DD} (same VTC as Read) and another BL is driven to Ground. When the cell is being written, the access transistor must overpower the pull-up transistor to create a single stable state which causing the butterfly curve for write margin is different from read margin (see Figure 1.12).

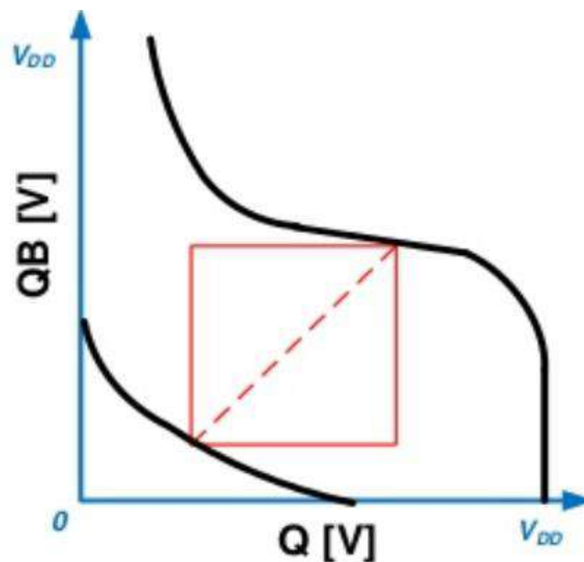

Figure 1.12: Write Margin for Conventional 6T [15].

1.2 Problem Statement

System on chip (SOCs) are comprise of nanoscale devices that are placed in small areas. This causes supply lines and other signals sources in a circuit that produce to give great impact on the operation of the other part of a system. One of the case where noise effect is a great concern is SRAM. This is because SRAM is composed of large number of minimum sized devices that are highly sensitive to noise. One of the main concern in SRAM design is its cell stability. The cell stability determines the sensitivity of the memory to operating conditions and process tolerances. SRAM cell must preserve right operation even in the presence of noise signal. Recent published works have shown that conventional 6T SRAM cell suffer serious stability degradation issue due to access disturbance at low power mode. The major problem in 6T SRAM is that, when the output voltage declined below the threshold voltage of the transistor, it will destroy the read operation of the 6T SRAM cell. The noises are easy to destruct the stored-data in the nodes of the 6T SRAM cell due to the direct path between storage nodes and bit lines. To overcome this issue, an 8T SRAM cell has been proposed where the read stability is expected to improve. In 8T SRAM, the two additional access transistors eliminate the discharging path from RBL to ground in 6T SRAM cell which in turn help in improving the stability of read operation in 8T SRAM.

1.3 Research Objective

The conventional 6T SRAM cell has been widely used nowadays. However due to read stability failures, 8T SRAM cell with FinFET-based is proposed. The objectives of this study are:

i. To design a FinFET-based 8T SRAM cell for 22nm technology.
ii. To analyze the performance of a 22nm FinFET-based 8T SRAM cell in terms of SNM, RSNM and WSNM.
iii. To compare the performance 6T and 8T MOSFET-based and FinFET-based SRAM cells.

1.4 Research Scope

To accomplish the stated objectives, intensive literature review on performance of SRAM cells especially on 6T and 8T SRAM cells are conducted, focusing mainly on the cell stability. Due to two extra access transistors in 8T SRAM, 8T SRAM cell is expected to have better read stability compared to 6T SRAM cell because it has more path to access the cross-couple inverter and the read operation is separated from write opretaion. Besides that, FinFET-based SRAM cell is expected to have better performance than MOSFET-SRAM cell due to the device structure of the FinFET which has better control on the channel. FinFET device will be simulated using GTS Framework Nano-Device and further will be used to design 8T SRAM cell. Then, its performance will be analyzed.

1.5 Thesis Organization

The structure of the report is organized as follows. Chapter 2 describe literature reviews conducted on SRAM cell in the scope of designing and evaluating the performance of SRAM cell and ways on how to improve its performance. Chapter 3 describe the research methodology of this project mainly on the designing and simulating 8T SRAM cell and the overall project flow. Chapter 4 illustrates the result and discussion obtained from this project. Chapter 5 specify the conclusion of this study.

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