THE DESIGN OF AN FPGA-BASED SINUSOIDAL PULSE WIDTH MODULATION GENERATOR

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ABSTRACT

The output of a DC to AC converter circuit is not a pure sine wave. To overcome this problem, a technique called sinusoidal pulse width modulation (SPWM) is used. Generation of SPWM requires a carrier wave and a reference wave. The reference wave is typically a sine wave. Many algorithms have been proposed in the past to optimize the generation of the sine wave but the most suitable scheme uses a lookup table (LUT). In this project the SPWM is implemented using a field programmable gate array (FPGA) where discrete sine values are stored as lookup table in the FPGA. The challenge here is developing an algorithm to minimize the size of the LUT specifically and the FPGA, as a whole. Three SPWM designs are proposed in the project using the VHDL hardware descriptive language. Simulations are done using Mentor Graphic's ModelSim SE 6.4 and the synthesis tool is Altera's Quartus II Web Edition version 9.1. The proposed designs use two approaches, namely, the symmetrical properties of the sine wave to reduce the LUT size and also improvements in the programming codes to reduce the use of logic elements. Each of the proposed synthesized designs uses less than 40% of logic elements compared to the designs from previous works.

ABSTRAK

Keluaran litar penukar arus terus (AT) ke arus ulangalik (AU) bukanlah merupakan suatu gelombang asli sinus. Untuk mengatasi masalah ini, satu kaedah yang dikenali sebagai *sinusoidal pulse width modulation* (SPWM) telah digunakan. Penghasilan SPWM memerlukan gelombang pembawa dan gelombang rujukan. Lazimnya gelombang rujukan adalah merupakan gelombang sinus. Banyak algoritma telah diketengahkan untuk mengoptimakan penghasilan gelombang sinus namun kaedah yang paling sesuai digunakan adalah kaedah *lookup table* (LUT). Di dalam projek ini, implementasi SPWM menggunakan *field programmable gate array* (FPGA) di mana nilai-nilai diskrit sinus disimpan dalam bentuk jadual yang dirujuk. Cabarannya di sini adalah menghasilkan satu algoritma untuk meminimakan saiz LUT khususnya, dan FPGA secara keseluruhannya. Dalam projek ini, tiga rekabentuk SPWM telah diketengahkan mengunakan bahasa perkakasan deskriptif VHDL. Simulasi dilakukan dengan menggunakan ModelSim SE 6.4 Mentor Graphic dan sintesis dilakukan dengan Quartus II Altera versi 9.1 edisi web. Setiap rekabentuk yang diketengahkan menggunakan pendekatan sifat simmetri gelombang sinus bagi meminimakan saiz LUT dan menghalusi teknik kode pemrograman bagi mengurangkan penggunaan elemen logik. Setiap rekabentuk yang diketengahkan ini menggunakan kurang daripada 40% elemen logik berbanding dengan rekabentuk terdahulu.

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CHAPTER 1

INTRODUCTION

1.1 Overview

The use of DC/AC converters in applications such as renewable energy, motor drive control and uninterruptible power supply has become dominant in power electronics conversions. The output produced from the dc/ac converter has two major drawbacks. One is that the output consists of rectangular pulses. Also, the harmonic content is high. Pulse Width Modulation (PWM) is normally employed to overcome these problems (Meng *et al*., 2010). The problem with a DC/AC converter circuit is that since it uses a switching strategy, the output waveform understandably consists of rectangular chunks (Austin and Drury, 2013). A typical output voltage is shown in Figure 1.

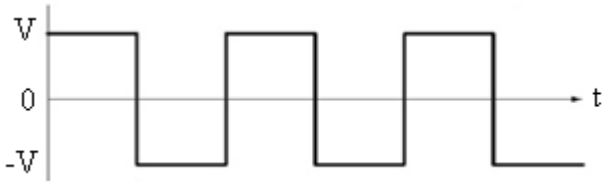

Figure 1.1 Inverter output

Though the rectangular output is adequate for some applications, for most applications, a sinusoidal output is the ideal requirement. Making the output to be as close as possible to a sine wave has also the advantage of reducing the output harmonic content (Barnes, 2003).

The rectangular output can be made closer to a sinusoid by using a scheme based on pulse width modulation (PWM). In this scheme, the on-off periods of the inverter switching devices are determined at certain switching points such that the output will consist of pulses with width varying in a sinusoidal manner.

1.2 Background of the Study

Many PWM techniques have been developed in the past few years. They are designed for applications in high power converters or for particular configurations. For example, selective harmonic elimination (SHEPWM) is used for complete control of voltage over harmonics (Gourisetti and Patangia, 2013; Espinoza *et al*., 2001). The space vector modulation(SVPWM) may be used to reduce switching frequency for a given harmonic frequency (Maha and Faouzi, 2013; Barbi and Batista, 2010).

Carrier techniques have been shown to be efficient in converter systems with multi-module. The most common carrier PWM is the sinusoidal pulse width modulation. (SPWM) (Song and Jones, 1999).

The SPWM generator may be physically realized using various technology but the most popular and preferred implementation uses a field programmable gate array (FPGA). The two most prime advantages for choosing an FPGA include the ability to reprogram and thus redesign the SPWM generator many times within a short period of time and a cheaper design cost (Sudha and Khatir, 2013)

1.3 Problem Statement

Sinusoidal pulse width modulation involves the generation of two interacting waves, namely, a reference wave and a high-frequency carrier wave. The reference wave is typically a sine wave and the carrier wave is normally a triangular wave. The primary concern here is the generation of the sine waveform. Generating sine wave digitally through the use of lookup tables (LUTs) is a well known and widely accepted method due to its simplicity and quick programming (Salazar *et al*., 2011). The LUT method is very fast and suitable for high speed system (Baozhong and Tiequn, 2011).

However, a key issue with using the look-up table method is power consumption, since a digital waveform with a bigger frequency will increase the Read-only-Memory (ROM) size and this may increase the power consumption (Mashayekhi *et al*., 2008; Gan *et al*.,2009; Veredas and Pfleiderer, 2006; Hao Li *et al.*, 2009). Consequently many researches have been conducted that aimed at reducing the ROM size (Meher, 2010; Dickin and Shannon, 2010; Azizi and Najm, 2005).

1.4 Project Questions

This project will attempt to answer the following questions:

i. What is the drawback of using FPGA in SPWM design?
ii. How may FPGA be used to design an SPWM?
iii. How efficient is the design technique proposed in this project?

1.5 Project Aim and Objectives

The aim of the project is to improve on the design of a sinusoidal pulse width modulation (SPWM) generator. The objectives of the project are :

i. To study the inefficient use of resources in the FPGA-based SPWM design.
ii. To design an FPGA-based SPWM.
iii. To evaluate the resource usage of the proposed FPGA-based SPWM design.

1.6 Scope and Limitation

The study uses the VHDL language for the hardware description tool, Mentor Graphic's ModelSim simulator and Altera's Quartus II web edition for design synthesis.. The FPGA device chosen is Altera's Cyclone II FPGA Thus, all the evaluation results obtained will be reflected by and are limited to only a specific device from a particular manufacturer and do not represent other available and more recent devices in term of overall performances. In addition to that, since only one output frequency is considered

(50 Hz), synthesis results of the SPWM design are limited to and cover only one particular frequency.

1.7 Significance of the Study

Most modern AC variable speed drives are based on power electronic switches which can be turned ON and OFF by low power control circuits connected to their control gates. Also, many microcontrollers and digital signal processors (DSPs) are already equipped with on-chip PWM controllers. These two facts make the study of SPWM more relevant. Also, because of the combination of electronic and magnetic components in a switching power supply, computer simulation plays a vital role in creating a successful design. Finally, since the design is FPGA-based, the design has the flexibility to be improved in the future by simply modifying and reprogramming the existing design codes.

1.8 Summary

This chapter discusses on some of the important aspects related to the design of a sinusoidal pulse width modulation generator and the issues involved with the design. Chapter 2 of the project report will discuss on the literature review. Chapter 3 will discuss on the methodology used in the design. Chapter 4 discusses on design and development and chapter 5 discusses on the results and discussions. Finally, the conclusions are covered in chapter 6.

REFERENCES

Meng, K., Gao, M., Bai,Y., and Chen, C. (2010). Analysis of Sine-wave Inverter's Harmonic Contents by Simulation. *2nd International Conference on Mechanical and Electronics Engineering (ICMEE 2010)*. Kyoto: IEEE, 51-58

Hughes, A. and Drury, B. (2013). *Electric Motors and Drives: Fundamentals, Types and Application.* 4th edition: Newnes.

Barnes, M. (2003). *Practical Variable Speed Drives and Power Electronics*. 1st edition: Newnes.

Gourisetti, S. N. G. and Patangia, H. A summary on modified carrier based real-time Selective Harmonic Eliminationt technique. *Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference*. Abu Dhabi, UAE: IEEE, 78-79

Espinoza, J. R., Joos, G., Guzman, J. I. , Moran, L. A., and Burgos, R. P. (2001). Selective harmonic elimination and current/voltage control in current/voltage-source topologies: a unified approach. *Industrial Electronics, IEEE Transactions*. 48(1), 71-81.

Maha, Z. and Faouzi, B. (2013). Implementation of Space Vector modulation using DSP *Electrical Engineering and Software Applications (ICEESA), 2013 International Conference*. Hammamet: IEEE, 1-7.

Barbi, I. and Batista, F. A. B. (2013). Space Vector Modulation for Two-Level Unidirectional PWM Rectifiers. *Power Electronics, IEEE Transactions.* 25(1), 178-187.

Song, Y. H., and Jones, Allan T. (Eds) (1999). *Flexible AC Transmission Systems (FACTS).* IEE Power Series. The Institution of Engineering and Technology.

Sudha, K. And Khatir, I. (2013). Implementation of FPGA Base Controller for Induction Motor Drives. *International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC).* Chennai: IEEE, 37-42.

Salazar, A. J., Bahubalindruno, G., Locharla, G. R., Mendonça, H. S., Alves, J.C., and Machado da Silva, J. (2011). A Study on Look-up Table Based Sine Wave Generation. *REC 2011,VII Jornadas Sobre Sistemas Reconfiguráveis, Faculdade de Engenharia De Universidade do Porto, 3-4 de Fevereiro de 2011*

Baozhong, Xie and Tiequn, Chen (2011). Sine wave algorithm based on 2nd offset and its implementation in FPGA. *10th International Conference on Electronic Measurement Instruments (ICEMI)*. Chengdu: IEEE, 173–176

Mashayekhi, M., Jeddi, Z., and Amini, Z. Power optimization of LUT based FPGA circuits. *Proceeding of: Optimization of Electrical and Electronic Equipment, 2008. OPTIM 2008. 11th International Conference*. Brasov: IEEE, 37-40.

Gan, Ming-gang, Chen, Jie. and Cheng, Lan. (2009). The Design of Direct Digital Frequency Synthesis Based on ROM Lookup Table. *International Conference on Information Engineering and Computer Science, 2009. ICIECS 2009*. Wuhan: IEEE, 1–3.

Veredas, F.-J. and Pfleiderer, H.-J. (2006). Power estimation of a LUT-based MPGA. *Field Programmable Technology, 2006. FPT 2006. IEEE International Conference.* Bangkok: IEEE, 313-316.

Hao Li ; Wai-Kei Mak ; Katkoori, S. (2003). Efficient LUT-based FPGA technology mapping for power minimization. *Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia and South Pacific*: IEEE, *353-358*

Meher, P.K. (2010). LUT Optimization for Memory-Based Computation. *Circuits and Systems II: Express Briefs. IEEE Transactions*. 57(4), 285-289.

Dickin, D. and Shannon, L. (2011). Exploring FPGA technology mapping for fracturable LUT minimization. *Field-Programmable Technology (FPT), 2011 International Conference*. New Delhi: IEEE, 1-8.

Jung, J.H. (2010). Data reduction method of sine look-up tables in microprocessor's memory storage. *Electronics Letters.* 46(25), 1656-1658

Azizi, N. and Najm, F.N. (2005). Look-up table leakage reduction for FPGAs. *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*: IEEE, 187-190

Ahmed, S.Z., Sassatelli, G., Torres, L., Rougé, L.(2010). Survey of New Trends in Industry for Programmable Hardware: FPGAs, MPPAs, MPSoCs, Structured ASICs, eFPGAs and New Wave of Innovation in FPGAs. *International Conference on Field Programmable Logic and Applications (FPL).* Milano: IEEE, 291–297.

Vahid, F. (2006). *Digital Design*. 1st edition. Wiley

Chu, Pong P. (2008). *FPGA Prototyping By VHDL Examples: Xilinx Spartan-3 Version.* 1st edition. New Jersey: John Wiley & Sons, Inc.

Whitaker, J. C. ed. (2005). *The Electronics Handbook.* 2nd edition: CRC Press.

Ahmed, A. (1998). *Power Electronics for Technology.* 1st edition: Prentice Hall.

Lakka,M. and Koutrolis, E. (2014) Development of an FPGA-Based SPWM Generator for High Switching Frequency DC/AC Inverters. *IEEE Transactions on Power Electronics*. 29(1), 356-365.

Yuan,L., Peng, J., and Bin, Z. (2012). The principle and realization of single-phase SPWM wave based on the counter method. *3rd International Conference on System Science, Engineering Design and Manufacturing Informatization*. Chengdu: IEEE, 10-13

Hussin, H., Saparon, A., Muhamad, M. and Risin, M. D. (2010). Sinusoidal Pulse Width Modulation (SPWM) Design and Implementation by Focusing on Reducing Harmonic Content. *2010 Fourth Asia International Conference on Mathematical/Analytical Modelling and Computer Simulation*. Kota Kinabalu, Malaysia: IEEE, 620-623.

Bohrn, M., Fujcik, L., Vrba, R.(2011). Novel on-chip sine wave generator. *34th International Conference on Telecommunications and Signal Processing (TSP).*Budapest: IEEE, 505–508

Sun, F., Wang, H. and Fu, F., Li, X. (2010). Survey of FPGA low power design. *International Conference on Intelligent Control and Information Processing (ICICIP).* 547–550.

Cheng-Shing Wu and An-Yeu Wu. Modified vector rotational CORDIC (MVR-CORDIC) algorithm and architecture. (2001). *IEEE Transactions on Circuits and Systems II Analog and Digital Signal Processing*: IEEE, Volume 48, Issue 6, 548-561.

Kaur, Sukhpreet and Singh, Kulbir (2012). Implementation of High Speed Fixed Point CORDIC Techniques. *International Journal of Computer Applications*. Volume 56, number 3.

Romli, M. S. N., Idris, Z., Saparon, A.(2008). An area-efficient Sinusoidal Pulse Width Modulation (SPWM) technique for Single Phase Matrix Converter (SPMC). *3rd IEEE Conference on Industrial Electronics and Applications, 2008. ICIEA 2008*. Singapore: IEEE, 1163–1168.

Chu, Pong P. (2006). *RTL Hardware Design Using VHDL : Coding for Efficiency, Portability and Scalability*. 1st edition. John Wiley & Sons, Inc.