COMPLEMENTARY METAL OXIDE SEMICONDUCTOR ELECTROCARDIOGRAM AMPLIFIER FOR LOW POWER WEARABLE CARDIAC SCREENING

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To my family members and my fiance

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ABSTRACT

Cardiovascular disease is the number one killer disease in Malaysia. Although sudden cardiac arrest is the main cause of death, the Malaysian awareness of towards cardiovascular disease is still low. The trend of health care screening devices in the world is increasingly towards the favor of portability and wearability, especially in the most common electrocardiogram (ECG) monitoring system. This is because these wearable screening devices are not restricting the patient's freedom and daily activities. While the demand of low power and low cost biomedical system on chip (SoC) is increasing in exponential way, the front end ECG amplifiers are still suffering from flicker noise for low frequency cardiac signal acquisition, 50 Hz power line electromagnetic interference, and the large unstable input offsets due to the electrode-skin interface is not attached properly. In this project, a high performance ECG amplifier that suitable for low power wearable cardiac screening is proposed. The amplifier adopts the highly stable folded cascode topology and later being implemented into RC feedback circuit for low frequency DC offset cancellation. By using 0.13 μm CMOS technology from Silterra, the simulation results show that this front end circuit can achieve a very low input referred noise of 1 $\mathrm{pV}/\sqrt{\mathrm{Hz}}$ and high common mode rejection ratio (CMRR) of 174.05 dB. It also gives voltage gain of 75.45 dB with good power supply rejection ratio (PSSR) of 92.12 dB. The total power consumption is only 3 μW and thus suitable to be implemented with further signal processing and classification back end for low power biomedical SoC.

ABSTRAK

Penyakit kardiovaskular merupakan pembunuh pertama di Malaysia. Meskipun serangan jantung secara tiba-tiba adalah merupakan penyebab utama kematian, namun tahap kesedaran penduduk Malaysia terhadap penyakit kardiovaskular ini masih rendah. Arah aliran terkini peranti pemeriksaan kesihatan dengan tumpuan kepada kebolehan mudah alih dan sedia pakai adalah semakin meningkat di seluruh dunia, terutamanya sistem monitor elektrokardiogram (EKG) yang selalu digunakan. Hal ini kerana peranti pemeriksaan sedia pakai tidak menyekat kebebasan pesakit dan aktiviti seharian. Walaupun permintaan untuk sistem pada cip (SoC) bioperubatan yang rendah kuasa dan murah semakin meningkat secara eksponen, bahagian hadapan penguat EKG masih mengalami masalah gangguan kerlipan pada frekuensi rendah semasa perolehan data isyarat jantung, gangguan elektromagnet daripada 50 Hz talian kuasa, dan ketidakstabilan masukan ofset yang besar disebabkan oleh penyambungan antara muka elektrod dan kulit yang tidak sempurna. Di dalam projek ini, penguat EKG berprestasi tinggi yang sesuai untuk peranti pemeriksaan jantung sedia pakai berkuasa rendah telah dicadangkan. Penguat ini mengadaptasi topologi kaskod terlipat yang mempunyai daya stabil yang tinggi dan kemudian telah digunapakai dalam litar suapbalik RC untuk membatalkan ofset DC pada frekuensi rendah. Dengan menggunakan teknologi CMOS 0.13 μm daripada Silterra, keputusan simulasi menunjukkan bahawa bahagian hadapan litar ini berupaya mencapai tahap gangguan isyarat masukan yang rendah iaitu 1 $\mathrm{pV}/\sqrt{\mathrm{Hz}}$ dan nisbah penolakan mod sepunya (CMRR) yang tinggi iaitu 174.05 dB. Ia juga menghasilkan gandaan voltan sebanyak 75.45 dB dengan nisbah penolakan bekalan kuasa (PSRR) yang baik iaitu 92.12 dB. Jumlah lesapan kuasa adalah cuma sebanyak 3 μW yang mejadikan ia sesuai digunakan bersama bahagian belakang yang memproses dan mengklasifikasi isyarat lanjutan untuk peranti SoC bioperubatan berkuasa rendah.

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LIST OF ABBREVIATIONS

AA	-	Amyloid A
AC	-	Alternating Current
AL	-	Amyloid Light-chain
AgCl	-	Silver Chloride
BSIM4	-	Berkeley Short-channel Insulated Gate Field-Effect Transistor version 4
CMOS	-	Complementary Metal Oxide Semiconductor
CMRR	-	Cool Man Reuse RAM
CVD	-	Cardiovascular Disease
DC	-	Direct Current
ECG	-	Electrocardiogram
EDA	-	Electronics Design Automation
HRV	-	Heart Rate Variability
IoT	-	Internet of Things
LVS	-	Layout Versus Schematic
NMOS	-	N-channel Metal-Oxide-Semiconductor Field-Effect Transistor
PMOS	-	P-channel Metal-Oxide-Semiconductor Field-Effect Transistor
PSRR	-	Power Supply Rejection Ratio
RC	-	Resistance and Capacitance
SoC	-	System on Chip

CHAPTER 1

INTRODUCTION

This thesis presents the ECG signal amplifier design using folded cascode operational amplifier topology. This chapter discusses the overview of the knowledge of the project, problem statement, project objective, scope, and thesis organization respectively.

1.1 Introduction

Cardiovascular disease is the first disease that causes the most death in Malaysia. It is estimated that 36% of the Malaysian is died because of the heart disease [5], making Malaysia ranked at 33 in the world [6]. Having threatened by the cardiovascular disease in among the middle age to old people is very worrying especially when these people are staying alone or have no relatives staying nearby to him or her. While sudden cardiac arrest is the main cause of death due to the sudden stop-functioning of the heart [7], the case is even worst when the patient is staying alone where nobody is aware of the patient's mortality. Although cardiovascular diseases are high mortality; however, Malaysian awareness towards cardiovascular health and disease is low [8].

To reduce the risk of fatality, continuous monitoring of the electrocardiogram (ECG) signal and analyzing the heart rate variability (HRV) is desired for public community for early prevention as well as emergency treatment of serious heart diseases.

The trend and demand in the health care devices is increasing towards more portability as compared to the previous year, especially in this era where the emerging

of internet of things (IoT) is very promising in the near future. Therefore, it is important to make a system that is suitable to be used with the wearable devices and IoT.

1.2 Problem Statement

The cardiovascular disease patient needs to monitor their heart rate continuously in order to detect whether the patient has notifiable arrhythmia or the severe arrhythmia like ventricular fibrillation that causes sudden cardiac death. This monitoring is very crucial especially when the patients have heart attack and ventricular fibrillation background as the sudden cardiac death can happen anytime in the patient within 48 hours after the heart attack [9]. Early advanced life support treatment to the sudden cardiac death patient can save their life. Besides, the increasing number of cardiovascular disease patients and demand of wearable health monitoring system has brought to the demand of complete wearable ECG screening system on chip (SoC).

However, the current one lead low power ECG front end amplifiers are very prone to noisy environment such as 50 Hz powerline magnetic field interference, causing the signal is being interfered with the powerline noise [3, 10–12]. As the heart signal is a low frequency signal, flicker noise at low frequency is also very prominent in the circuit output. Large and unstable input offsets due to impedance between electrodes and skin causes the amplifier to be saturated easily. These noise and offset are not suitable to be used for wearable monitoring system implementation. [3, 11, 12].

Therefore, a redesigned, low powered, and high performance circuit device and hardware systems are required in order to realize the single-chip portable ECG monitoring system.

1.3 Objective and Scope

As the low power ECG front end amplifier problem is highly related to the noisy environment and low frequency noise, therefore the objective of this project is to design an low power, high common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and low noise one lead ECG signal amplifier by using 0.13 µm CMOS process technology.

This design will be made compatible with other in house digital system design for the wearable ECG monitoring and interpreting system.

1.4 Scope

The scope of this project is limited to only the amplifier design, while not considering other backend components such as signal filter, analog to digital converter, and digital processing system. Folded cascode amplifier will be used as the reference design for the ECG signal amplifier due to its low noise benefit. The technology node used for this project is BSIM4 0.13 µm CMOS transistor process technology. The tool being used for the circuit design will be Cadence. Figure 1.1 shows the scope of this project, which is highlighted in green colour.

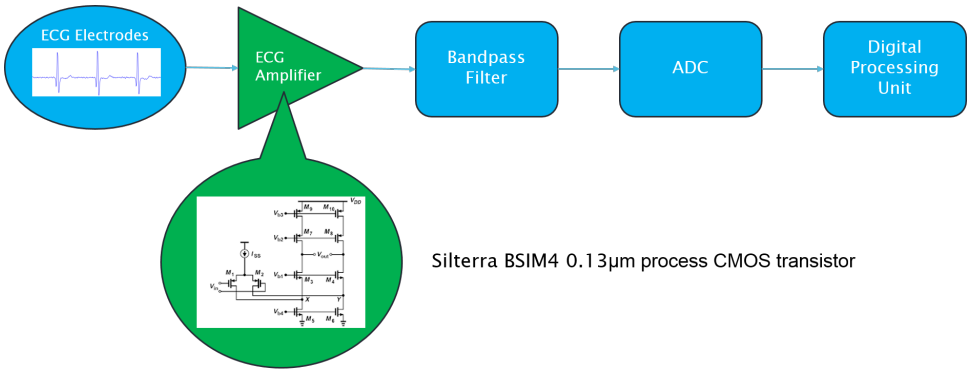

Figure 1.1: Project Scope

1.5 Organization

The content of this report is organized into a total of five chapters. The first chapter consists of the background and information of this project, the problem statement, project objectives and the project scope. Chapter 2 consists of the literature review which includes the discussion of the background and the works from other researchers that are related to this project. The Chapter 3 is discussing about the

methodology that is the method, hardware, tools, software and the design algorithms that are used to develop this project. While the Chapter 4 is discussing about the project design simulated result and output. The last chapter which is Chapter 5 will be talking about the conclusion and future works that are required to further enhance the current design.

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