# Study on Threshold Voltage Shifts and Reliability in PFETs by High-Voltage ON-State and OFF-State Stress

(オンおよびオフ状態高電圧ストレスによる PFET のしきい値電圧シフトと信頼性に関する研究)

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# Abstract

In recent decades, electronics have made much progress thanks to the scaling of silicon complementary metal-oxide-semiconductor (CMOS) very-large-scale integration (VLSI). Now, dimensions of state-of-the-art metal-oxide-semiconductor field effect transistors (MOSFETs) are as small as tens of nanometers. The size of MOSFETs in VLSI has been rapidly scaled down for more than forty years for higher performance, lower power consumption, and higher integration. In such aggressively scaled MOSFETs, the short-channel effects (SCEs) and variability have large impact on the behavior of devices, and other problems are arising.

It is well known that the random variability of transistor characteristics is caused by the statistical nature of dopant atoms in the transistor channel which is called as random dopant fluctuation (RDF). The number and position of impurity atoms in the channel depletion layer in determining the threshold voltage of the transistor are randomly distributed. It is well known that the variability of transistor characteristics is one of the most critical challenges in VLSI. In particular, the instability in static random-access memory (SRAM) cells due to the variability of individual transistors in the cells is a serious problem that prevents further device integration and supply voltage lowering. Therefore, the analysis of cell unbalances at the transistor level, which leads to a severe yield loss of SRAM is needed for better understanding of SRAM stability at low $V_{DD}$ operation.

Recently, a new concept of post-fabrication self-improvement technique of SRAM cell stability has been demonstrated. The self-improvement scheme in SRAM is used to improve cell stability after chip fabrication. This technique is simply applying stress voltage to the $V_{DD}$ node, when $V_{DD}$ is raised to high voltage, stronger pFET is stressed by ON-state stress, and

$|V_{th}|$ is increased and selectively weakened by self-improvement scheme indicating self-improvement mechanism works. On the other hand, the weaker pFET is stressed by OFF-state stress, and $|V_{th}|$ is decreased and selectively strengthened by self-improvement scheme which is favorable for self-improvement technique. As a result SRAM cell stability is self-improved.

In this work, experimental study on $|V_{th}|$ shifts (the difference between $|V_{th}|$ before stress and after stress) and reliability in pFETs by high voltage ON-state and OFF-state stress have been intensively done. Variability of $|V_{th}|$ shifts ($\Delta|V_{th}|$) in pFETs by high voltage ON-state and OFF-state stress for post-fabrication SRAM cell stability self-improvement technique has been experimentally investigated. It is found that sigma $\Delta|V_{th}|$ and mean $\Delta|V_{th}|$ have universal dependence. Large $\Delta|V_{th}|$ is better for self-improvement scheme, however, the sigma $\Delta|V_{th}|$ increases as $\Delta|V_{th}|$ increases. The magnitude of $|V_{th}|$ shifts in pFETs by high voltage ON-state and OFF-state stress are also very important because it varies for different transistors. Some of the transistors has large $|V_{th}|$ shift and some has small $|V_{th}|$ shift. Experimental results show that $|V_{th}|$ shifts in pFETs by high voltage ON-state and OFF-state stress are strongly dependent on process technology and transistor size.

Recovery behaviors of $|V_{th}|$ shifts in pFETs by high voltage ON-state and OFF-state stress for SRAM self-improvement technique are an important issue. After stress application, $|V_{th}|$ shifted, however, after some relaxation time, $|V_{th}|$ shift tend to move back to its initial state. Therefore, how much $|V_{th}|$ shift is recover and how much remains (become permanent part) have been thoroughly discussed in this dissertation. After stress removal, there is a sudden recovery in a very short time. From long-time recovery measurements, it is found that the permanent part ($\Delta|V_{th}|$) certainly exists even after 2 to 3 months relaxation period. It is newly found that $|V_{th}|$ shifts in pFETs by high voltage ON-state and OFF-state stress for SRAM cell

stability self-improvement technique has no critical recovery issue.

One of the major concerns in SRAM self-improvement technique is the reliability issue. The transistors particularly pFETs are stressed by high voltage, and therefore, the reliability may be degraded. Hence, the reliability measurements of pFETs under the post-fabrication SRAM self-improvement technique have been performed. Negative Bias Temperature Instability (NBTI) degradation and NBTI lifetime estimation of pFETs under this technique are compared with fresh pFETs. It is found that although the NBTI lifetime of pFETs is slightly shortened by the application of self-improvement technique, the lifetime difference is just a little, indicating the self-improvement scheme has no critical reliability issues.

In conclusion, the experimental study on $|V_{th}|$ shifts in pFETs by ON-state and OFF-state stress for SRAM cell stability self-improvement scheme has been performed and their origins have been investigated through this study. The experimental results that have been obtained in this dissertation show important information on the $|V_{th}|$ shifts and their variability behaviors in pFETs by high voltage ON-state and OFF-state stress for post-fabrication SRAM cell stability self-improvement scheme. It is found that the reliability of pFETs under this technique has no critical issues. This is an important step for the realization of this self-improvement technique. Post-fabrication technique will be essential in improving degraded yield of future large-scale SRAM with increased transistor variability.

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# Contents

# Chapter 1

# Introduction

## 1.1 Background

For more than three decades, microelectronic industry has benefited enormously from the metal-oxide-semiconductor field effect transistors (MOSFETs) miniaturization. The shrinking of transistors to nanometer regime allows millions of single transistors in one single chip. The "scaling" of MOSFETs, which are the fundamental elements of silicon complementally-MOS (CMOS) large-scale-integration (LSI), has realized such a significant advance. As MOSFETs are scaled down, the performance and integration density of CMOS LSIs increase, and the power consumption and manufacturing cost per transistor decrease.

In 1965, Moore predicted exponential increase in the integration density of large-scale-integration (LSI), which is well known as "Moore's Law" [1, 2]. Moore's law has been understood differently in different phases of the semiconductor technology industry's development. The general formulation that has been accepted is "the number of components per chip doubles every 18 months". The scaling of CMOS LSIs has continued for more than 40 years with a great deal of effort, as Moore predicted. LSI performance is improved due to scaled down MOSFET because when MOSFET size becomes smaller, number of transistors in one chip is increased. Besides, the scaling rule has been accepted as a principal guideline for the device scaling. R. H. Dennard *et al.* presented their pioneering research work on the scaling rule of MOSFET devices [3]. The basic principle is in order to increase the performance of a MOSFET, the size of the transistor must be linearly reduce, together with

the supply voltage, and increase the doping concentration in a way which keeps constant electric field in the device [3]. When MOSET is scaling down for higher integration and higher performance for decades, the conventional silicon, the basic element in VLSI circuit, approaches its scaling limit. Despite achieving this great progress until now, it is clear that there is a physical limit at the end of scaling and we can not shrink the device size forever.

One strategy for overcoming the limitations of current VLSI technology is to introduce novel devices with new structure and operation principle different from conventional devices and whose performance is enhanced in a smaller dimension, that is to say, which has the higher scaling potential. With the help of "nanotechnology", which has attracted worldwide extensive attention for recent years, a lot of promising new-principle devices are proposed to aid the further performance enhancement. Nanotechnology has the ability to manipulate matter at the molecular and atomic level. Nanotechnology deals with developing materials, devices and other structures processing at one dimensional sized from 1 to 100 nanometers. So far, various kinds of ultra-small materials such as silicon, compound semiconductors, nano-carbon, organic materials, biomedical materials, etc. have been utilized in nanotechnology.

Among all the issues which arise to handicap the continuous device scaling, two issues are with most great importance, one is the short channel effect (SCE), and the other is the variability. To curb the short channel effect, devices with multiple gates have been developed to improve the gate-channel controllability for better electrical characteristics with the progress in nano-scale fabrication technology. In the past decade, performance has progressed through introduction of transistor architecture innovations. In 2002, 50 nm transistors with strained silicon channels were successfully introduced [4]. In 2007, 45 nm transistors with high-k/metal-gate technologies were successfully demonstrated [5].

Now, the gate length of MOSFETs in most advanced CMOS LSIs is as small as 30 nm [6]. Aggressive scaling has realized an excellent integration density and performance of today's CMOS LSIs. In addition, novel channel structures are now being introduced, including ultra-thin-body MOSFETs with 22 nm technology node [7] and FinFETs with 22 nm process technology [6]. In this work, 40 nm and 65 nm nodes pFETs are used for experimental studies.

Advance technology scaling has led to a significant increase in process variability caused by random dopant fluctuations, imperfections in lithographic patterning of small devices, and some other related effects [2]. The threshold voltage ($V_{th}$) variability considerably degrades the stability of integrated circuits [8-13]. In particular, some of the SRAM fails due to cell unbalance caused by transistor variability of individual transistors in the cells which is known as a serious problem that will prevent further device integration and supply voltage lowering [14-18]. It is now very important to take this variability into consideration in circuit design to maintain a high yield.

Recently, a new concept of post-fabrication self-improvement technique of SRAM cell stability has been demonstrated [19-21]. In this technique, high stress voltage is simply applied to the $V_{DD}$ terminal of SRAM cell array. The ON-state stress is selectively applied to the stronger pFETs resulting in $|V_{th}|$ increase, while the OFF-state stress is selectively applied to the weaker pFETs resulting in $|V_{th}|$ decrease. As a result, cell stability is automatically improved [21].

However, there are some other major concerns in this technique which are the variability, recovery and reliability issues after SRAM self-improvement stress application. In SRAM self-improvement scheme, both nFET and pFET are being stressed by high voltage. However, nFET's shift is very small (not shown in this dissertation) compared to pFET and can be

negligible. pFET is stressed by high stress voltage, and therefore, the reliability may be degraded. This work is concerning on the pFETs' reliability due to its major shifts by high stress voltage after the self-improvement stress application. The variability dependence on the pFETs' size should be experimentally studied to investigate the variability behavior for the possibility of further variability suppression. These measurement data will provide clear device design guidelines for the post-fabrication self-improvement scheme of SRAM cell stability.

## 1.2 Objectives

The objective of this work to find out the best stress conditions of pFETs for SRAM self-improvement scheme in terms of threshold voltage shifts and their variability, recovery and reliability issues. Specifically, the objectives of this work are divided into following parts.

1. To clarify the relationship between $|V_{th}|$ shift and variability in pFETs by systematic measurements of high voltage stress application.
2. To clarify the origins of transistor size dependence of $|V_{th}|$ shifts and variability behaviors in pFETs.
3. To clarify the mechanisms of the recovery behaviors in pFETs after high voltage stress.
4. To clarify the mechanisms of reliability in pFETs after high voltage stress.

## 1.3 Chapter Organizations

In chapter 2, post-fabrication SRAM self-improvement scheme and its operational principle were reviewed. The self-improvement technique utilizes nonvolatile $V_{th}$ shift by high voltage stress. In chapter 3, the variability of $|V_{th}|$ shifts in pFETs by high voltage ON-state and OFF-state stress for post-fabrication SRAM self-improvement scheme is

experimentally investigated. To be specific, the stress techniques, stress voltage and stress time dependences of the variability of $|V_{th}|$ shifts are discussed. In chapter 4, the process technology and transistor size dependences of the $|V_{th}|$ shifts and variability in pFETs by high-voltage ON-state and OFF-state stress are experimentally investigated. To be specific, the gate length (L) and gate width (W) dependences of $|V_{th}|$ shifts in pFETs under high voltage ON-state and OFF-state stress are experimentally investigated. Their variability dependence of L and W of pFETs before and after stress is discussed. In chapter 5, the recovery behaviors of pFETs by high voltage ON-state and OFF-state stress are experimentally investigated. The contour plots of permanent and recoverable parts of $|V_{th}|$ shifts after high voltage ON-state and OFF-state stress are determined. In chapter 6, the NBTI reliability of pFETs under SRAM self-improvement scheme is experimentally investigated. NBTI degradation and NBTI lifetime estimation of pFETs under self-improvement scheme are compared with fresh pFETs. Finally, in chapter 7, the conclusion of this thesis is discussed.

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