ARITHMETIC LOGIC UNIT DESIGN FOR SILICON NANOWIRE FIELD-EFFECT TRANSISTORS LOGIC

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Specially dedicated to my beloved family,

siblings and friends for their

love and sacrifice.

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ABSTRACT

As dimensions of conventional planar metal-oxide-semiconductor field effect transistor (MOSFET) are reduced, it cause a lot challenging issue such as short-channel effects (SCEs), scaling of gate oxide thickness and increase power consumption. Multigate such as double gate, tri-gate, surrounding gate and FinFET has been studied as potential structure to replace MOSFET. Thus this research report will describes the simulation and characterization of surrounded gate Silicon Nanowires Transistor (Si NWT). The cylindrical Gate-all around (GAA) Si NWT has showed robustness against SCE, ideal sub threshold swing, suppresses corner effect and suitable for low power devices. From this study simulation had proven that GAA Si NWT provides the best short channel device performance. Also highlighted in this research studies, to achieve symmetrical current in PMOS and NMOS, different number of nanowires channel is selected. Therefore by choosing large number of nanowires channel for PMOS transistor can help compensated the low value of hole mobility. In this work, 2:3 ratios of NMOS and PMOS channel of inverter had used as benchmark for ALU designed. Using the circuit modeling HSPICE, performance for Arithmetic Logic Unit (ALU) circuit in 30nm technology is analyzed with Silicon Nanowire (Si NW) compared with conventional planar MOSFET. The assessment of this circuit logic performance metric includes propagation delay, power-delay-product (PDP) and energy-delay-product (EDP) of full adder, XOR, AND and OR gate forming the ALU block. Moreover, ALU is built with less transistor count to implement Boolean expressions which help to reduced average power consumption, and delay.

ABSTRAK

Pengecillan saiz dimensi *Metal-oxide-semiconductor field effect transistor* (MOSFET) menyebabkan banyak isu yang mencabar seperti *Short Channel effect* (SCE), *scalling of gate oxide thickness* dan peningkatan penggunaan kuasa. Antara alternatif lain bagi mengantikan struktur MOSFET adalah *Multigate* transistor seperti *double gate, tri-gate, surrounding gate* dan FinFET. Melalui laporan penyelidikan ini, akan menerangkan simulasi dan pencirian *Silicon Nanowire Transistor* (Si NWT). Silinder *Gate-all around* bagi Si NWT menunjukkan pretasi penambah baik terhadap SCE, *sub-threshold swing, corner effect* dan sesuai untuk peranti kuasa rendah. Ditonjolkan juga dalam kajian penyelidikan ini, bagi mencapai semetri arus PMOS dan NMOS, bilangan saluran nanowires berbeza dipilih bagi menambahan pengaliran arus. Dalam project ini, 2:3 nisbah NMOS dan PMOS dalam *inverter gate* digunakan sebagai rujukaan dalam mengahasilkan ALU litar. Dengan mengunakan model simulasi HSPICE, prestasi bagi ALU litar dalam teknologi 30nm telah dianalisi dengan mengunakan Si NW model dan dibandingkan pretasi MOSFET model sedia ada. Penambah Penuh yang berasaskan Si NW telah menunjukkan pengurangan yang besar dari segi kelewatan, kuasa yang dilepaskan dan PDP jika dibandingkan dengan MOSFET dan memberikan kelebihan kepada Si NW dari segi kecekapan tenaga. Selain itu didalam project ini, pengurangan transistor didalam ALU litar telah dihasilkan bagi pengahasilan ungkapan Boolean yang tepat bagi membantu mengurangkan penggunaan kuasa purata, dan kelewatan didalam sebuah litar ALU.

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LIST OF ABBREVIATIONS

ALU	-	Arithmetic Logic Unit
BJT	-	Bipolar Junction Transistor
CMOS	-	Complementary Metal-Oxide-Semiconductor
CPU	-	Center Processing Unit
DIBL	-	Drain Induced Barrier Lowering
EDP	-	Energy Delay Product
FET	-	Field-Effect Transistor
GAA	-	Gate-all Around
GIDL	-	Gate Drain leakage
IC	-	Integrated Circuit
ITRS	-	International Technology Roadmaps
INV	-	Inverter gate
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
IV	-	Current –Voltage characteristic graph
NMOS	-	N-Channel Mosfet
PDP	-	Power Delay Product
PMOS	-	P-Channel Mosfet
SCE	-	Short Channel Effect
Si	-	Silicon
Si NW	-	Silicon Nanowire
Si NWT	-	Silicon Nanowire Transistor
Si NWFET	-	Silicon Nanowire Field-Effect Transistors
SiO_2	-	Silicon Dioxide
SS	-	Subthreshold Swing

CHAPTER 1

INTRODUCTION

1.1 Research Background

Integrated Circuit (IC) technology has been observed as one of the most important inventions in engineering history. With an incredible progress in IC technology since 1971, there were about 2,300 transistors with a size of 10 micrometres (10,000 nanometres) on a 12 square millimetres chip. Till today, the 3rd generation Intel Corei7 has 1.4 billion transistors with the size of 22 nanometres, on a 160 square millimetres chip.

With reduction of transistors sizes, more things could be built on a chip and it can increases the processing power of the center processing unit (CPU) by having more processor cores with higher clock frequency and more data cache space. As a result the processor could run faster on more than one thing at the same time, and could store more information.

Thus with a new trend in IC technology, Moore's Law today is not showing any sign of slowing down, but they are showing signs of changing by looking consideration on scaling down the dimension of each transistor in the basic element of integrated circuits and the increasing the total numbers of transistors in one chip.

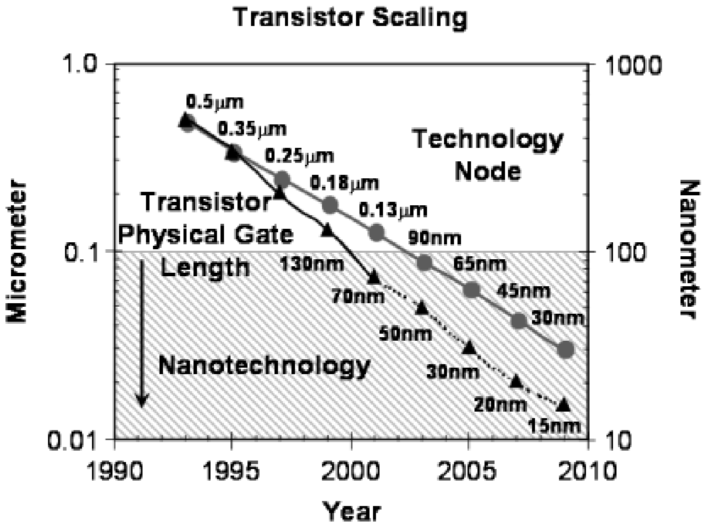


Figure 1.1 Scaling of transistor size (physical gate length) with technology node to sustain Moore's Law. Nodes with feature size less than 100 nm can be referred to as nanotechnology. [1]

As technologies are scaled down in deep sub-half micron regime as shown in Figure1, the conventional bulk metal-oxide-semiconductor field-effect transistor (MOSFET) faces several challenges like higher drain induced barrier lowering (DIBL), poor subthreshold swing collectively known as short channel effects (SCEs) [2]. Moreover, the gate oxide thickness is seems impossible to further scale down beyond the inter-atomic distance as it will increase the gate leakage current.

To sustain scaling transistor for the next decade, the innovation of the transistor must be in the area of a new material (such as as GaAs, High k dielectric and strained silicon channel) or a new transistor structure which will improved the device performance by giving faster speed, higher mobility and low power consumption. One of the most promising new transistor structure solutions from ITRS roadmap has been proposed by using Multi-gate MOSFET architecture including Double-Gate (DG), Pi-FET, Fin Field-Effect Transistors (FinFETs) and rectangular or cylindrical Gate-all around (GAA) nanowire MOSFETs as shown in Figure 1.2 below.

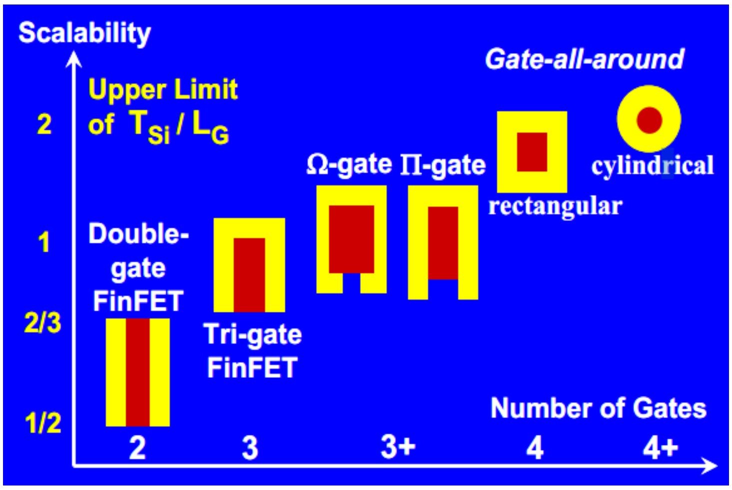


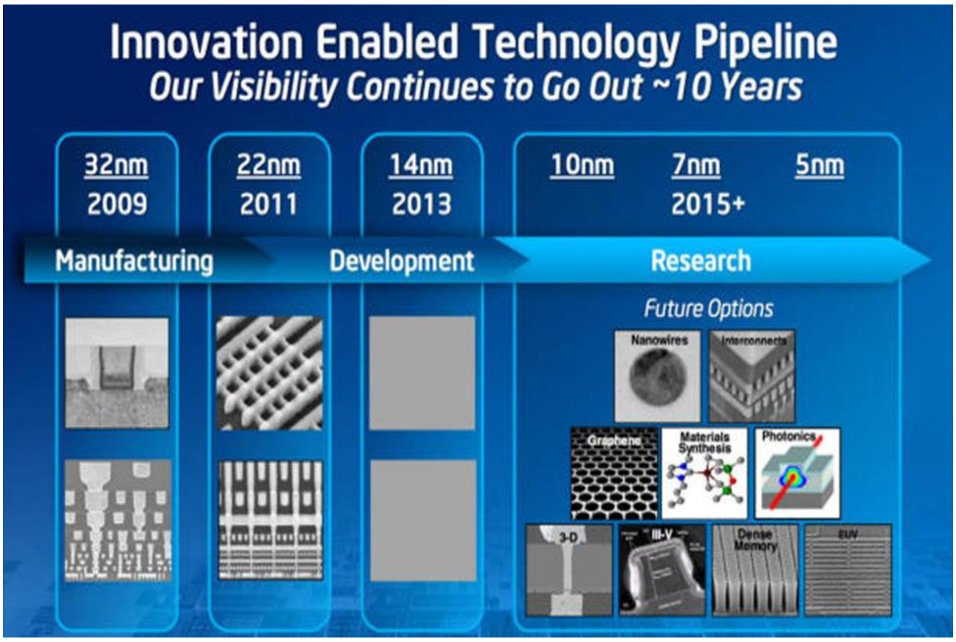
Figure 1.2 Next generation of extended Moore Law's [1]

Among those new silicon structures, GAA Silicon Nanowire Transistor (Si NWT) has emerged as promising device for nano-scale circuits because of the improved electrostatic control of the channel via the gate voltage and the consequent suppression of short-channel effects. Another big advantage from GAA structure is that the silicon channel thickness can be equal to the gate length (1x or 2xL_G) rather than about 2/3xL_G in double Fin FET [3]. So continues with shrinking of feature size, the channel thickness can be reduced till nanowires like geometry. As a result, the silicon nanowires transistor has obtained broad attention from both the semiconductor industry [4]. According to director of advanced device technology at Intel’s Hillsboro, Ore, Kelin Kuhn, also had agreed that GAA gate structures have some key advantage as it expected to provide the best gate control for very short channels [5].

On the other hand using silicon nanowire in designing in Integrated circuits can be effective approach for higher speed and lower power consumption which increase the whole microprocessor system. Hence this project will focuses on using silicon nanowire field effect transistor as a most promising device in electronic technology for designing ALU. The reason behind choosing ALU as a research work is that, ALU is the key element of digital processors like as microprocessors, microcontrollers, central processing unit etc. Every digital domain based technology depends upon the operations performed by ALU either partially or whole. That’s why it highly required designing high speed ALU, which can enhance the efficiency of those modules which lies upon the operations performed by ALU [6].

1.2 Problem Statements

The breaking down of Moore’s law has been predicted the dead end since 2010 as computer power simply cannot maintain its rapid exponential rise using standard silicon technology. The downscaling of the feature size in CMOS technology had made conventional CMOS transistor model is facing severe challenges for scaling beyond 22nm nodes [7].



Innovation Enabled Technology Pipeline

Our Visibility Continues to Go Out ~10 Years

32nm 2009 | 22nm 2011 | 14nm 2013 | 10nm 7nm 5nm 2015+

Manufacturing | Development | Research

Future Options

Figure 1.3 Intel’s future development plan showing a trend in size reduction [8]

Therefore, the conventional devices' modelling is no longer accurate when the channel lengths reach beyond 22 nanometre scale due to the numerous unknown parameters. There are much work has also been done by researcher to investigate the scope of various multi-gate structures. One of the most promising candidates is GAA Silicon Nanowire Transistor (Si NWT) because of process compatibility with complementary metal-oxide-semiconductor (CMOS) technology and also because of its small off-leakage current and high on-current.

On the other hand, nowadays ALU design in digital IC that has low power consumption, high speed and energy efficient is in highly demand. As a result the use of convention transistor i.e. MOSFET in ALU circuit design has also spotted reaching it performance limit such as average power dissipation and speed as the sizes reaches nanometres scale. One of new structure alternative to solve the problem proposed by Technology Roadmap of Semiconductor (ITRS) is Si nanowires FET to replace conventional transistor MOSFET.

Therefore in this project, the performance if GAA Si NWT in digital system namely ALU circuit is explorer. This can be achieved by investigating the physical of Silicon nanowires as compared with MOSFET. Hence the problems in this project are:

1. How does the performance of silicon Nanowires Field effect on Bulk wafer?
2. How Gate-All-Around Si NW characteristic design for CMOS Inverter?
3. What is the maximum number of Si NW channel can be replaced to obtain the optimum performance of the device?
4. What are the performance differences in logic circuit such as ALU using GAA Si NWT as compared with MOSFET

1.3 Objectives

The project focuses on to develop and analysed the GAA Silicon Nanowire (NW) vs traditional convention MOSFET which is based on 30nm process technology. Thus the objectives of this project are:

1. To build circuit and simulate using HSPICE based on GAA Si NWT.
2. To obtain symmetrical output IV characteristic GAA Si NWT with number of channel variation between N and P type.
3. To optimize the ALU circuit with the smaller number of transistor count.

1.4 Research Scope

There are few research scopes that are highlighted in this project. This research scope cover analysed and developed the Cylindrical Si NWT (GAA) and MOSFET which is based on 30nm process technology. First, the Si NWT characteristic is obtained from IV curve with different number of channel N and P type by choosing CMOS inverter as the test vehicle. The transistor model that been use through this project is from BSIM-CMG model. Once the drive current for N and PMOS transistor are matched using different number of channel for each and excellent performance of the inverter is achieved from GAA Si NWT model, then the ALU circuit is applied in SPICE code where the code will be simulated in HSPICE and the graph will be plotted in CosmoScope and Matlab. This project will analyse on performance of Si NWT ALU using 30nm Berkeley Short-channel IGFET Model-Common Multi-Gate (BSIM CMG) model against 30nm conventional MOSFET model. The important metric performances such as power delay product (PDP) and energy delay product (EDP) will be obtained.

1.5 Contribution

GAA Si NWT structure is a new alternative solution for conventional MOSFET as identified by The International Technology Roadmap for Semiconductor (ITRS), would give great advantages over the conventional CMOS. This project successfully reveals few items as show below:

1. Achieved different number of channel for each N and P type of Si NW in logic gate. A symmetry in NMOS and PMOS current is achieved by using 2 channel wire N-type and 3 channel wires for Ptype of GAA nanowires CMOS inverters as benchmark.
2. Design the ALU using ripple carrier adder (RCA) structure with 2-1 multiplexer connected in parallel in order to maintain the speed of the circuit. Optimize the transistor count in the logic gate to improve the performance by using 2-1 AND-OR-Invert Logic (AOI) Gate and one NOR without any INV.
3. Achieved better performance ALU with Si NW as compare to Benchmark MOSFET in propagation delay, power and efficiency of the circuit.

1.6 Thesis Outline

This Project consists of five chapters. The first chapter provides an introduction to this research including the objective and fields of study. The theories and fundamental about relevant research are discussed in the second chapter. Additional information related to this project are taking from journal or other research as references to understand the physical silicon nanowire transistor and manufacturing process. Apart from that, the results from other research thesis, User's Manual and datasheet are obtained. In the third chapter, research and method are recorded and explained in details can be explained in detail. Chapter 4 will provide the conclusion and the future work can be expand in the project.

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