

OPTIMUM LOCATION AND ALLOCATION OF FAULT CURRENT LIMITER IN
DISTRIBUTION POWER SYSTEM USING Y-BUS MATRIX

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This research specially dedicated to both my beloved mother and father
for their support and encouragement,
also to my supervisor Prof. Dr. Ir. Mohd Wazir Bin Mustafa,
my family members and all my friends.

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ABSTRACT

The fault monitoring system is a serious part as one of the components that give the negative impact to the system. The fault needs to identify the magnitude of the nominal current, this magnitude is more than five (5) times greater than nominal current. If this happened on the system, it will cause the disaster on the Power System itself, either, system failure or, system damage. The FCL can be applied to the system for maintaining the circuit breaker operates within their limits/ratings. The Y-Bus Matrix has been implemented to analyse the optimal location of FCL for limit the fault current. This Y-Bus Matrix is identify for each buses declared as a Point of Common Coupling. Different location of fault impedance will be resulting the different location of FCL. Two categories of simulation has been used, Matlab Simulation and Y-Bus Matrix Simulation Technique as an additional support instrumentation. This project discover that FCL should be located in series at high admittance value. The analyses are verified by simulation result.

ABSTRAK

Sistem pemantauan lebih arus adalah merupakan satu perkara penting yang memberikan kesan negatif kepada sesuatu sistem. Lebih arus perlu dikenalpasti dari segi nilai arus sebenar, arus ini merupakan lebih 5 kali ganda daripada nilai arus sebenar. Jika perkara sedemikian berlaku dalam sesuatu sistem, ia akan menyebabkan bencana kepada sistem kuasa tersebut, sama ada, sistem mengalami terputus bekalan atas kemusnahan sistem tersebut. Penghad Arus Kerosakan (*FCL*) diperkenalkan kepada sistem untuk menyokong kepada pemutus litar supaya beroperasi pada kadar yang ditetapkan. Matrik Bas digunakan sebagai kaedah analisa untuk mendapatkan lokasi yang sesuai bagi kedudukan *FCL* untuk mengurangkan kadar lebih arus. Matrik Bas ini dikenalpasti pada kedudukan setiap palang bas yang diishtiharkan sebagai kedudukan asas. Dengan perbezaan kedudukan bebanan yang mempunyai lebih arus, ianya akan memberi keputusan yang berbeza-beza dari segi kedudukan *FCL*. Dua keadaan simulasi digunapakai, Simulasi *Matlab* dan Simulasi Y-Bas sebagai kaedah tambahan. Projek ini adalah menerangkan bahawa kedudukan *FCL* adalah bersesuaian pada keadaan sesiri dengan nilai Lepasan yang tertinggi. Analisa dapat dibuktikan melalui keputusan yang diperolehi.

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LIST OF ABBREVIATIONS

TNB	-	Tenaga Nasional Berhad
FCL	-	Fault Current Limiter
GA	-	Genetic Algorithm

CHAPTER 1

INTRODUCTION

1.1 Introduction

By the capacity usage of power system increases, that influence the increasing number of fault [8]. As a result, the short circuit current will be flowing in power system and some cases, it might be exceeded the circuit breaker rating, and finally damage the system equipment itself [6]. Today, the Fault Current Limiter (FCL) is very important for power system to ensure the system operated in safe condition, which can minimize the nominal fault current while the circuit breaker system operated within the setting limits.

The FCL is one of the cheaper solution that can contribute to for minimize the nominal of the fault current level where the replacement of the switch gear protection is not feasible [9]. FCL is connected in series to the Circuit Breaker to limit current under fault condition [6].

Depending on the location of installation, FCL could offer the additional advantages such as, i) increasing the interconnection of energy sources; ii) increasing

the capacity of energy carrying on the system itself; iii) reducing the sagging voltage caused by fault impedance; iv) improving the system stability; and v) improving the system security and reliability [6].

For the FCL has been decided, the fault current impedance is easy to identify and calculate using the Ohm's law equation. But, in a large power system, it could be difficult to determine the optimal number, location and FCL parameters during abnormal condition [6].

The FCL can be located at generator feeders, load feeders and inter-bus tie cables to limit the fault current under fault condition [8]. This give the benefit effect to circuit breaker to ensure the nominal current do not exceed the rating of circuit breaker.

The optimal locations of FCL depends on the structure of the power system and other aspects such as, location of fault impedance, the method applied to solve the issue needed. Here we focus on the method used to identify the optimum location and allocation of FCL for minimizing the fault current.

In that case, this project will propose the method to identify the suitable location of FCL and achieve the minimum nominal fault current value. This method will contribute many advantages especially to ensure the system stable and the electrical equipment operated in safe during the fault event.

1.2 Problem Statement

Not all of the equipment is easy to change, either during upgrading or during replacement of old system to the new system, i.e. transformer in vault, underground cable and etc. The one of most direct application of Fault Current Limiter at the main

buses, the large transformer can be used to meet the increasing of demand without any breaker upgrades. Thus, the simple technique needed in order to protect the TNB's equipment during the fault occurs on the selected system in TNB Johor Bahru.

Several ways of designing the method for locate the Fault Current Limiter has been discussed in the past. Some method used, such as Genetic Algorithm to solve the problem, a few steps of the Genetic Algorithm has presented [6]. The steps involved are; (i) Coding; (ii) Initialization; (iii) Evaluation; (iv) Crossover; and (v) Mutation. By the optimal placement of FCL, the FCL adjust the distribution of fault currents in matrix structures to keep the nominal fault current under the interrupting of circuit breaker [8]. The proper method needs to clarify the suitable location of Fault Current Limiter using Y-Bus Matrix.

The triggering current limit is arranged to ensure the switch quick opening under fault condition. It is depend on the storing a small charge to trip the main conductor [9]. This triggering current must be managed properly to support the breaker open. It is because, the circuit breaker do not open when the fault current under the Fault Current Limiter operated not exceed the current setting to operate the circuit breaker. The Y-Bus Matrix is the method used to minimize the fault current under abnormal condition.

In addition, further study is needed to analyse the location and allocation of Fault Current Limiter for minimizing the fault current under fault condition using this method.

1.3 Objective

The main objective of this project is to propose a method for optimize location of FCL and further objective are as follow:

- a) To minimize the nominal fault current value before the circuit breaker system operated.
- b) To develop the Y-Bus Matrix for monitoring system of fault.

1.4 Scope of Project

The limitation of this project is covered the 11kV voltage at Johor Bahru Distribution area, selected feeder. It is involved the 10 substations whereas it is connected in parallel to the 11kV source voltage. The source of voltage is taking from the 132/11 kV Main Intake Substation (PMU) Kangkar Tebrau. The system operation for this project is focusing on the radial circuit. The location of FCL is located in series to all substation and the condition is open circuit.

1.5 Research Contributions

From this project, those users having the problem regarding the Power System Networks issues could be easily to implement this method as a value added for minimizing the nominal fault current.

For more understanding is, the contribution of this project is to get the minimum nominal fault current value through the suitable location of FCL. From this minimum value of fault current, it can provide the voltage stable in the system during the fault event. The voltage problem related to this event is, the voltage dip (sag) can be improved using this method by locating the FCL at suitable location. Another output of this method is to minimize the effect of other adjacent feeder under abnormal condition.

This project also contribute the proper way of explanation for the Fault Current Limiter operating system. In addition, the choosing of the best location of Fault Current Limiter will be identified using this method.

1.6 Project Outline

This project is reported in five chapters, Chapter 1 will involve the Problem Statement, Objective, Scope of Project, Research Contributions and Project Outline to cover the project topic.

After this chapter, Chapter 2 will discuss more on Fault Current Causes, Fault Current Impressions, Types of Fault, Fault Current Protection, and Fault Current Limiter. The next chapter, Chapter 3 is focussing on maximum demand of all substation involved, system during fault at selected buses, location of FCL, and Y-Bus matrix. On the other hand, Chapter 4 is determined the Matlab simulation, and Y-Bus simulation technique.

This report is ended with Chapter 5 which cover the conclusion and recommendation of overall project to cater the findings and any additional suggestion for future improvement.

REFERENCES

- [1] (H. G. Sarmiento, C. Tovar, and E. Malero, "A feasibility study for a fault current limiter to reduce voltage sag at sensible loads," in Industrial and Commercial Power Systems Technical Conference, 1995. Conference Record, Papers Presented at the 1995 Annual Meeting, 1995 IEEE, 1995, p. 99.)
- [2] (C. Po-Tai, H. Chian-Chung, P. Chun-Chiang, and S. Bhattacharya, "Design And Implementation Of A Series Voltage Sag Compensator Under Practical Utility Conditions," Industry Application, IEEE Transactions on, vol. 39, pp.844-853, 2003.
- [3] The fundamental of understanding for the fault current were discussed by:- (S. Eckroad, "Survey Of Fault Current Limiter (FCL) Technologies," S. Eckroad, Ed.: Electric Power Research Institute, 2005.)
- [4] (C. S. Chang and P. C. Loh, "Integration Of Fault Current Limiters On Power System For Voltage Quality Improvement," Electric Power System Research, vol. 57, 2001)
- [5] (Nagata, M. Tanaka, K. and Taniguchi, H. "FCL Location Selection In Large Scale power system," IEEE Transactions on Applied Superconductivity, Volume 11, Issue 1, Part 2, March 2001, pp. 2489-2494)
- [6] (Jen-hao Teng, Chan-nan Lu, "Optimum Fault Current Limiter Placement", the 14th international conference on intelligent applications to power system", ISAP 2007)

- [7] (K. M. Salim, T. Hoshino, A. Kawasaki, I. Muta, and T. Nakamura, “Waveform of the bridge type SFCL during load changing and fault time,” Applied Superconductivity, IEEE Transactions on, vol. 13, pp. 1992-1995, 2003)
- [8] (Yucheng Zhang, Roger A. Dougal, “Specification of Fault Current Limitation Level for FCLs in Power System”, Department of Electrical Engineering University of South Carolina Columbia, SC, USA)
- [9] (Syed Salman Ali Shah, Faheem Khan, Pr. Abdul Mutalib, “Fault Current Limiter for a Distribution Power System”, University of Engineering and Technology, Peshawar, Pakistan)
- [10] (S. Behzadi Rafi, M. Fotuhi-Firuzabad, T. S. Sidgu, “Reliability Enhancement in Switching Substations Using Fault Current Limiter”, 9th International Conference on Probabilistic Methods Applied to Power Systems KTH, Stockholm, Sweden – June 11-15, 2006)
- [11] (J. Cerulli, “Requirements for a Superconductor Fault Current Limiter in the Utility Bus-Tie Location”, IEEE proceedings 1998. Pp 950-955)
- [12] (M. Tarafdar Hahg, S. B. Nageri, M. Jafari, “Improvement of Power System Transient Stability Using a Controllable Resistor Type Fault Current Limiter”, International Conference on Power Systems Transients (IPST2011) in Delft, the Netherlands June 14-17, 2011)