ELECTROCHEMICALLY DEPOSITED GERMANIUM ON SILICON AND ITS CRYSTALLIZATION BY RAPID MELTING GROWTH

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ABSTRACT

It is well known that continuous miniaturization of transistors tends to create several problems such as current leakage, short channel effect, etc. Therefore, introduction of new channel material with higher carrier mobilities such as Germanium (Ge) is suggested to overcome this physical limitation and also to improve the performance of conventional transistors in chips. Basically, there are several techniques to grow Ge such as Chemical Vapour Deposition (CVD) and Molecular Beam Epitaxy (MBE) system. However, these processes require high vacuum environment, highly depend on such hard-to-control variables as well as costly. Therefore, an alternative method that practically cheaper to grow Ge utilizing electrochemical and rapid melting technique is investigated here. In this thesis, a systematic study of electrochemical deposition of Ge on Silicon (Si) substrate is outlined. Results show the unwanted Germanium Dioxide (GeO_2) tends to form in the air-exposed process and germanium tetrachloride:dipropylene glycol ($GeCl_4$:$C_6H_{14}O_3$) electrolyte. Therefore, a Nitrogen (N_2) controlled ambient is preferable. The uniform amorphous Ge film on Si (100) substrate was successfully obtained at the optimum current density of 20 $mAcm^{-2}$ in germanium tetrachloride:propylene glycol ($GeCl_4$:$C_3H_8O_2$) electrolyte. Crystallization of electrodeposited Ge on Si (100) was demonstrated by rapid melting process. Effect of different annealing temperatures from 1000 to 1100 ^oC has also been studied. Raman spectra and Electron Backscattering Diffraction (EBSD) result confirmed that the grown Ge was highly oriented with the crystal orientation identical to that of Si (100) substrate at all annealing temperature tested. Based on depth profile from Auger Electron Spectroscopy (AES) measurement and Raman spectra, it was found that Si-Ge mixing occurred upon rapid melting process, particularly at near the Si-Ge interface caused by atoms diffusion. Calculated Si fraction diffused into Ge region in the Si-Ge mixing was high at higher annealing temperature that shows good agreement with solidus curve of Ge-Si equilibrium phase diagram. Correspondingly, the amount of Ge diffused into Si region also increased as annealing temperature increased. The result also shows that the tensile strain turns from high to low with the increase of annealing temperature. In addition, it drastically becomes more compressive as the depth is approaching the interface of Ge and Si. The difference in thermal expansion coefficient is a possible cause to generate such strain behaviour. For applications, the presence of strain in channel will improve the transistor performance by enhancing the carrier mobility. In conclusion, this study proves that electrochemical deposition and rapid melting growth technique are promising methods for synthesizing crystalline Ge and significantly contribute to the improvement of carrier mobility. It is expected that high performance Complementary Metal Oxide Semiconductor (CMOS) transistor scaling and Moore's Law will continue in the future through new materials introduction in the transistor structure and by incorporating significantly appropriate levels of strain and composition of Ge/Si in the channel.

ABSTRAK

Adalah diketahui umum bahawa pengecilan berterusan transistor cenderung untuk mewujudkan beberapa masalah seperti arus bocor, kesan saluran pendek dan lain-lain. Maka, pengenalan bahan saluran baru dengan mobiliti pembawa yang lebih tinggi seperti Germanium (Ge) dicadangkan untuk mengatasi had fizikal ini dan juga untuk meningkatkan prestasi transistor konvensional dalam cip. Pada asasnya, terdapat beberapa teknik untuk pertumbuhan Ge seperti sistem Pemendapan Wap Kimia (CVD) dan Pancaran Molekul Epitaksi (MBE). Tetapi, proses ini memerlukan persekitaran vakum yang tinggi, sangat bergantung kepada pembolehubah sukar dikawal serta kos yang tinggi. Oleh itu, satu kaedah alternatif praktikal berkos rendah untuk pertumbuhan Ge menggunakan teknik elektrokimia dan lebur pesat dikaji disini. Dalam tesis ini, kajian sistematik berkaitan pemendapan elektrokimia Ge pada Silikon (Si) substrat dilaporkan. Keputusan menunjukkan Germanium Dioksida (GeO_2) yang tidak diingini cenderung untuk terbentuk dalam proses terdedah kepada udara dan penggunaan elektrolit germanium tetraklorida:dipropylene glikol ($GeCl_4$:$C_6H_{14}O_3$). Oleh itu, ambien terkawal Nitrogen (N_2) adalah lebih baik. Filem Ge amorfus yang seragam pada substrat Si (100) telah berjaya diperolehi pada ketumpatan arus optimum 20 $mAcm^{-2}$ di dalam elektrolit germanium tetraklorida:propylene glycol ($GeCl_4$:$C_3H_8O_2$). Penghabluran Ge yang dielektropendap pada Si (100) telah ditunjukkan oleh proses lebur pesat. Kesan suhu pemanasan yang berbeza dari 1000 ke 1100 ^oC juga telah dikaji. Raman spektra dan Pembelauan Balik Serakan Elektron (EBSD) mengesahkan bahawa Ge yang ditumbuhkan adalah berorientasi tinggi dengan orientasi kristal sama dengan Si (100) substrat. Berdasarkan profil kedalaman daripada pengukuran Auger Elektron Spektroskopi (AES) dan Raman spektra, didapati bahawa percampuran Si-Ge berlaku apabila pertumbuhan lebur pesat, terutamanya berhampiran antara muka lapisan Si-Ge yang disebabkan oleh resapan atom-atom. Kiraan pecahan Si yang disebarkan ke rantau Ge dalam pencampuran Si-Ge didapati tinggi pada suhu pemanasan yang lebih tinggi, menepati dengan gambarajah fasa keseimbangan lengkung pepejalan Ge-Si. Sejajar dengan itu, jumlah Ge diresapkan ke rantau Si juga meningkat dengan peningkatan suhu lebur. Hasil kajian juga menunjukkan terikan tegangan bertukar dari tinggi ke rendah dengan peningkatan suhu peleburan. Di samping itu, ia secara drastik menjadi lebih mampat apabila kedalaman menghampiri rantau antara muka Ge dan Si. Perbezaan pekali pengembangan terma antara kedua-dua bahan adalah mungkin penyebab berlakunya ketegangan tersebut. Bagi aplikasi, kewujudan ketegangan dalam saluran akan meningkatkan prestasi transistor dengan meningkatkan mobiliti pembawa. Kesimpulannya, kajian ini membuktikan bahawa pemendapan elektrokimia dan teknik pertumbuhan lebur pesat merupakan kaedah yang baik untuk mensintesis kristal Ge dan memberi sumbangan dalam peningkatan mobiliti pembawa. Dijangka bahawa pengecilan Pelengkap Oksida Logam Semikonduktor (CMOS) transistor prestasi tinggi dan Undang-undang Moore akan berterusan melalui pengenalan bahan-bahan baru dalam struktur transistor dan dengan menggabungkan Ge/Si ke dalam saluran dengan ketegangan dan komposisi yang sesuai.

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LIST OF ABBREVIATIONS

2D	-	two-dimensional
3D	-	three-dimensional
AES	-	Auger electron spectroscopy
AFM	-	atomic force microscopy
a-Ge	-	amorphous germanium
Ar	-	argon
C	-	carbon
CCD	-	charge coupled device
$C_3H_8O_2$	-	propylene glycol
$C_6H_{14}O_3$	-	dipropylene glycol
CH_3COOH	-	acetic acid
CMOS	-	complementary metal oxide semiconductor
Cu	-	copper
CVD	-	chemical vapor deposition
DC	-	direct current
DI	-	deionized
EBSD	-	electron backscattering diffraction
EDS	-	energy dispersive x-ray spectroscopy
FESEM	-	field emission scanning electron microscopy
FET	-	field effect transistor
FWHM	-	full width at half maximum
Ge	-	germanium
$GeBr_4$	-	germanium bromide
$GeCl_4$	-	germanium tetrachloride
GeH_4	-	germane
GeI_4	-	germanium (IV) iodide

GeO_2	-	germanium dioxide
GOI	-	germanium-on-insulator
H_2O	-	water
H_2O_2	-	hydrogen peroxide
H_2SO_4	-	sulphuric acid
HeCd	-	helium cadmium
HF	-	hydrofluoric acid
HNO_3	-	nitric acid
IR	-	infra red
ITRS	-	International Technology Roadmap for Semiconductors
LCD	-	liquid crystal display
LED	-	light-emitting diode
MBE	-	molecular beam epitaxy
MOSFET	-	metal oxide semiconductor field effect transistor
N_2	-	nitrogen
NH_3	-	ammonia
Ni	-	nickel
NMOS	-	n-channel MOSFET
O	-	oxygen
PET	-	polyethylene terephthalate
PMOS	-	p-channel MOSFET
Pt	-	platinum
RCA	-	Radio Corporation of America
RF	-	radio frequency
RHEED	-	reflection high-energy electron diffraction
RMG	-	rapid melting growth
RMS	-	root-mean-square
rpm	-	rotation per minute
RTA	-	rapid thermal annealing
SC	-	standard cleaning
sccm	-	standard cubic centimeters per minute
Si	-	silicon
Si_xGe_{1-x}	-	silicon germanium
SiN_x	-	silicon nitride

SiO_2	-	silicon dioxide
SEM	-	scanning electron microscopy
SPM	-	sulphuric peroxide mixtures
TEM	-	transmission electron microscopy
ULSI	-	ultra-large-scale-integrated circuits
UV	-	ultra violet
XRD	-	x-ray diffraction

LIST OF SYMBOLS

Å	-	angstrom (1 Å = 1.0 x 10^{-10} meters)
$n\ (\omega)$	-	Bose-Einstein occupation number
cm	-	centimeter
J	-	current density
^{o}C	-	degree Celcius
ϕ	-	diameter
$\omega_i(q)I$	-	dispersion of *i*th phonon branch
v_d	-	drift velocity
E		electric field
eV	-	electron volt
ω	-	frequency
$\Delta\omega$	-	frequency shift
d	-	grain size (in nm)
Γ	-	line width
μm	-	micrometer
μ	-	mobility
r_o	-	nanocrystal radius
nm	-	nanometer
I	-	peak intensity from the spectra
x	-	Si composition (x: $0 \leq x \leq 1$)
ε	-	strain
m^*_t	-	transverse electron mass
λ	-	wavelength
q	-	wave vector

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CHAPTER 1

INTRODUCTION

1.1 Overview of present ultra-large-scale-integrated circuits (ULSIs) technology

Silicon (Si) based electronics is one of the most successful technologies in history. Introduction of several innovations such as strained Si [1], high-*k* materials [2-4] and tri-gate [4-6] structure also have enhanced the performance of Si ultra-large-scale-integrated circuits (ULSIs). Conforming to Moore's Law, about more than 10^{19} transistors are made each year and these gains have been possible because the physical size of transistors has been scaling to smaller dimensions progressively, that called as miniaturization process [4, 7-10]. Principally, this miniaturization of transistors is known to be very helpful in increasing the performance of the Si-ULSIs [4, 8-12].

Nevertheless, continuous miniaturization of transistors down to nano-scale regime tends to create several problems such as short channel effect [11, 12], gate leakage current [11, 13] and others. Owing to these physical limitations, the miniaturization of transistors becomes increasingly difficult and the conventional scaling rule will not be enough to enhance the performance of the ULSIs.

According to the International Technology Roadmap for Semiconductors (ITRS) 2009 edition [14], new channel materials with higher carrier mobilities than Si are promising to enhance the switching speed of complementary metal oxide

semiconductor (CMOS) transistors [7, 8, 15-21]. Over the past decade, much attention has been paid to germanium (Ge) and III-V semiconductor channels [7, 8, 15-32] as the candidates to fulfil such purposes. A co-integration of these materials on Si platform should enable the realization of the so-called More than Moore technology [15]. Interestingly, these materials are not only can be used to fabricate high speed conventional CMOS, but also to fabricate new transistors with different operating principles, such as tunnel field effect transistor (FET) [2] and plasma wave device [33, 34] etc, as well as to fabricate various kinds of functional devices such as sensors [35-37], optical devices [38], detectors [34, 39-42], and solar batteries [43], display panels [44, 45] and ultra high frequency electronic devices [34, 40, 46, 47].

In addition, co-integration of these materials on the Si platform is beneficial since Si is a cheap material and available in large wafer size. Si technology is mature and Si based devices are still needed for certain purposes. Therefore, the growth method of these materials, particularly Ge films in this present study, should be tailored so that the well developed Si technology still could be utilized with minimum modification and cost.

Nowadays, there are many researches on the growth of Ge on Si [48-52] which seems to accelerate the realization of such technology. As a result, a co-integration of Ge on Si platform, i.e. Ge/Si heterostructure, seems to offer the present ULSIs with superb multi-functionalities [23]. The evolution idea of Si based nanoelectronics devices is illustrated in **Figure 1.1**.

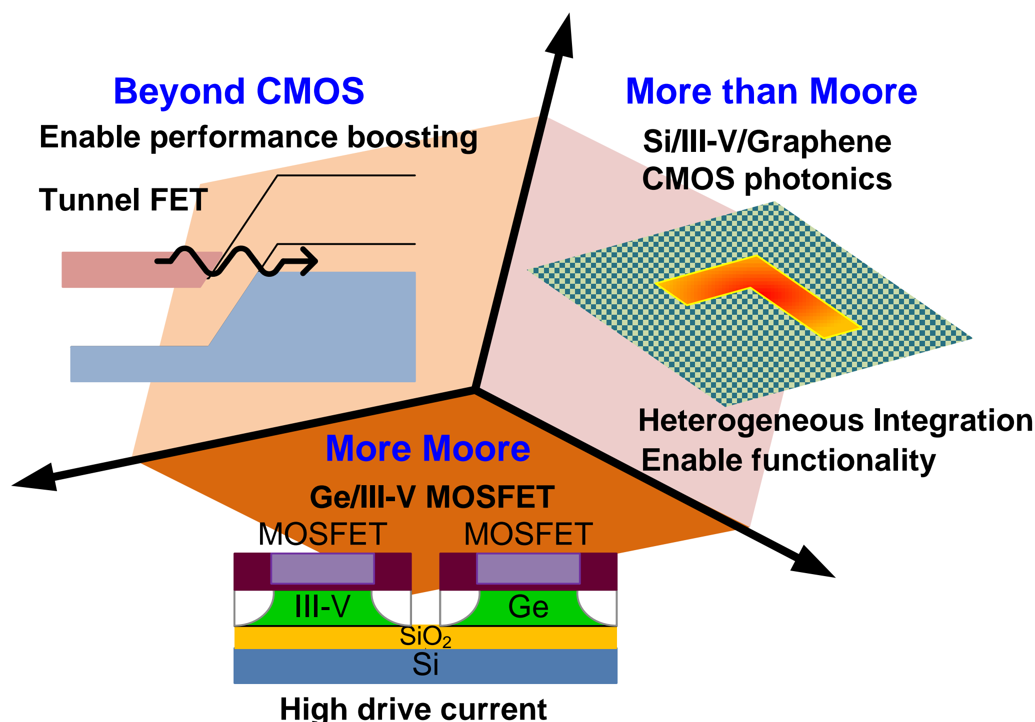

Figure 1.1 Evolution of Si based nanoelectronics (adopted from ref [53, 54])

1.2 Future heterogeneous integration on silicon platform

As the next-generation technology, advanced heterogeneous integration on Si platform has been considered as the promising and practical direction [54]. In this concept, new semiconductor materials with higher carrier mobility than Si are becoming the ideal channel materials to enhance the performance of the conventional transistors in the chips. Ge exhibits electron mobility two times greater and hole mobility four times greater than that of Si [48]. Therefore, Ge channel devices are expected to provide significant performance enhancement.

The growth of high quality materials on Si, particularly Ge films in this present study, is highly required in order to realize such concept of heterogeneous integration. As reported by Takagi *et al.* [23], co-integration of these functional materials on Si platform seems to offer the present ULSIs with superb multi-

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