MODELING AND SIMULATION OF STRAINED GRAPHENE NANORIBBON FIELD EFFECT TRANSISTOR

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Specially dedicated to my family
Thanks to all of you.

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ABSTRACT

Stretching technique used in material fundamental is not a new technology. It has been adopted in silicon industry to overcome the limitations arisen by scaling down the size of the conventional metal oxide semiconductor Field Effect Transistor (FET). This technique is known as strain technology. As the semiconductor industry grows in their maturity, the replacement of strained silicon with another material offering a higher potential quasi-ballistic-carrier velocity and higher mobility is importance. Recent enlisted superior material is quasi-one dimensional Graphene NanoRibbons (GNR). GNR is the most promising material for future nanoelectronic that inherited most properties from graphene and Carbon NanoTube (CNT) itself. To characterize the effect made by strain technology in silicon, an analytical model of strained GNRFET is presented in this work to analyse the suitability of this material for future FET. This works presents a simple model of current-voltage characteristic in the function of strain for different widths. By using a tight-binding approximation and analytical solution, the strained GNR bandstructure, density of states and carrier statistic are presented. Further observation on their carrier transport and their current-voltage characteristic is also investigated and presented in this research. It is found in this research that strain gives significant effect according to different width groups. It is successful in tailoring the energy gap and linearly changing the carrier statistic and carrier transport. In terms of physical and electrical performance, strained 3m+1 GNR is found to be a good material for future FET with enhanced mobility due to the energy gap alteration by strain. Strained GNRFET also was found to be 55mV/dec in subthreshold slope, which is smaller than normal GNRFET, which means the transistor has faster switching. Besides, the current-voltage characteristic is reported to have delayed saturation region compared to published model due to the different in quantum effect consideration.

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G0	-	Maximum conductance
MOSFET	-	Metal-Oxide Semiconductor Field-Effect Transistor
μ	-	Mobility
η	-	Normalized Fermi energy
M(E)	-	Number of mode at an energy, E
C_{ox}	-	Oxide capacitance
h	-	Plank constant
I_{sat}	-	Saturation current
v_{sat}	-	Saturation velocity
ε	-	Strain tensile
T	-	Temperature
v_{th}	-	Thermal velocity
V_T	-	Threshold voltage
K	-	Wave number
W	-	Width

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CHAPTER 1

INTRODUCTION

1.1 Background

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been utilized for several decades as the basic building blocks for almost all integrated circuit. A MOSFET is a transistor that functioned like a ‘heart’ in everything from mobile phones, computers, laptop, cameras and other electronics devices. Rapid advances in electronic technologies have increased the demands of transistors with higher processing speed and lower power consumption. Meanwhile, the size of the transistor needs to be smaller enough to squeeze more devices on a chip in order to achieve the required performance. Famous prediction, known as Moore’s Law has stated that, the number of transistors in a die will be doubled every 18 to 24 months. The graph is shown as in Figure 1.1.

Since decades ago, semiconductor manufacturing is struggling to fulfill and prolonged the Moore’s Law. They are focusing on the size shrinking of MOSFET by scaling down its physical properties. However, continued to decrease the size of transistors into nanoscale regime has led to the severe technology challenges and lithography restriction as shown in Figure 1.2. The scaling method becomes harder particularly after shrinking the size into sub 100 nm. Instead of several physical limitations on doping concentration and gate oxide thickness, the most severe problem is the presence of short channel effect (SCEs). These limitations has resulted in the device performance is not as expected. The challenges due to the lithography process are another problem. Smaller dimension devices increased complexity of process and equipment cost (Schaller, 2004).

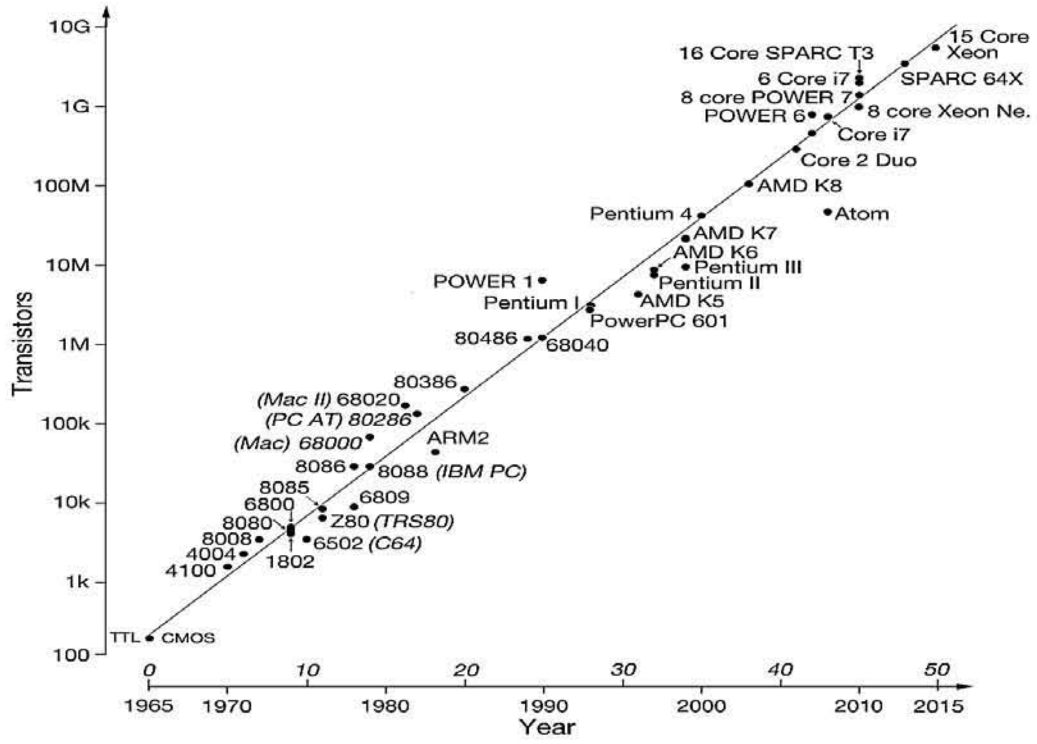

Figure 1.1: The graph of Moore's Law (Scherer, 2015)

The Advanced Lithography 2014 has shown that 13nm half pitch technology is appears to be the end of the line for shrinks. Different technology and devices is required to go below 13 nm. A group of semiconductor industry experts via the International Roadmap of Semiconductor (ITRS) has opened a new paradigm of technologies to extend CMOS platform. The new technologies were introduced under extended plan called 'Beyond Moore' which includes new structures of transistor such as dual gate, FinFet, silicon-on-insulator (SOI) and also introduced new materials to replace current conventional and strained silicon. Candidate materials include strained Ge, SiGe, and a variety of III-V compound semiconductors, carbon nanotubes, and graphene (ITRS, 2014). These novel materials and devices were predicted by ITRS to replace the silicon based technology before reach its limit by the year 2020.

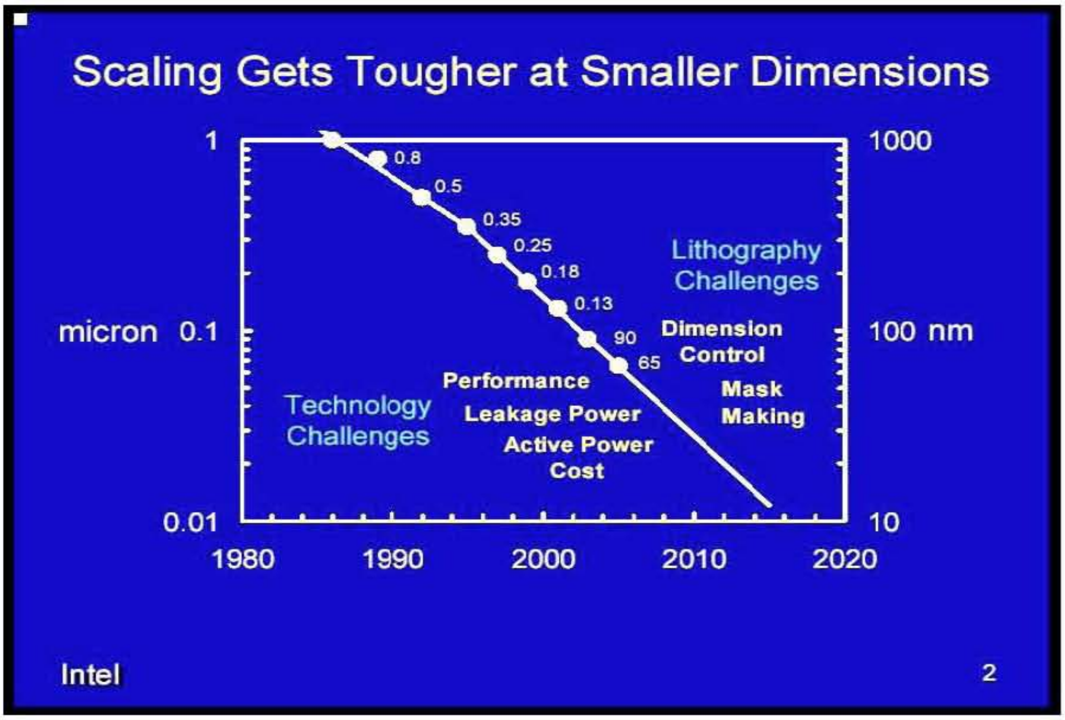

Figure 1.2: Advanced Lithography 2014 (Kim, 2010)

The priority and primary challenge of semiconductor industry is aimed on how to produce absolutely small devices while boosting the performance standard to meet consumer demands. Introduction of non-silicon materials such as carbon nanotubes (CNT) and graphene as the field effect transistor (FET) channel seems to be a most promising solution. However, semiconductor expertise encountered a problem to deal with the CNT chirality (Liang et al., 2007). CNT formed a mixture of metal and semiconductor especially during the fabrication process. Same goes to graphene. Despites of having great features for future FET, it has zero presence of energy gap and behaves in metallic manner (Zhu et al., 2010, Geim and Novoselov, 2007). It is hard to open up the gap eventhough strain technology is used (Ni et al., 2008, Mohiuddin et al., 2009, Li et al., 2010).

Patterning graphene into a narrow channel width can provide graphene with an energy gap (Li et al., 2008, Lu and Guo, 2010). It called quasi one-dimensional (1D) graphene nanoribbon (GNR). The 1-2 nm width of GNR can open up a suitable energy gap useable for FET channel. But, ultra-narrow GNRs (≥ 2 nm) with smooth edges are not easy to be formed. The smooth ribbon edge is important to decrease the scattering effect that may cause the mobility and conductivity of GNR to be degraded. Wider GNR width (>15 nm) have a higher tolerance of edge roughness, therefore their mobility and conductivity show the higher compared to ultra-narrow GNR (Guo, 2012). Unfortunately, the wider the ribbon width, the smaller the energy gap splits (Son et al., 2006). So, it is desirable to change the GNR energy gap for high performance applications.

Strain technology can be applied to GNR in order to tune the energy gap. Currently, strained GNRs are yet to be produced on an industrial scale. The intensive studies are still undergoing to reveal its suitability as FET channel. Strained GNR is absolutely new material which its characteristics are still unclear. Building a device using new material with several uncertainties is high cost and time consuming. Therefore, modeling and simulation is a good choice to study the characteristics of strained GNR based devices before it is fabricated and produced by the industry.

1.2 Problem Statements

Strain in semiconductor industry is not a new technology. It has been applied in silicon technology and helps boosting the silicon-based devices performance. Not to forget that, strain also normally introduced in semiconductor material due to the lattice mismatch during a fabrication process. Thus, this is a need to understand the behaviour of material under strain. In this research we focused on GNR, upon tensile uniaxial strain. One approach to investigate the strain effect on GNR is using the tight binding model and ab-initio calculation. An analytical modeling approach is also used to model the strained GNR around low energy limit region.

There has been a number of computational works such as work done by Mei et.al and Guo et.al on the modeling and simulation pertaining to strained GNR physical and electrical properties. However the simulation tends to focus on the simple tight-binding bandstructures of GNR and exclude the main effect which is the third nearest neighbour (3NN) and edge bond relaxation. Eventhough the simulations on strained GNR electrical characteristic are overflowing, there are still a bunch of question remain unclear. Question arisen especially on how straining the lattice affects the carrier's statistic and transport in GNR which is not much studied. As the GNR behaviour depends strongly on the width, it is still questionable how strain reacts in the certain GNR width to further change the normality.

Proposed GNRFET experimentally and theoretically proved have better current characteristic. Thus, investigations the strain effect on the carrier statistic and carrier transport are paramount important to further answer the questions arising from GNR current-voltage characteristic upon strain. These works is important in order to observe the performance of strained GNR at device level for the next generation FET.

1.3 Research Objectives

This research is focusing on modeling the strained GNR field effect transistor. The following are the objectives of this research:

1. Study the effect of strain to GNR carrier statistic and carrier transport
2. Model the current-voltage characteristic of strained GNRFET

3. Evaluate the strained GNRFET in term of electrical performance by comparing the formulated current-voltage model with the experimental or published data.

1.4 Research Scopes

The following scopes are conducted in order to achieve the objectives of this research:

1. Analytical derivation is performed to formulate strained GNR carrier statistic and carrier transport model from the bandstructure modified by strain.
2. Modeling the current-voltage characteristic of strained GNR.
3. Simulate the formulated model using MATLAB simulation software.
4. Analysed and validate the suitability of formulated strained GNRFET in term of electronic and electrical performance

1.5 Research Contributions

Strained GNRFETs are structures in which the conventional planar MOSFET channel is replaced with a strained graphene nanoribbon. Work on strained based material is currently becomes trend and proceeding at a rapid pace. But for the new material like strained GNR, there are still many issues to address and discover. The purpose of this study is to investigate the characteristic of strained GNR properties and provide a better understanding of strained GNR behaviour through analytical modeling. This is important to predict the suitability of strained GNR as a future channel material for FET. This research also provides a simulation of strained

GNRFET to explain in detail the overall device performance. Therefore, this research can be used as a preliminary analysis to further develop the device at the state-of-the-art for future nanoelectronics.

1.6 Thesis Organization

The research is conducted to model the strained GNRFET through analytical and simulation method. The thesis work had been divided into 6 chapters. Chapter 1 discusses the background of the research study by stating the problem statements, research objectives, research scopes and contributions of the research. The literature review that provides the root of the studies about graphene, graphene nanoribbon and strained graphene nanoribbon was performed in Chapter 2. This chapter also presented the previous studies done by other researches in the same field.

Chapter 3 discussed the research flow and methodology adopted in this research. The research activities, research flowchart and software tools used to complete the research are also briefly reported in this chapter. The results and findings from the research were demonstrated in Chapter 4 and Chapter 5. The modeling in this chapter includes the modeling of strained GNR bandstructures, the carrier statistic and carrier transport model. In the carrier statistic part, the brief explanation about the states and carrier densities were presented. This thesis also demonstrated the carrier flow and electrical characteristic for strained GNR in the carrier transport model sub-topic.

The formulated model performance evaluation as well as the validation was discussed in Chapter 5. The evaluation on the suitability of strained GNR over the other devices in term of electrical performance was also discussed in this chapter. Finally, all the works done in this research was concluded in the Chapter 6.

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