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Comparison Analysis on Scaling the Vertical and Lateral NMOSFET in Nanometer Regime

(Analisis Perbandingan Penskalaan NMOSFET Menegak dan Mendatar dalam Regim Nanometer)

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ABSTRACT

Conventional lateral and vertical n-channel MOS transistors with channel length in the range of 100 nm to 50 nm have been systematically investigated by means of device simulation. The comparison analysis includes critical parameters that govern device performance. Threshold voltage V_T roll-off, leakage current I_{off}, drain saturation current I_{Dsat} and sub-threshold swing S were analyze and compared between the device. Due to double gate (DG) structure over the side of silicon pillar a better electrostatics potential control of channel is obtained in vertical device shown by an analysis on V_T roll-off. A two decade higher of I_{off} in planar device is observed with L_g=50 nm. A factor of three times larger I_{Dsat} is observed for vertical MOSFETs compared to planar device. The sub-threshold swing S remains almost the same when the L_g larger than 80 nm. It increased rapidly when the L_g is scaled down to 50 nm due to the short channel effect SCE. However, the vertical device has a steady increase whereas the planar device has suffered immediate enhance of SCE. The analysis results confirmed that vertical MOSFET with double-gate structure is a potential solution to overcome SCE when scaled the channel length to 50 nm and beyond.

Keywords: Vertical MOSFET; DIBL; double-gate; surrounding-gate

ABSTRAK

Kajian terperinci berkenaan transistor MOS jenis-n secara menegak dan mendatar dengan kepanjangan saluran L_g dalam lingkungan 50 nm ke 100 nm telah dijalankan berdasarkan pensimulasian peranti. Analisis perbandingan meliputi parameter kritikal yang mengukur prestasi peranti. Penurunan voltan ambang V_T, arus bocoran I_{off}, arus tepu salir I_{Dsat} dan ayunan sub-ambang S telah dianalisis dan dibanding antara peranti. Disebabkan struktur dua get (DG) di sisi tiang silikon, kebolehupayaan elektrokstatik kawalan saluran yang baik dapat dilihat pada peranti tegak dengan menjalankan analisis prestasi kejatuhan voltan ambang (V_T). Dua dekad lebih tinggi I_{off} dapat diperhatikan pada peranti mendatar dengan L_g=50 nm. Faktor tiga kali lebih besar I_{Dsat} diperhatikan pada MOSFET menegak berbanding peranti mendatar. Ayunan sub-ambang S adalah hampir sama apabila L_g besar daripada 80 nm. Ia menaik secara mendadak apabila L_g diskalakan ke 50 nm disebabkan kesan saluran pendek (SCE). Peranti menegak mempunyai kenaikan yang agak sekata manakala peranti mendatar mengalami kenaikan mendadak SCE. Keputusan ini membuktikan bahawa MOSFET menegak dengan stuktur dua-get berpotensi bagi mengatasi SCE apabila kepanjangan saluran diskalakan ke 50 nm dan kebawah.

Kata kunci: MOSFET tegak; DIBL; dua-get; get-keliling

INTRODUCTION

Aggressive scaling of CMOS technology into the nanometer regime requires an innovative approach for overcoming various physical limits such as gate oxide thickness (t_{OX}) and channel doping effects. The corresponding short channel effect (SCE) such as leakage current, drain induced barrier lowering (DIBL), threshold voltage (V_T) roll-off and velocity saturation has also need to be carefully addressed in assessing the performance of transistor design structure. Vertical MOSFETs built on the sidewalls of vertical pillars are increasingly being studied as an alternative to standard lateral MOSFETs for the scaling of CMOS into the nanometer regime (ITRS 2006; Jayanarayanan et al. 2006; Mori et al. 2002; Hergenrother et al. 1999; Saad et al. 2006). They are numbers of important advantages over planar MOSFETs for this technology. First, the channel length (L_g) has no dependence on the critical lithography. Second, the vertical MOSFET can double the channel width per transistor area leading to an increased packing density and the drive-on current that is twice as large. Third, a fully depleted (FD) vertical MOSFET provides almost ideal sub-threshold slope and excellent SCE immunity. Considering these advantageous features, the vertical double gate MOSFET (VDGM) is suitable for high-density, low-voltage and low-power DRAM applications.

Generally, there are two methods to fabricate vertical MOSFET. Utilizing epitaxial growth such as molecular beam epitaxy (MBE) is one alternative (Jayanarayanan et al. 2006; Mori et al. 2002; Hergenrother et al. 1999; Saad et al. 2006). However, this approach is not CMOS compatible. The other method is to etch silicon pillars and then diffuse the implanted dopants (Liu et al. 2003; Schulz et al. 2001; Gili et al. 2004). Nevertheless, the minimum channel length that can be reached in this way is limited by the height of silicon pillar and the thickness of nitride fillets. Non-self-aligned channel also contribute to this problem. This limits the scaling of such devices into nanoscale. An oblique rotating ion implantation (ORI) method has been utilized to address such problem (Saad & Ismail 2007a; Okumura. et al. 1992; Saad & Ismail 2007b). A comparison study of scaling L_g of vertical double gate MOSFETs fabricated with ORI method and standard planar MOSFET is successfully done for 100 nm to 50 nm in the aid of numerical simulation (Silvaco-ATLAS 2005).

Device Structure

The standard planar and vertical MOSFET structure illustrated as in Figure 1 respectively. The complete fabrication process for vertical MOSFET was explained elsewhere (Saad & Ismail 2006). Compatible process parameters for both devices are maintained such that a valid comparison is made. The channel and source/drain doping is 5×10^{18} cm^{-3} and 1×10^{20} cm^{-3} respectively with junction depth of between 100 nm to 120 nm. The conductance of insulating film is considered as zero by switch-off the models of tunneling current through the gate oxide t_{OX}. A $t_{OX} = 5$ nm and silicon body thickness $t_{si} = 136$ nm was set for both devices. For scaling the channel length of vertical MOSFET, the height of silicon pillar during dry etch process was vary from 200 nm to 300 nm. Such heights with fixed nitride thickness of 97 nm will approximately prepared 100 nm to 50 nm channel length. By modifying the dry etch parameter and simultaneously observed the obtained L_g based on source/drain impurity junction concentration profiles the analytical correlation is plotted as in Figure 2.

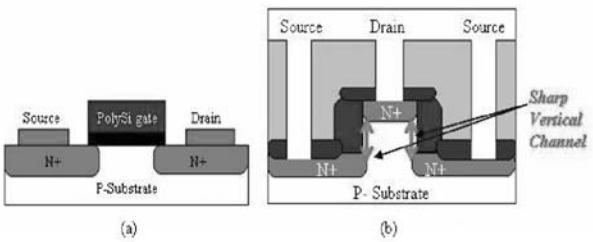

FIGURE 1. (a) Standard plannar MOSFET and (b) Vertical MOSFET with sharp vertical channel fabricated with ORI

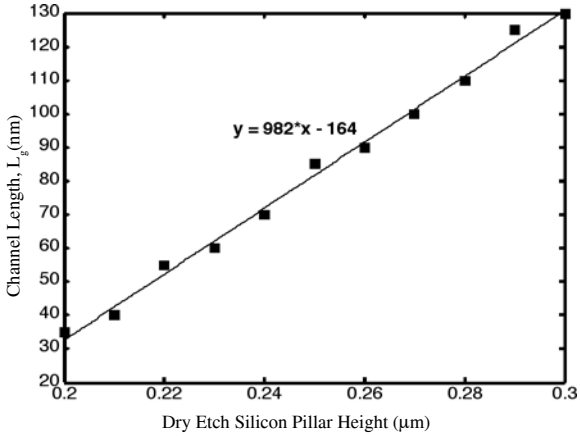

FIGURE 2. Analytical correlation of defining channel length of vertical MOSFET with dry etching of the silicon pillar height

As depicted in Figure 2, a linear correlation has been obtained between silicon pillar height and L_g where it's analytical expression given as:

$$y = 982x - 164. \quad (1)$$

Using (1) we can explicitly calculated the obtainable L_g. For example, with 0.22 mm silicon pillar height the L_g is 50.04 nm. In contrast, for scaling the planar MOSFET L_g, the polysilicon gate length needs to be scaled accordingly before the source/drain ion implantation took place. This process is highly dependent on the accuracy of etching the polysilion gate length by the critical lithography process and limits by the wavelength of the light. In vertical MOSFET with 0.22 μm silicon pillar height, a channel length of 50 nm is reachable presume relax lithography dependent. The 0.22 μm is easily can be done using normal photolithography steps without the needs of using the expensive electron beam lithography.

Numerical Simulation

The characterization of any semiconductor device is done by solving three differential equations numerically and self-consistently within explicitly defines nodes or meshes of the device. By Poisson's equation, the electrical potential energy and electronic band structures can be calculated. Continuity equations for electrons and holes are then used to calculate the current densities of electrons and holes. The process of solving these two equations needs the solution of transport equations or charge transport models obtained by applying an approximation to Boltzmann Transport Equation (BTE). Carrier transport is modeled using a drift-diffusion model based on work for non-planar device and is applicable here for vertically defined channel of vertical MOSFETs (Lombardi et al. 1988). In general drift-

diffusion models are known to underestimate the drive current in MOSFETs at deep submicron geometries (Bude 2000). Therefore, the absolute values of drive current in these simulations may not be accurate. However, for the purpose of comparison study based on identical models for both device the analysis on IV characteristics and secondary effects are to be captured well. The Lombardi models has taken into account the mobility degradation occurs inside inversion layers through transverse and longitudinal field. In a low electric field, the carrier mobility is given by three components that are combined using Matthiessen's rule:

$$\mu_{\mathrm{T}}^{-1} = \mu_{\mathrm{AC}}^{-1} + \mu_{\mathrm{b}}^{-1} + \mu_{\mathrm{sr}}^{-1} \tag{2}$$

μ_{AC} is the surface mobility limited by scattering with acoustic phonons given by:

$$\mu_{\mathrm{AC}} = \frac{B}{E_{\perp}} + \frac{CN^{1/8}}{T_{\mathrm{L}} E_{\perp}} \tag{3}$$

where B = 4.75 × 10^7 cm/s, C = 1.74 × 10^5, N is total doping concentration, $E_{\perp}$ transverse field and T_{L} is lattice temperature in Kelvin. μ_{b} is the mobility limited by scattering with optical intervalley phonons given by:

$$\mu_{\mathrm{b}} = \mu_0 + \frac{\left\lfloor \mu_{\mathrm{m}} \left(T_{\mathrm{L}} / 300\right)^{-2.5} - \mu_0 \right\rfloor}{1 + \left(N_{\mathrm{A}} / C_{\mathrm{r}}\right)^{0.680}} - \frac{\mu_1}{1 + \left(C_{\mathrm{s}} / N_{\mathrm{A}}\right)^2} \tag{4}$$

where μ_{o} = 52.2 cm^2/(V.s), μ_{m} = 1417 cm^2/(V.s), μ_1 = 43.4 cm^2/(V.s), $C_{\mathrm{r}} = 9.86 \times 10^{16}$ cm^{-3}, $C_{\mathrm{s}} = 3.43 \times 10^{20}$ cm^{-3} and N_{A} is the total density of impurities. μ_{sr}, the surface roughness factor for electrons, is given by:

$$\mu_{\mathrm{sr}} = \delta / E_{\perp}^2 \tag{5}$$

where $\delta = 5.82 \times 10^{14}$ cm^2/(V.s). The mobility degradation due to present of electric field is given by the relation:

$$\mu_{\mathrm{n}}\left(E_{||}\right) = \mu_{\mathrm{n0}} \left[1 / 1 + \left(\mu_{\mathrm{no}} E_{||} / VSATN\right)\right]^{\frac{1}{2}} \tag{6}$$

where μ_{n0} is the electrons low-electric-field mobility and $E_{||}$ is the longitudinal electric field in the direction of current. *VSATN* is the saturated drift velocity calculated from temperature-dependent model (Schwarz et al. 1983):

$$VSTN = v^* / 1 + C \exp\left(T_{\mathrm{L}} / \theta\right) \tag{7}$$

where v^*= 2.4 × 10^7 cm/s, C = 0.8 and θ = 600K. The recombination behaviors between electrons and holes are described by Shockley-Read-Hall equation with fixed carrier lifetimes. An interface fixed oxide charge of 3 × 10^{10} C/m^2 is assumed with the presence of n-type polysilicon gate.

Results and Discussion

The combination of Gummel and Newton numerical methods is employed for a better initial guess in solving quantities for obtaining a convergence of the device structure. By using a transconductance g_m-linear extrapolation (GMLE) method (Tsuno et al. 1999) the threshold voltage V_{T} for channel length between 100nm to 50 nm were extracted for both planar and vertical MOSFET at lower drain voltage, V_{DS}. Figure 3 shows the V_{T} versus the channel length for both devices. As the L_{g} is decreased, the V_{T} decreases due to short channel effect (SCE). However, sharply decrease of V_{T} roll-off is seen to happen for planar device as compared to vertical device. This is due to the double gate structure on both side of vertical channels that makes a better electrostatic control of the channel by the gate even when the channel is scaling down to 50 nm.

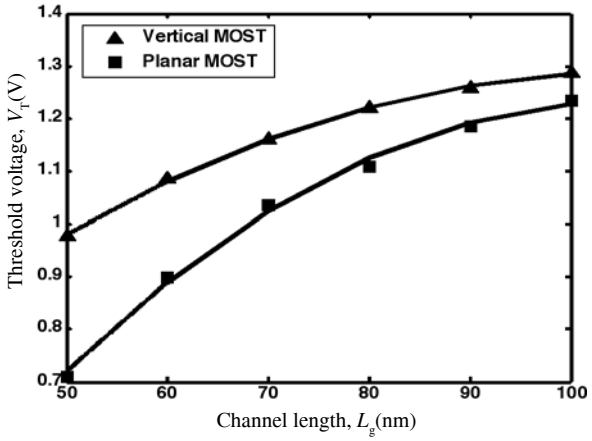

FIGURE 3. Threshold voltage, V_{T} roll-off characteristics for planar and vertical MOSFET down to 50 nm channel length, L_{g}

The leakage current, I_{off} defined as the drain current at V_{GS} = 0V and low V_{DS} was also extracted for both devices. This current which is due to the reverse-biased p-n junction at the drain region is a very important parameter in making sure the immobile state of the transistor in sustaining the power drainage. It's particularly essential as the number of transistors per chip growth monotonically in support of system-on-chip (SOC) paradigm. Figure 4 illustrate the comparison of these values for both devices when the

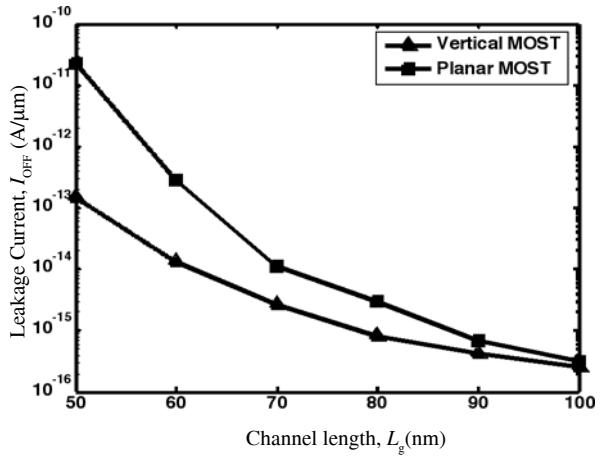

FIGURE 4. Drain leakage current I_{OFF} for both planar and vertical MOSFET extracted at V_{GS} = 0V and low V_{DS}

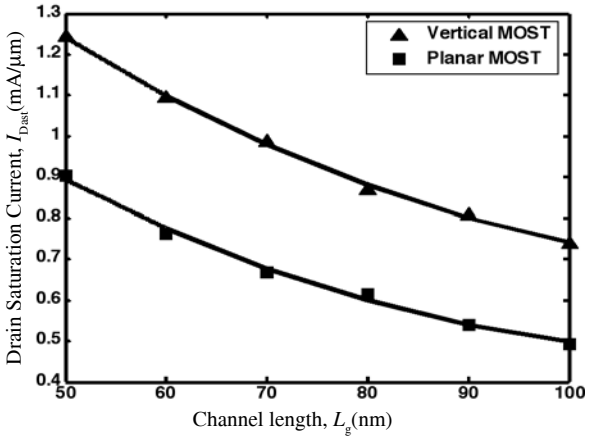

FIGURE 5. Drain saturation current, I_{Dsat} at V_{GS} = 3.3V and V_{DS} = 1.5V for planar and vertical MOSFET

channel is scaling down to 50 nm. With the same body doping, the SCE is pronouncedly observed when the channel is scaled to 50 nm for both devices. However, due to the structure of vertical MOSFET during the drain-on-top (DOT) mode the leakage current is lower compared to planar device. The I_{off} increase with L_g scaled to 50 nm and planar MOSFETs have risen up to two decade higher than vertical MOSFETs. For 50 nm, the $I_{off} = 2.3 \times 10^{-11}$ A/mm and 1.47×10^{-13} A/mm is observed for planar and vertical MOSFETs respectively. This gives an advantage to vertical channel device for making sure a lower value of I_{off} in an application such as DRAM and SRAM.

Rapidly increase of drain saturation current I_{Dsat} is observed in Figure 5 as the L_g scaled down. This is due to mobility degradation at high transverse field and an enhanced of carriers velocity saturation V_{sat} at high longitudinal field. However, a factor of three times larger I_{Dsat} is observed for vertical MOSFETs compared to its counterpart. This is possibly due to an increase of electron concentrations in the channels and better gate controllability in dual channels configuration of vertical MOSFETs. For L_g = 50 nm, the I_{Dsat} is 0.9 mA/μm and 1.24 mA/μm for planar and vertical MOS respectively. Higher I_{Dsat} gives an advantage to vertical device since most of electronics device is operating in the linear region rather than in saturation domain.

For measuring the ON-OFF switching behavior of the device, the lower value of S swing or a steep sub-threshold slope S is necessary. The dependence of the sub-threshold slope for both devices on the channel length is shown in Figure 6. The sub-threshold voltage remains almost the same when the channel length is larger than 80 nm. But, it increase rapidly when the channel length is scaled down to 50 nm due to the SCE. However, the vertical device has a steady increases whereas the planar device has suffered immediate enhance of SCE. An almost ideal value of S = 78 mV/dec was obtained for vertical MOSFET with L_g = 60 nm and increased to S = 82 mV/dec as the channel goes to 50 nm. On the other hand, the planar device has

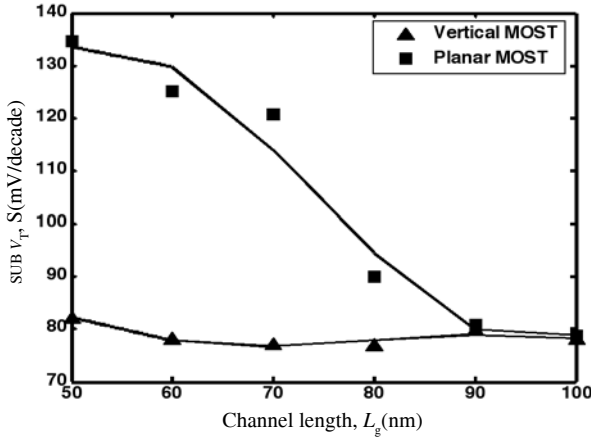

FIGURE 6. Sub-threshold slope or swing S for planar and vertical MOS at V_{DS} = 1.5 V and lower V_{GS}

almost plane S = 83 mV/dec for L_g = 90 nm and 100 nm and rapidly increase from 90 mV/dec to 132 mV/dec for L_g = 80 nm and 50 nm respectively.

CONCLUSION

Comparative study has been successfully done between the conventional planar MOSFET with vertical MOSFET with double-gate (DG) structure. The unique structure of vertical MOSFET was defined using self-aligned oblique rotating ion implantation (ORI) method. The channel lengths of both devices were scaled from 100 nm to 50 nm regime. The comparison includes critical parameters of the device that govern their performance. Threshold voltage V_T roll-off, leakage current I_{off}, drain saturation current I_{Dsat} and sub-threshold swing S were analyze and compared between the device. The physical explanation concerning the devices behavior is well given and captured. In evaluating V_T roll-off, the double gate (DG) structure over the side of silicon pillar has been shown to have a very good electrostatic gate control over the channel, enabling channel

length scaling down to 10 nm for vertical MOSFET. The increase in I_{off} as the L_g scaled to 50 nm is shown to happen for both devices. However, the planar MOSFETs have risen up to two decade higher than vertical MOSFETs. For 50 nm, the planar device has $I_{off} = 2.3 \times 10^{-11}$ A/mm whereas a lower leakage current of 1.47×10^{-13} A/mm is observed for vertical MOSFETs. The effects of mobility degradation at high transverse field and an enhanced of carriers velocity saturation V_{sat} at high longitudinal field is performed by measuring the drain saturation current I_{Dsat}. A factor of three times larger I_{Dsat} is observed for vertical MOSFETs compared to planar device. For L_g = 50 nm, the I_{Dsat} is 0.9 mA/μm and 1.24 mA/μm for planar and vertical MOS respectively. An almost ideal value of S = 78 mV/dec was obtained for vertical MOSFET with L_g = 60 nm and increased to S = 82 mV/dec as the channel goes to 50 nm. On the other hand, the planar device has almost flat S = 83 mV/dec for L_g = 90 nm and 100 nm and rapidly increases from 90 mV/dec to 132 mV/dec for L_g = 80 nm and 50 nm respectively. These results show that the vertical transistor is seen to offer considerable advantages down to the 50 nm node and beyond due to the dual or surrounding channels configuration and the ability to produce a 50 nm channel length with relax lithography.

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