Design and Simulation of a High Performance Lateral BJTs on TFSOI

Ismail Saad and Razali Ismail
Faculty of Electrical Engineering, University Technology Malaysia, 81310, Skudai, Johor Bharu,
E-mail: ismail_s@ums.edu.my, razali@fke.utm.my

Abstract **Lateral BJT's have received renewed interest with the advent of BiCMOS and Silicon on Insulator (SOI) technology. It's been reported in [1] that a 67 GHz f_{max} novel lateral BJT's on TFSOI has been fabricated with a simplified process. This paper presents an investigation of this high performance transistor by using 2D process and device numerical simulation. Accurate geometrical structure and reasonably good doping profiles with a simple fabrication process are successfully achieved in the process simulation. However, a careful attention is required to define the mesh for the device to obtain an accurate measurement of device characteristics. With a base, low-doped collector, emitter and high-doped collector concentrations of 3 x 10^{17} cm^{-3}, 1.0 x 10^{17} cm^{-3}, 5 x 10^{20} cm^{-3} and 3 x 10^{20} cm^{-3} respectively, a variation of 0.1– 0.13μm base width is observed. I-V and frequency performance of these transistors are simulated and analyzed. Y-parameter measurement at frequency 10 MHz - 1000 GHz shows a 21 GHz f_{max} was successfully achieved at V_{BE}=0.7V, V_{CE}=2.0V and I_{CE}=6.0 μA.**

I. INTRODUCTION

Most existing BiCMOS processes combine high-performance vertical BJT's with MOSFET's. These technologies offer a trade-off between speed and power dissipation and attain digital/analog systems with a performance exceeding that of circuits based on either technology alone [2, 3]. This results in a rather complex and expensive process due to the technological incompatibility of two types of transistors [4]. Several sophisticated technologies such as self-aligned double-polysilicon structure [5], shallow and/or deep trench isolation [6] and an epitaxial base [7] has been used. However, such superior process technologies increase fabrication costs of RF LSI's. Consequently, the cost of the extra steps to produce the buried layer and epitaxial collector vertical bipolar transistors has also limited BiCMOS LSI's marketability [8]. With the advantages of low power and high speed operation and simpler integration of devices, Silicon on Insulator (SOI) has become an excellent candidate as an alternative substrate for BiCMOS circuits. Furthermore, the use of SOI as a substrate in BiCMOS circuits is dependent on the development of a proper bipolar device (in a lateral structure) on SOI [9]. A number of novel high performance lateral bipolar's on SOI have been proposed and implemented. All of these transistors have been fabricated with a different approach of structure. This paper presents an investigation of a high performance transistor by carrying 2D process and device numerical simulation [10]. With a base, low-doped collector, emitter and high-doped collector concentrations of 3 x 10^{17} cm^{-3}, 1.0 x 10^{17} cm^{-3}, 5 x 10^{20} cm^{-3} and 3 x 10^{20} cm^{-3} respectively, a variation of 0.1– 0.13μm base width is observed. I-V and Frequency performance of these transistors are simulated and analyzed. Y-parameter measurement at frequency 10 MHz - 1000 GHz shows a 21 GHz f_{max} was successfully achieved at V_{BE}=0.7V, V_{CE}=2.0V and I_{CE}=6.0 μA.

II. DEVICE STRUCTURE AND PROCESS

Figure 1 shows the schematic structure of the lateral bipolar transistor considered in the present study.

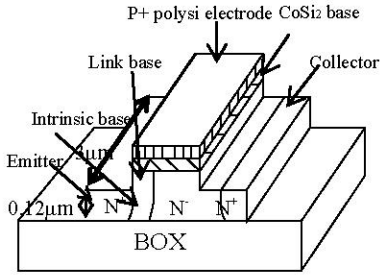

Fig. 1 Schematic 3D cross-sectional view of lateral BJT

The intrinsic base is formed by an angled (45°) boron and BF_2 ion implantation with the condition of BF_2 1.2x10^{12} cm^{-2} at 25KeV, boron

2×10^{12} cm^{-2} at 15 KeV and boron 7.2×10^{12} cm^{-2} at 35 KeV. This gives a flat profiled intrinsic base in the direction of the depth and also provides a link between intrinsic base and the p+ poly Si electrode. The length of this self-aligned link base is about 0.07 μm. An anisotropic poly Si etching process is used to form the poly Si sidewall. The emitter region is formed by ion implantation of phosphorus under the condition of $8.0 \times 10^{15} cm^{-2}$ at 65KeV and N^+ collector is obtained by implanting phosphorus dose of $4.0 \times 10^{15} cm^{-2}$ at 60KeV. RTA for 20 seconds at 950°C is applied to activate the doped impurities. Note that each of the emitter, base and collector regions has to be diffused and penetrated deeply into buried oxide. This is to maintain neutral charge within emitter/base, base/N^- collector and N^- collector/N^+ collector depletion regions and to reduce the junction capacitances. TEOS SiO_2 is then deposited over the transistor for isolation. Cobalt Silicide ($CoSi_2$) is used on the exposed p+ poly-Si to reduce the base resistance. TEOS SiO_2 is deposited again and conventional wiring process is carried out.

The Drift-Diffusion transport model with simplified Boltzmann carrier statistics is employed for numerical computation of the device design [10]. The bandgap narrowing effects in heavy doping surroundings has also taken into account. The standard carrier low electric field mobility concentration dependent and its smooth transition to a high electric field for carrier velocity saturation effects in the direction of current flow models was all switch on. The Auger recombination model combined with SRH model (Shockley-Read-Hall) in concentration dependent carrier lifetimes was also selected for characterization of the device [10]. The workfunction of p+ polysilicon with $CoSi_2$ is given for base electrode contact.

III. RESULTS AND DISCUSSION

Doping Profiles

Horizontal doping profile at the center of device is shown in figure 2, impurity concentration of intrinsic base is $3 \times 10^{17} cm^{-3}$. Both emitter and high-doped collector concentrations are at 4×10^{20} cm^{-3} and 3×10^{20} cm^{-3} respectively. Also, a slight variation in base width, W_B (0.1– 0.13μm) as a function of depth is observed. For a better result, a narrow W_B is vital in making sure that the injected carriers from emitter will reach the depletion region of B/C junction to be swept across the junction into collector region. Thus, an optimized doping profile of base region is very important for definition of narrow base width, W_B. In addition, the vertical impurity profile of the base p+ polysi and n- collector region are also investigated as shown in Figure 3. A flat boron concentration of 2.5×10^{20} cm^{-3} is obtained in p+poly region. As shown in the figure, the boron has diffused into n- collector layer with the junction depth of 63 nm from the interface between p+poly and n^- collector. This diffusion length is an important factor for the high frequency performance of transistor. The diffusion of boron into n^- collector causes the decrease of cross-sectional area of collector region, which results in the increase of the collector current density. Consequently, the f_T-I_C curve falls down earlier as the collector current is increased mainly due to the Kirk effect. However, this will accordingly decrease the breakdown voltage. Thus, the trade-off between increasing doping level of collector region for a higher frequency or faster circuit and high value of breakdown voltage must be carefully optimized.

In overall a trade-off between decreasing the base region and increasing the collector region doping profile for definition of a narrow base width, W_B and minimizing the kirk effect in a reduce series collector resistance is essential for getting a higher frequency performance and more faster circuit operation.

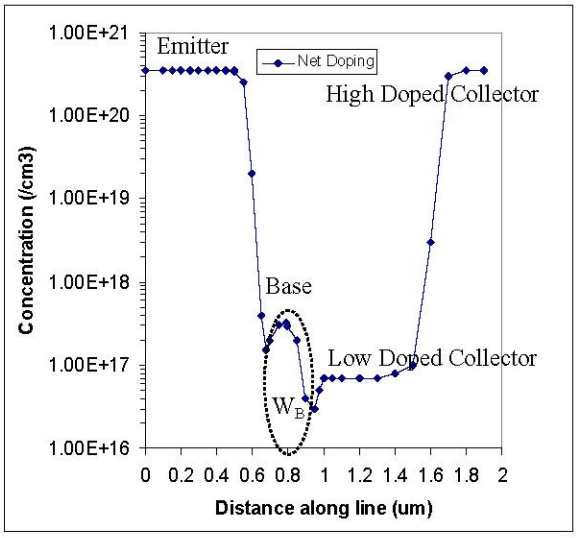

Fig. 2 Horizontal doping profile at the center of device

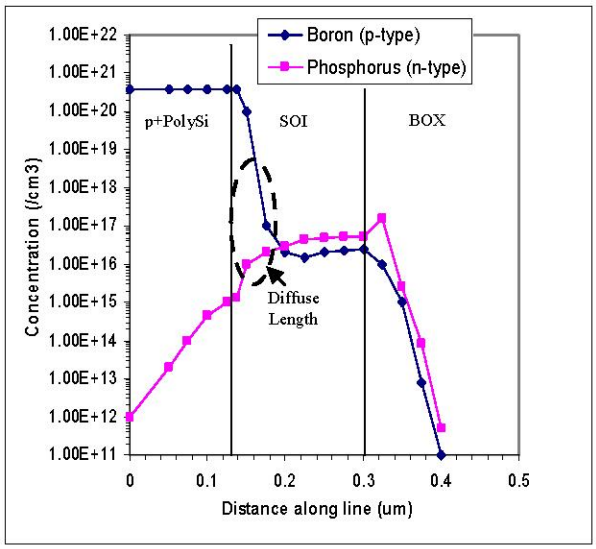

Fig. 3 Transistor vertical doping profiles

Device Characteristics

By using ATLAS DC solutions, the transistor's Gummel plot is obtained (Figure 4) at V_{CE}= 2.0V and V_{BE}= 0.4 – 1.5V. The emitter area is taken as 0.36 μm^2. I_C equal to 0.2 x 10^{-8}A/μm and 3 x 10^{-4}A/μm and I_B equal to 6x10^{-10}A/μm and 6x10^{-7}A/μm at V_{BE}=0.6V and 0.8V, are exhibited respectively. Consequently, a gain of about 350 is obtained at V_{BE}=0.6V. I_C saturates at 2x10^{-4}A, due to high series collector resistance and kirk effect.

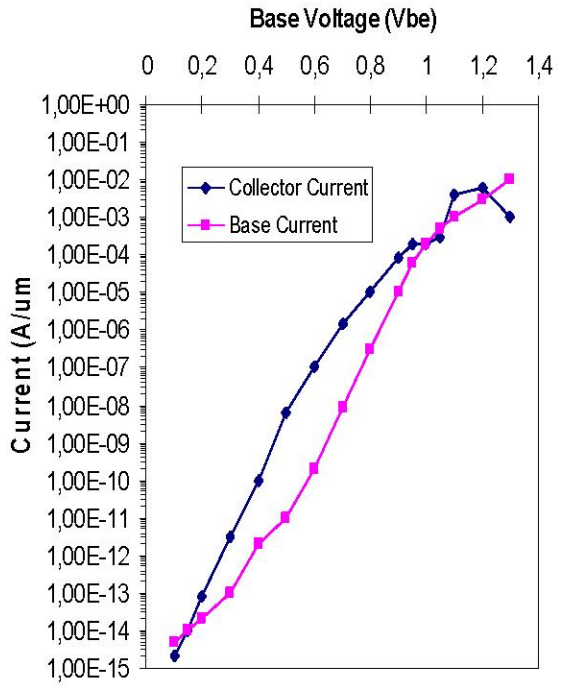

Fig. 4. Gummel plot of transistor at V_{CE}=2.0V& V_{BE}=0.4-1.5V with N_{AB}= 3x10 ^{17}cm^{-3}, N^-_{DC}=1x10^{17}cm^{-3} and β=350 at V_{BE}=0.6V

This effect is minimized in the second transistor simulation by increasing the low-doped collector concentration from 1x10^{17}cm^{-3} to 5x10^{17}cm^{-3} and base region to 2x10^{18} cm^{-3} with $W_B \approx 0.12$μm. This resulted in a higher I_C saturation at 7x10^{-4} A/μm and a larger gain (1000) (Figure 5) at the cost of decreasing the E-C breakdown voltage ($BV_{CEO} \approx$ 4V) obtained from the output characteristics of the device.

Figure 6 shows the cut-off frequency, f_T obtained from y-parameter measurements at frequency 10 MHz - 1000 GHz. A peak f_T (f_{MAX}) of 21 GHz at I_{CE}=6.0 μA is observed for the simulated transistor. With f_{MAX} of 21 GHz and gain of 350 – 1000, an excellent process and device simulation characteristics of the lateral bipolar transistor have been accomplished.

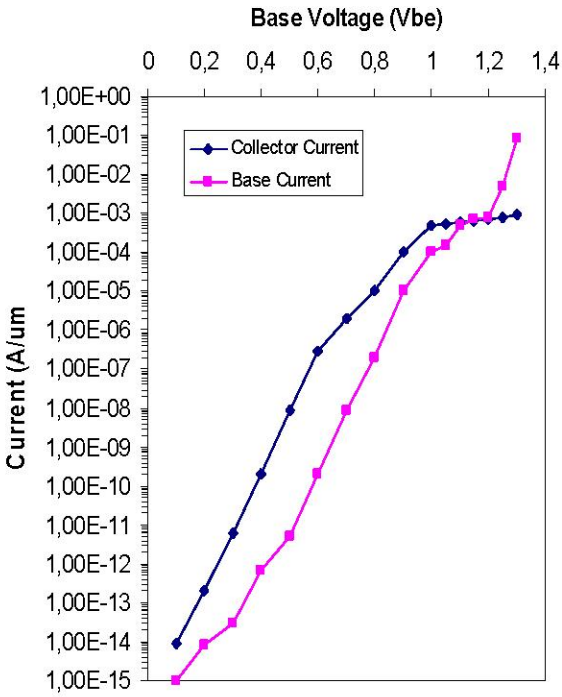

Fig. 5. Gummel plot of transistor at V_{CE}=2.0V and V_{BE}=0.4-1.5V with N_{AB}= 2x10 ^{18}cm^{-3}, N^-_{DC}=5x10^{17}cm^{-3} and β=1000 at V_{BE}=0.6V

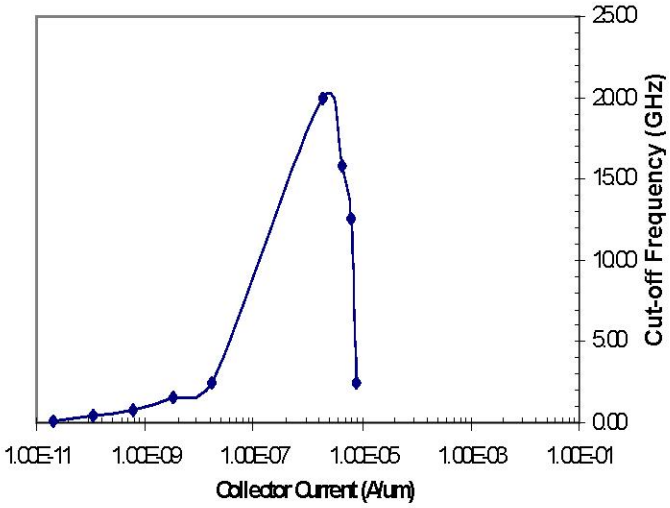

Fig. 6. f_T-I_{CE} (f_{TMAX}) characteristics of transistor at V_{CE}=2.0V

IV. CONCLUSION

The simulation of a high performance lateral bipolar transistor on Thin Film Silicon-On-Insulator (TFSOI) has been successfully carried out. Both process and device simulations for lateral bipolar transistors are carried out in order to understand the device performance. In process simulation, reasonably good doping profiles have been successfully accomplished. In device simulation, the current-voltage (I-V), typical output characteristics and frequency performance of lateral bipolar transistor have been obtained. With increasing N_{DC}^{-} with a factor of less than 5 ($5x10^{17}cm^{-3}$) and reducing N_{AB} by a factor of less than 10 ($2x10^{18}cm^{-3}$) the I_{Csat} has been pushed to occur at $7x10^{-4}$A with V_{BE}=1.1V. Thus, a higher gain of 1000 is obtained with a decreasing value of $BV_{CEO}\approx$ 4.0V. However, for both cases the f_{MAX} of 21 GHz has been obtained and a gain of 350 up to 1000 is observed respectively.

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