Design and Simulation of 50 nm Vertical Double-Gate MOSFET (VDGM)

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Abstract **The paper demonstrate the design and simulation study of 2D Vertical Double-Gate MOSFET (VDGM) with an excellent short channel effect (SCE) characteristics. With the gate length of 50nm, body doping of 3.5 x 10^{18} cm^{-3} and oxide thickness, T_{OX} = 2.5nm, a good drive current I_{ON} of 7 µA/µm and a low off-state leakage current I_{OFF} of 2 pA/µm was explicitly shown. Besides that, the subthreshold characteristics also highlighted a reasonably well-controlled SCE with subthreshold swing $SubV_T$ = 89 mV/decade and threshold voltage V_T = 0.56V. The analysis of body doping effects for SCE optimization and drive current trade-off was also done for an overall investigation and limit of the VDGM.**

I. INTRODUCTION

With the advantages of controlled gate length by a relax photolithographic process, high drives current per unit silicon area and decoupled channel length from packing density, Vertical double-gate (VDGM) and/or surround gate (VSGM) MOSFET become prominent candidate to extend CMOS technology to and beyond the 45nm as depicted by International Technology Roadmap for Semiconductor, ITRS [1]. In contrast, the planar double-gate (DG) has also been intensively in research. The focus is on new structure such as Self-aligned FinFet structure [2, 3, 4], Silicon On Nothing (SON) [5], PAGODA concept [6] and Bonded double-gate [7]. However, this planar device requires advanced processes and precise definition of channel length that make it less acceptable compared with Vertical channel types. Generally, the vertical type MOSFET can be categorized according to channel definition fabrication method. It can be ion implanted process [8-15], epitaxially grown [16-19], and retarded etching [20] on the sidewalls of Silicon pillars. In this paper the structure of a Vertical replacement gate transistor [19], in which the source/drain electrodes are defined by solid state diffusion after channel epitaxial growth is been analyzed with a double-gate configuration. The VDGM device was design and simulated using 2D commercial device simulation (ATLAS) software [21]. The utilization of such process and device simulation for an investigation and detail analysis of new device structure has been raised sharply. Such methods are employed in [22-24]. Using such standard, we demonstrate the design of 2 Dimensional vertical double-gates MOSFET (VDGM) with an excellent short channel effect (SCE) feature. With the gate length of 50nm, body doping of 3.5 x 10^{18} cm^{-3} and oxide thickness, T_{OX} = 2.5nm, a good drive current I_{ON} of 7 µA/µm and a low off-state leakage current I_{OFF} of 2 pA/µm was obtained. In addition, the subthreshold characteristics also highlighted a reasonably well-controlled short channel effects (SCE) with subthreshold swing $SubV_T$ = 89 mV/decade and threshold voltage V_T = 0.56V. An effect of lowering the body doping for getting an acceptable I_{OFF} and V_T as it will increase the surface mobility and drive current was also done. However, an optimization is needed as a high body doping was essential for controlling SCE. The trade-off between controlling SCE with an optimize level of body doping was done explicitly in this paper.

II. MODELING PROCEDURE

The simulated VDGM structure is shown in figure 1a and 1b with the double gate region (in contact), drain and source electrode, channel length L_g, silicon oxide T_{ox}, silicon body and the respective dimensions of the device is explicitly shown. The process start with a mesh or grid definition in which the critical area such as L_g and T_{ox} were given a finer mesh compare to other regions. Subsequently, the coordinates of source, drain, body, left and right gate, gate oxide and separation oxide region were defined. The electrode region of drain, source and double gate area were also formed for the contacts to be

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used in device characterization process later. Notice that an electrode line is visible in figure 1a for making sure that the left and right gate was in contacts. Later, a uniform doping profile is assumed and applied to drain (n-type), source (n-type), double gate (n-type)and body (p-type) of the device with the concentration of $1x10^{20}$ cm^{-3}, $1x10^{20}$ cm^{-3}, $1x10^{21}$ cm^{-3} and 3.5×10^{18} cm^{-3} respectively. The channel body doping may be varied for an analysis on its effects in device performance.

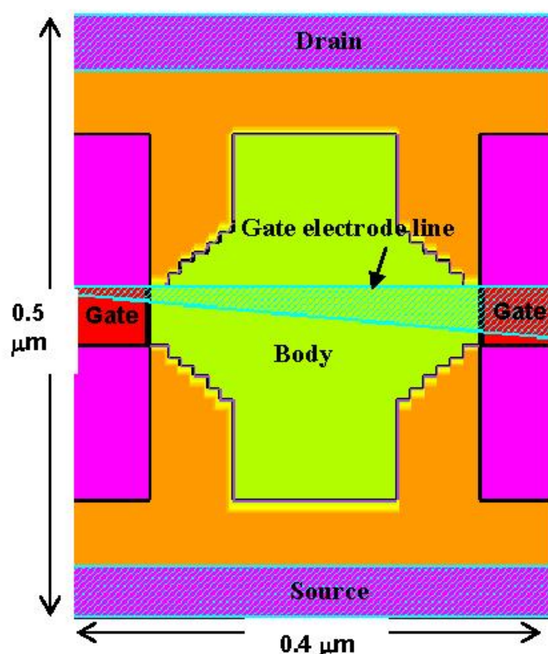

Fig.1a. Vertical Double-Gate MOSFET (VDGM) structure showing double gate, source, drain, and body

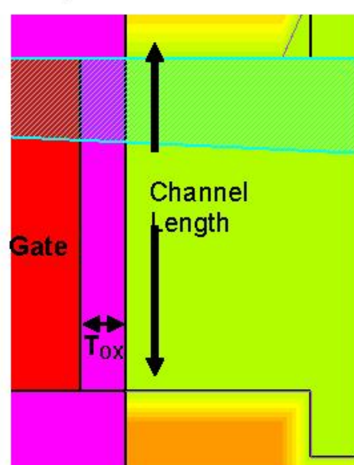

Fig.1b. Vertical Double-Gate MOSFET (VDGM) structure showing channel length and oxide thickness

The inversion layer mobility model from Lombardi [21] was employed for its dependency on the transverse field (i.e field in the direction perpendicular $E_{\perp}$ to the Si/SiO_2 interface of the MOSFET) and through velocity saturation at high longitudinal field (i.e field in the direction from source-to drain parallel E to the Si/SiO_2 interface) combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models [21]. This recombination model was selected since its take into account the phonon transitions effect due to the presence of a trap (or defect) within the forbidden gap of the semiconductor. An interface fixed oxide charge of $3x10^{10}$ is assumed with the used of n-type Polysilicon gate contact for the device. The Drift-Diffusion transport [21] model with simplified Boltzmann carrier statistics [21] is employed for numerical computation of the design device.

III. ELECTRICAL CHARACTERIZATION

The combination of Gummel and Newton numerical methods [21] was employed for a better initial guess in solving quantities for obtaining a convergence of the device structure. Figure 2 shows the current-voltage (I_{GS} – V_{GS}) characteristics for VDGM device with channel length L_g = 50nm, oxide thickness T_{OX}= 2.5nm and body channel doping N_A=$3.5x10^{18}$ cm^{-3}. By using a linear extrapolation of transconductance g_m (V_{GS}) to zero [25] a 0.56V threshold voltage V_T was obtained for both V_{DS}=1.2V and 0.1V in the linear operated region.

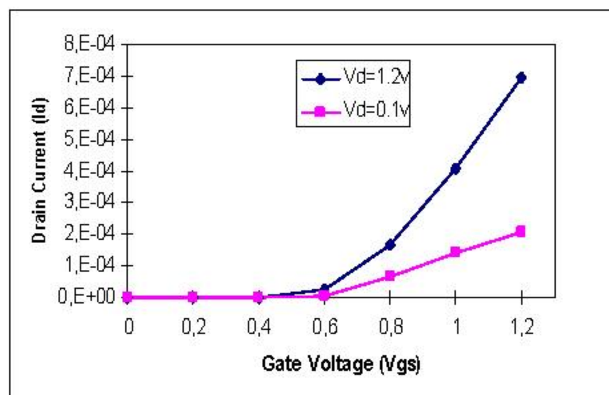

Fig. 2. Current-Voltage characteristic of VDGM with L_g=50nm, T_{OX}=2.5nm, N_A=$3.5x10^{18}$ cm^{-3} and V_T=0.56V taken at V_{DS}=0.1V and 1.2V

A low V_T =0.56V extracted for this device yield that a low power consumption of the MOSFET device is maintained and is comparably better

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with a planar MOSFET for deep sub-micron device [13, 16, 17]. However, this V_T is considerably high for 1.2V intended circuit operation due to a high channel doping N_A that reduces the surface mobility and degrade the drive current I_{ON}. However, high doping is necessary for controlling the SCE. An output characteristic I_{DS}-V_{DS} is shown in figure 3, that explicitly illustrate a moderately low drain current due to a high doping.

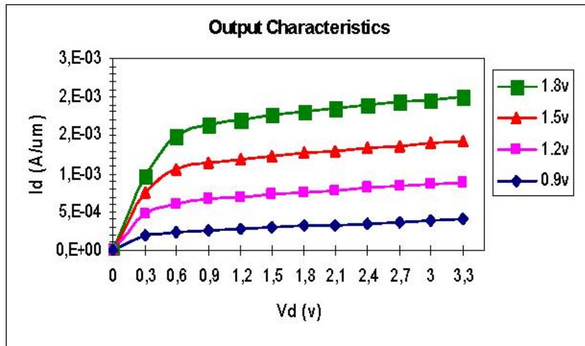

Fig. 3. Output characteristic of VDGM with L_g=50nm, T_{OX}=2.5nm, N_A=3.5x10^{18} cm^{-3} and V_T=0.56V for V_{GS}=0.9, 1.2, 1.5 and 1.8V.

Figure 4 shows a good off-state leakage current I_{OFF} of 2 pA/µm and drive current I_{ON} of 7 µA/µm due to high doping that control the off and on state of the device. Furthermore, reasonably well-controlled SCE with subthreshold swing $SubV_T$ = 89 mV/decade is also highlighted in figure 4.

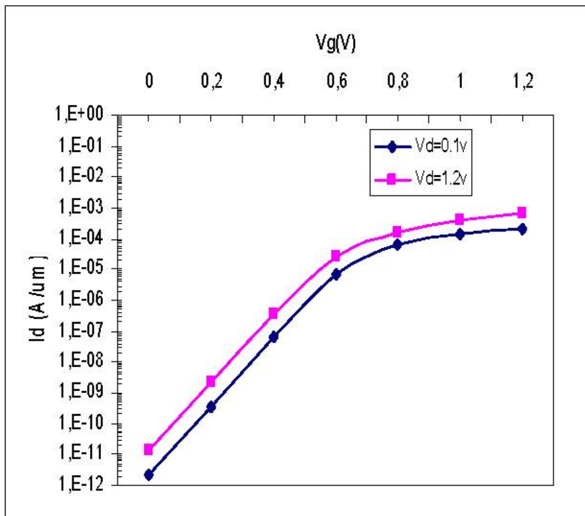

Fig. 4. Subthreshold characteristic of VDGM with L_g=50nm, T_{OX}=2.5nm, N_A=3.5x10^{18} cm^{-3} and I_{OFF}=2pA/µm, I_{ON}=7µm/µm, $SubV_T$=89mV/dec

Further analysis on the VDGM performance was done by comparing its capability to control SCE with single gate MOSFET. By applying the same mobility and recombination model with different channel length which is higher by a factor of 50 in single gate MOS, the resulted subthreshold characteristics is shown in figure 5.

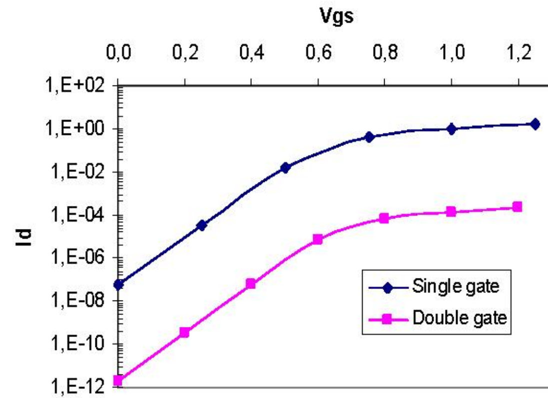

Fig. 5. Comparison of Subthreshold characteristic of VDGM with Single gate MOSFET (SGM). Low leakage current is exhibited in VDGM in pico range as with SGM.

As expected, the vertical double gate give a low off-state leakage current as compared to single gate MOSFET (SGM) and an acceptable OFF/ON ratio due to a better control of electrostatic potential in gate region for the vertical defined channel [8, 9, 10]. However, these was achieved due to a high body doping in VDGM which gave a good SCE control with a high threshold voltage due to a degradation in surface mobility as depicted in figure 2 and consequently reduced the drain current as shown in figure 3. Thus, the effect of body doping has to be analyzed for obtaining an acceptable V_T, I_{DS} and optimize control of SCE. This will be carried out in the next section.

V. Doping Effect Analysis

Three variant of body doping are used: low doped (N_a = 1x10^{18} cm^{-3}), moderately doped (N_a = 2x10^{18} cm^{-3}) and the high doped (N_a = 3.5x10^{18} cm^{-3}). In Figure 6 we can see that V_T is reduced as the doping level is decreased.

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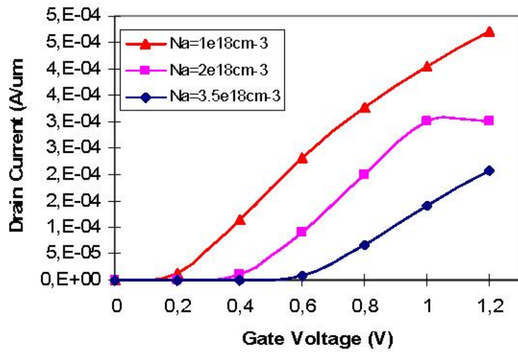

Fig.6. I_{GS}-V_{GS} characteristic of VDGM shows a decreased in V_T is observed with a lower doping level.

The V_T value decreases from 0.56V for high doped to 0.36V in moderate doped and to a lower value of 0.15V in low doped body. Further analysis is done, by comparing the subthreshold characteristics with different doping level as shown in figure 7.

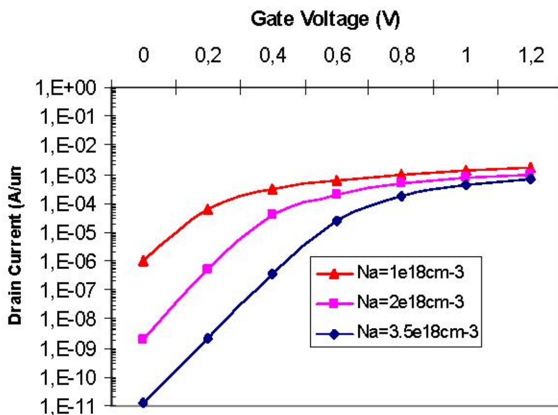

Fig.7. Subthreshold characteristic of VDGM showing an increased in leakage and drive current with a lower doping level.

As can be seen in figure 7, a decreased in doping will ultimately increased the leakage current from 2pA/µm to 7nA/µm and finally to a value of 80µA/µm. However, the increased in drive current is almost unity with a value of 7µA/µm to 10µA/µm and 1mA/µm respectively. These effects arise due to the fact that at higher doping the surface mobility is decreased and a better gate electrostatic potential observed within the device which makes the leakage current controllable. However, as the doping level decreased, the carrier mobility is increased and consequently the leakage current will also rise sharply. On the other hand, since the channel is defined vertically with a double gate configuration, a unity drive current is observed which also increased with a decreased in doping level. Due to a double gate arrangement the increased in drain current (I_{DS}) was observed as shown in figure 8 of the output characteristics.

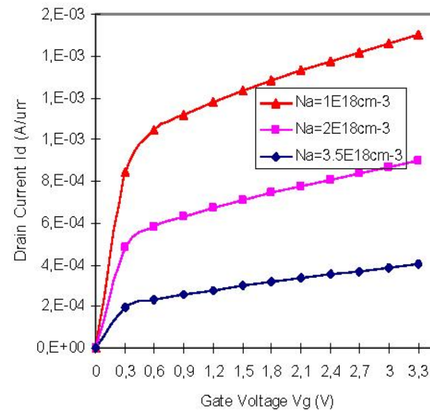

Fig.8. Output characteristic of VDGM shows an increased in Drain current with a lower doping level in a double-gate configuration.

Even though the drive current is high with lower doping level, a high leakage current is observed in figure 7, I_{OFF} = 80µA/µm is highly unacceptable. These results are in conjunction with the value of subthreshold voltage obtained, which is 89 mV/decade for higher doped, 83 mV/decade in moderate doped and sharply increased to 110 mV/ decade in lower doped device as depicted in figure 7. Thus, an optimize value of body doping is highly vital in order to have a high drive current while maintaining the acceptable leakage current and controlling the aggravated SCE. If one fails to control such parameters, the transistor designed will not succeed to work in a giga-scaled integrated circuit where the total standby power of the system is of paramount important.

VI. Conclusion

The design of a 50nm Vertical Double Gate MOSFET (VDGM) device based on the structure reported in [19] has been successfully done using commercial ATLAS TCAD tools. By employing the inversion layer mobility model from Lombardi combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models with an interface fixed oxide charge of $3x10^{10}$ assumed and the used of n-type Polysilicon gate contact, a detailed investigation on the VDGM performance was done. With the gate length of 50nm, body doping of 3.5×10^{18}

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cm^{-3} and oxide thickness, T_{OX} = 2.5nm, a good drive current I_{ON} of 7 μA/μm and a low off-state leakage current I_{OFF} of 2 pA/μm was obtained. In addition, the subthreshold characteristics also highlighted a reasonably well-controlled short channel effects (SCE) with subthreshold swing $SubV_T$ = 89 mV/decade and threshold voltage V_T = 0.56V. The effects of body doping N_A in obtaining a good drive current I_{ON} while maintaining an acceptable leakage current I_{OFF}, threshold voltage V_T and subthhreshold voltage $SubV_T$ for controlling the SCE was investigated. With a moderate body doping level N_A = $2.0x10^{18}$ cm^{-3}, a threshold voltage V_T = 0.36V, leakage current I_{OFF} = 7nA/μm and $SubV_T$ = 83 mV/decade and a good drive current I_{ON} = 10μA/μm was successfully obtained and optimized for the simulated VDGM device.

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