Device Design Consideration for Nanoscale MOSFET Using Semiconductor TCAD Tools

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Abstract The evolution of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) technology has been governed mainly by device scaling over the past twenty years. One of the key questions concerning future ULSI technology is whether MOSFET devices can be scaled to 100nm channel length and beyond for continuing density and performance improvement. In this paper, the design, fabrication and characterization of high-performance and low-power 90nm channel length MOSFET devices are described. Several parameters have to be scaled down such as gate oxide thickness, channel length, ion implantation for threshold voltage adjustment and other specifications to achieve desirable electrical characteristic. To control the short-channel effect (SCE) and hot-carrier reliability that limits device scaling, lightly doped drain (LDD) structure, shallow junction of drain / source and Shallow Trench Isolation (STI) are implemented. Virtual Wafer Fabrication (VWF) Silvaco TCAD Tools is used for fabrication and simulation of CMOS transistor namely ATHENA and ATLAS. Simulations using these programs provided the opportunity to study the effect of different device parameters on the overall device performance. The devices were simulated and gradually the performance of each one was improved, until an optimal device configuration was created for a particular application.

I. INTRODUCTION

Over the past 50 years of the semiconductor industry, the size of MOSFET has been scaled down obeying the Moore's law : feature sizes of transistors are scaled at a rate of approximately 0.7 times every 18 months [1]. However, as MOSFET technology approaches nanoscale region, researchers face with critical technology barrier known as SCE. While the gate voltage fully controls the channel conduction state in an ideal MOSFET, the drain voltage begins to give more influence on the channel potential in a nanoscale MOSFET.

In order to enhance the speed performance of the circuit and for higher density while maintaining its reliability and circuit performance, the MOSFET transistor has been scaled down by using Constant Field Scaling rules because it is easier and assumed to avoid the high field problems. Important parameters like channel length (L), doping concentration (N_A, N_D) during ion implantation for threshold voltage adjustment and gate oxide thickness (t_{ox}) will be scaled [2].

Advanced transistor design such as STI eliminates the bird's beak shape characteristic, subthreshold hump and field oxide thinning effect in LOCOS isolation. STI has advantages such as perfect planarity, scalability and latchup immunity [3]. Besides that, LDD is designed to smear out the strong electric field between the channel and heavily doped s/d, in order to reduce hot-carrier generation. While shallow junction of drain/source can increase device density. To reduce charge sharing effect, halo implant is introduced in which the locally high doping concentration in the channel near the source/drain junctions is created. Retrograde well is a form of vertical channel engineering. It is used to improve SCE and to increase surface channel mobility by creating a low surface channel concentration followed by a highly doped subsurface region.

II. OPTIMIZATION

Optimization is essential in scaling down device to obtain better device performance. Optimization of these devices using the TCAD tools requires many hours of lab simulation time.

Several aspects of each device were selected for optimization. Once the device characteristics were selected for optimization, the process of device simulation began. First each parameter was tested individually for its effect on device performance as a whole. Once several plots were obtained that indicated the particular parameter's effect on device performance, improved values could then be selected for the device. Several simulations needed to be run to find improved values for each device parameter until an optimal value were reached. Once an optimal value was reached for each of the device parameters, the improved parameters were then combined into a single device. When all these new values were present in a single device, they were again simulated and adjusted to optimize based upon their combined effects to ultimately produce an optimal device configuration. Various analysis and discussion are done on particular parameter's effect on device characteristics.

## III. ANALYSIS AND DISCUSSION

There are a number of parameters that affect the value of threshold voltage and drain induced barrier lowering (DIBL) parameter which will result in different device performance and characteristics. Each of the parameters will be discussed in the following section.

A. Effect of Channel Doping on Threshold Voltage

The channel doping depends on several components such as the type of atom being implanted, the dosage and the energy of the implant. The doping concentration and depth are affected directly. Multiple threshold voltages can be achieved by adjusting the channel doping as shown in Fig. 1. Threshold voltage increases as channel doping increases which is comparable to the result reported in the literature [4].
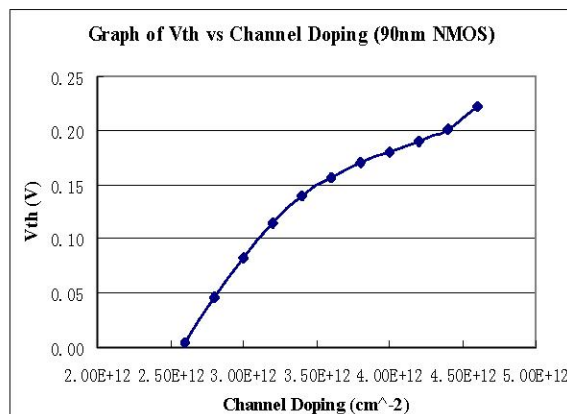

(a)
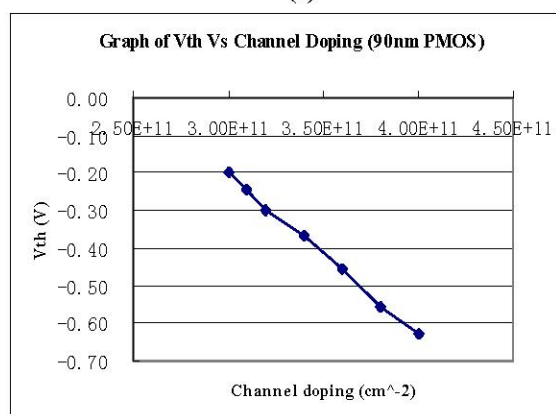
(b)

Fig. 1 Threshold voltages at different channel doping dose for (a) 90nm NMOS (b) 90nm PMOS.

B. Effect of Oxide Thickness on Threshold Voltage

Gate oxide thickness can be used to modify the threshold voltage of a transistor. Variation of threshold voltage with different oxide thickness for a 90 nm device is shown in Fig. 2. Lower oxide thickness and hence lower threshold voltage in critical paths can maintain the performance. Higher oxide thickness not only reduces the subthreshold leakage, it also reduces gate oxide tunnelling current since the oxide tunnelling current exponentially decreases with an increase in the oxide thickness [5].

Graph of Vth Vs Gate Oxide Thickness (90nm NMOS)

(a)

Graph of Vth Vs Gate Oxides Thickness (90nm PMOS)
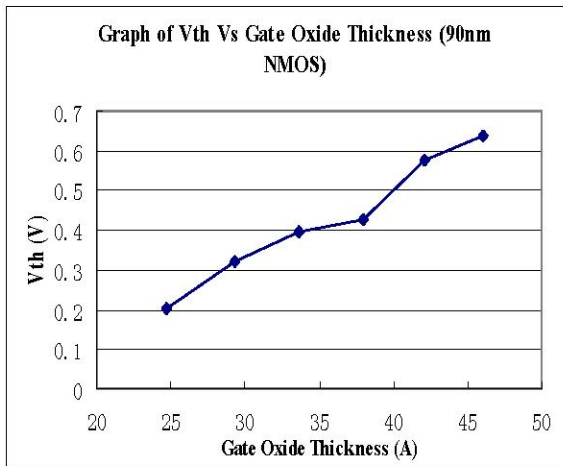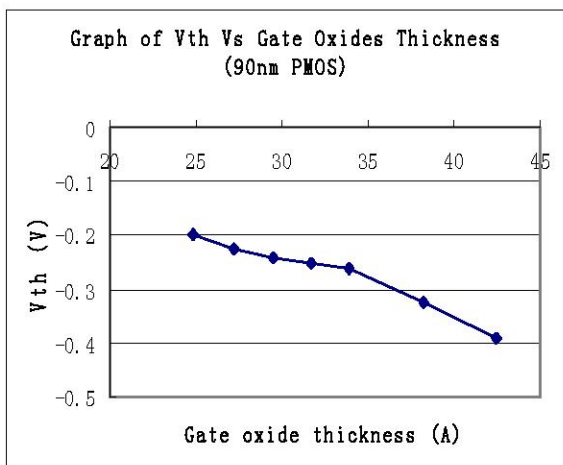
(b)

Fig. 2 Variation of threshold voltage with different gate oxide thickness for (a) 90nm NMOS (b) 90nm PMOS.

C. Effect of Channel Length on Threshold Voltage

Fig. 3 illustrates how threshold voltage of NMOS decreases as the channel length is reduced. Hence, different threshold voltage can be achieved by using different channel length. This reduction of threshold voltage with reduction of channel length is known as threshold voltage rolloff.
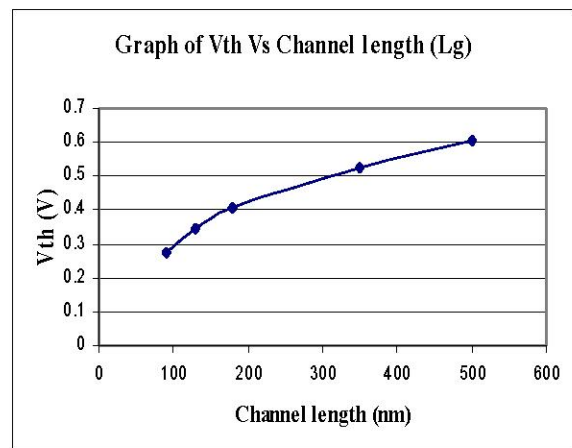
Graph of Vth Vs Channel length (Lg)

Fig. 3 Effect of various channel length on threshold voltage for NMOS.

D. Effect of Drain Voltage on Threshold Voltage

In a short-channel device, the source and drain depletion width in the vertical direction and the source drain potential have a strong effect on the band bending over a significant portion of the device. Therefore, the threshold voltage and consequently the subthreshold current of short-channel devices, vary with the drain bias. This effect is referred to as drain induced barrier lowering (DIBL).

Fig. 4 is a plot of threshold voltage (V_t) vs drain voltage (V_d) to investigate the varying of threshold voltage as different drain voltage is applied. The threshold voltage decreasing as the drain voltage is increasing which is comparable to the explanation above. For comparison, the value of the threshold voltage of the 90 nm NMOS that is doped with halo implant is higher than the one without halo implant doping which

Graph of Vth vs Vd (90 nm NMOS)

— Vth (without halo)
— Vth (with halo)
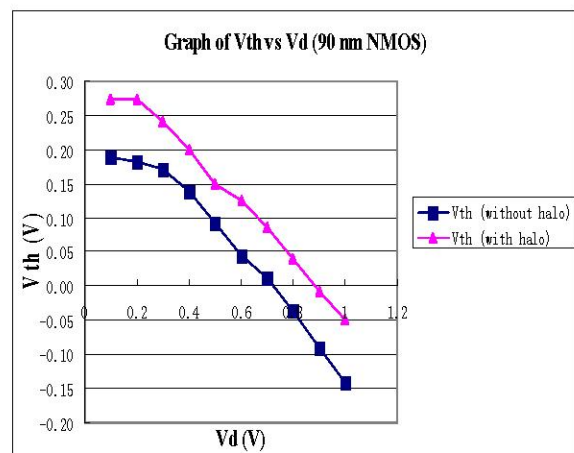
contributes less subthreshold current. By using halo implant, the threshold voltage degradation is reduced.

Fig. 4 Graph of threshold voltage versus drain voltage for 90nm NMOS with and without halo implant.

E. Dependence of Halo Dose on Threshold Voltage

Fig. 5 shows the Id-Vg curves for 90nm NMOS at different halo doses. It can be seen that the value of the threshold voltage increased as we increased the halo dose. Thus, threshold degradation can be controlled well since the halo implant reduces the charge sharing effects from source and drain fields.
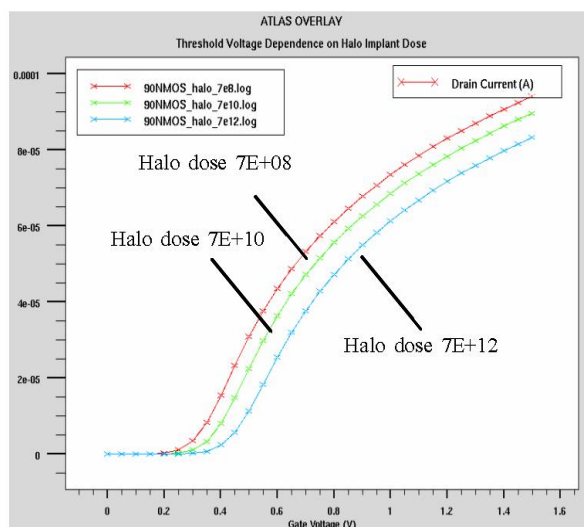

Fig. 5 I_d-V_g curve with different halo doses for 90nm NMOS.

F. Dependence of Threshold Voltage on Retrograde Well Dose

Fig. 6 shows the dependence of threshold voltage on retrograde well dose. The threshold voltage for 90 nm NMOS is increased by the increasing retrograde well dose. Threshold voltage is adjustable by using retrograde well dose as well as using implantation technique.
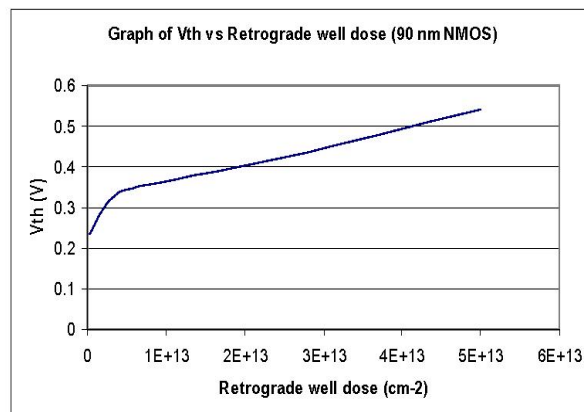

Fig. 6 Graph of V_t versus retrograde well dose for 90nm NMOS.

G. Dependence of DIBL on Halo Dose

Fig. 7 is the graph of DIBL versus halo dose for the 90 nm NMOS with halo implant. It shows that increasing halo implant dose reduces the value of DIBL. This indicates that we can use halo implant to control the MOSFET degradation due to DIBL.

Fig. 7 Graph of DIBL versus halo dose for 90nm NMOS.

H. Dependence of DIBL on Retrograde Well
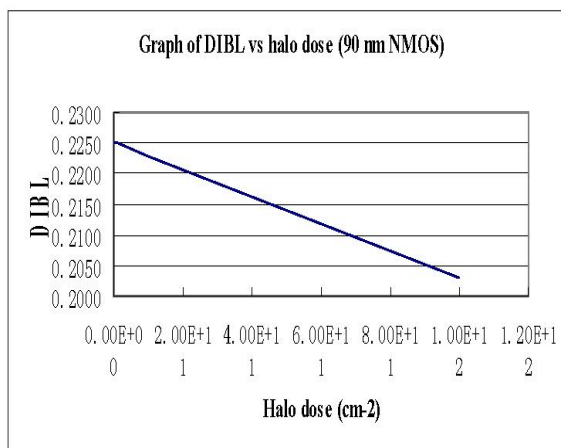
Dose

Fig. 8 shows the effect of DIBL for the 90nm NMOS with different retrograde well doses. The DIBL effect is defined as the change in the threshold voltage ΔV_t divided by the change in the drain voltage ΔV_d. It is clear from Fig. 8 that for a higher retrograde well dose the DIBL will decrease.
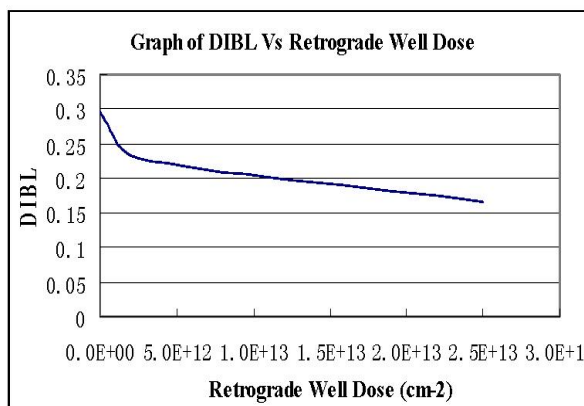

909

Fig. 8 Graph of the dependence of DIBL on retrograde well dose for 90nm NMOS.

I. **Overall Effect of Process Parameters on Threshold Voltage**

Table 1 : The overall effect of process parameters on threshold voltage for 90nm NMOS and PMOS

Table 1 summarized the overall effect of process parameters on threshold voltage for the 90nm NMOS and PMOS. Threshold voltage increased as channel doping, gate oxide thickness, channel length, halo dose and retrograde well dose increased. However, threshold voltage decreased as drain voltage increased.

IV. CONCLUSION

A number of parameters that affect the value of threshold voltage and DIBL parameter which result in different device performance and characteristics are discussed. The improved parameters were again simulated and adjusted to optimize based upon their combined effects to produce an optimal device configuration.

ACKNOWLEDGEMENT

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	Threshold voltage	
	90nm NMOS	90nm PMOS
Increasing channel doping		
Increasing gate oxide thickness		
Increasing channel length		
Increasing drain voltage		
Increasing halo dose		
Increasing retrograde well dose		