Characterization of Strained Silicon MOSFET Using Semiconductor TCAD Tools

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Abstract **- The paper is looking into the enhancement of conventional PMOS by incorporating a strained silicon within the channel and bulk of semiconductor. A detailed 2D process simulation of Strained Silicon PMOS (SSPMos) and its electrical characterization was done using TCAD tool [1]. With the oxide thickness, T_{OX} of 16nm and Germanium concentration of 35%, the threshold voltage V_t for the strained Si and conventional PMOS is -0.5067V and -0.9290V respectively. This indicates that the strained silicon had lower power consumption. Beside that, the drain induced barrier lowering (DIBL) value for the strained PMOS is 0.3034V and the conventional PMOS is 0.4747V, which shows a better performance for strained silicon as compared to conventional PMOS. In addition, the output characteristics were also obtained for SSPMos which showed an improvement of Drain current compared with conventional PMOS.**

I. INTRODUCTION

Scaling down of MOSFET devices has been the driving force in IC industry in order to achieve higher speed and lower power requirements [2]. The recent MOSFET devices have been scaled down to 50nm gate lengths where the gate oxide thickness has become thin enough to suppress the short channel effect (SCE) [3]. However further scaling down of the MOSFET beyond 50nm will cause the SCE to intensify, thus degrading the current drivability and electron mobility of a MOSFET [4]. The continuous downsizing of the gate length have caused the gate oxide to become so thin that current begins to leak across the gate even when there is no applied voltage. Therefore further improvement without minimizing the gate length is strongly required. Carrier mobility improvement has been seen as one of the best alternative for faster devices at lower power levels [5]. Strained silicon technology can offer significant performance enhancement to MOSFET devices [6] by increasing carrier mobility without having to make the devices become smaller [7], [8]. By stressing or straining, the silicon lattice lets electrons flow with less resistance. This will increase the drive current and make the transistor switch faster thus contributing to a higher clock frequency in integrated circuits (IC) with gate length downsizing to 60nm [9]. Another significant improvement in electrical performance for both n and p-channel device of strained Si with 25% Ge composition is demonstrated in [10]. In this paper we will study the performance enhancement by strained silicon as compared to conventional PMOS comprehensively with the help of Silvaco TCAD process and device simulation tools. With the T_{OX} of 16nm and 35% of Ge concentration, the V_T for the strained Si and conventional PMOS is -0.5067V and -0.9290V respectively. The drain induced barrier lowering (DIBL) for the SSPMOS is 0.3034V and the conventional PMOS is 0.4747V, which shows a better performance for strained silicon as compared to conventional PMOS. Consequently, the output characteristics were also obtained for SSPMos that showed an improvement of Drain current compared with conventional PMOS.

II. DEVICE STRUCTURE AND PROCESS

Both strained silicon PMOS with an added SiGe layer and normal conventional PMOS device without SiGe layers process simulation were carried out using ATHENA, Figure 1 shows the structure of both devices. The simulation process to create the strain silicon PMOS is similar to the conventional PMOS fabrication process. The fabrication of SSPMOS device starts by creating a silicon substrate with phosphorus doping of 2×10^{18} cm^{-3} and then a silicon layer with the thickness of 0.018μm is deposited on the silicon

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substrate. Next a silicon germanium (SiGe) layer with 0.35 Ge concentration is deposited on the silicon layer, followed by the deposition of another silicon layer with 0.007um thickness on to the SiGe layer. After the deposition, strained silicon is created at the channel. Polysilicon is then deposited and patterned to form the gate. The process continues with the implantation of source/drain. The boron is implanted with the 1.0 x 10^{15} cm^{-2} doping concentration. Next the silicon nitride (Si_3N_4) layer is deposited and patterned to cover the gate, source and drain. Then the aluminum is deposited and patterned to act as the metal contact. Finally, the final structure of the strained silicon PMOS is created as shown in Figure 1(a).

The conventional PMOS structure is shown in Figure 1(b). The difference between the conventional structure with the SSPMos structure is that there is no added SiGe layer, thin Si layer and Si_3N_4 capping layer.

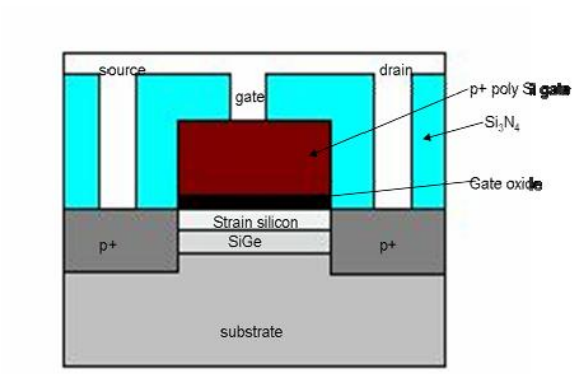

Fig. 1(a): The strain silicon PMOS device structure.

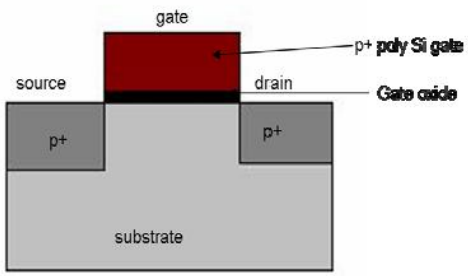

Fig. 1(b): The PMOS device structure.

The SSPMos structure is created with 0.0160µm gate oxide thickness and 0.71µm channel length. Meanwhile the conventional PMOS structure is created with 0.0091µm gate oxide thickness and 2.5µm channel length.

III. DEVICE DOPING PROFILE

Figure 2 shows the net doping and Ge concentration profile for the SSPMos. This is the result from the Athena simulation by performing a vertical cutline which starts at the gate and stops at the substrate. From Figure 2, we can see that the boron doping is high at the gate with 1 x 10^{20} cm^{-3} doping concentration. There is no doping in the silicon dioxide layer. Meanwhile the phosphorus doping at the strained silicon, SiGe layer and substrate is 1 x 10^{16} cm^{-3}. From the figure, the composition *x* shows a 0.35 of Ge concentration in silicon germanium layer only.

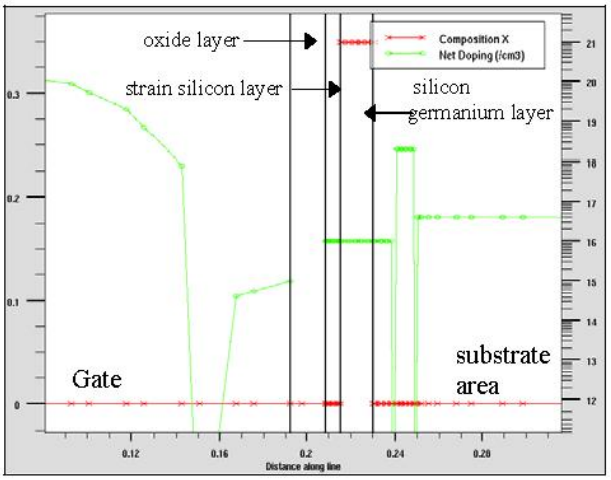

Fig. 2: The net doping and Ge concentration profile for SSPMos.

IV. ELECTRICAL CHARACTERIZATION

In device simulation, both the strained silicon structure and the conventional PMOS structure are simulated in Atlas. The devices are simulated to obtain the characteristics of the conventional PMOS and strained silicon PMOS (SSPMos). The mobility models that are used to obtain the electrical characteristics are the parallel electric field dependence and concentration dependent model. Beside that, the carrier static lifetime for the Si material is set at 1e-7 tau for electron and hole. Meanwhile the SiGe material is set to 1e-8 tau for electron and hole. For the carrier statistic model, the bandgap narrowing and Boltzman are chosen in this simulation. As for the recombination models, the auger and SRH concentration dependent lifetimes are chosen. The characteristics of the devices that was obtained from the simulation are the drain current versus gate voltage curve,

threshold voltage, drain induced barrier lowering (DIBL) and drain current versus drain voltage curve.

From the simulation, the drain current, I_d versus gate voltage, V_{gs} curve with a drain voltage, V_{ds} of -0.1V for both conventional PMOS and the SSPMos devices are shown in Figure 3. From Figure 3, it is obvious that the drain current for SSPMos structure is higher than conventional PMOS. This indicates that the SSPMos has higher drive current compared to conventional PMOS. Meanwhile the extracted threshold voltage parameters from Figure 3 are -0.511299V and -0.92902V for the SSPMos and conventional PMOS respectively. This indicates that the strained PMOS has lower voltage threshold than the conventional PMOS which translates to lower power consumption.

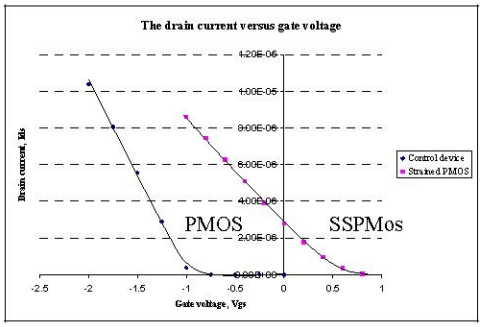

Fig. 3: The comparison of drain current versus gate voltage graph when V_{ds} is -1.0V.

Next, the drain induced barrier lowering, (DIBL) parameter is obtained from the difference between the threshold voltage divided by -2.8V. The DIBL for the strained PMOS is 0.3034V and the conventional PMOS is 0.4747V. The DIBL for the strained PMOS is smaller than the conventional PMOS. This shows that the strain silicon for PMOS is better compared to conventional PMOS.

Beside that, both structures are simulated to ramp the drain voltage, V_{ds} to -3.3V when the gate voltage, Vgs is bias to -1.1V, -2.2V and -3.3V. The simulation results are presented in Figure 4 which represents the graph of the drain current versus the drain voltage. From Figure 4, it can be seen that the strained PMOS device has a higher drive current compared to the conventional PMOS. From these results, it is evident that the strained silicon PMOS has a better drive current than conventional PMOS.

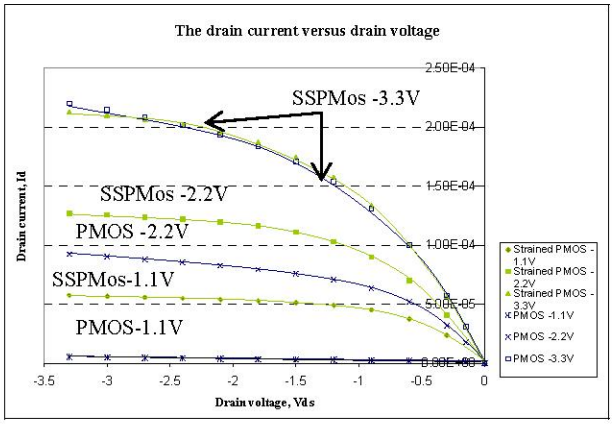

Fig. 4: The comparison of drain current versus drain voltage graph when V_{gs} is -1.1V,-2.2V and -3.3V.

V. Conclusion

From the results, it can be seen that the strained silicon has a better performance compared to the conventional PMOS even though the channel length for the strained silicon is larger than the conventional PMOS. This research will continue to study the electrical characteristics of the SSPMos such as the effective mobility enhancement. Further improvements and optimization will be done to the device performance in order to achieve a significant enhancement on MOSFET. Strained silicon is still considered as a new technology and more research is still needed to improve its implementation to the current technology.

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