Hardware Implementation of the High Frequency Link Inveter Using the dSPACE DS1104 Digital Signal Processing Board

Zainal Salam, *IEEE Member,* Toh Leong Soon *IEEE Student Member,* and Mohd. Zulkifli Ramli

Abstract - **In this paper, a detail description of a highly efficient and compact high frequency link inverter is given. The focus will be on the Deadbeat controller implementation using the dSPACE DS1104 Digital Signal Processing (DSP) board. In addition, other hardware components such as the gate drives, power circuit, control signals generation, signal conditioning and test-load banks is also described. Selected results from the experimental prototype will be presented.**

Index terms – High frequency inverter, high frequency transformer, pulse-width modulation[1]

I. INTRODUCTION

High frequency (HF) link inverters are widely used in uninterruptible power supply (UPS) and renewable energy sources applications[1]. Compared to the inverter that uses 50Hz isolation transformer, HF link inverter offers significant advantages in terms of compactness, weight and cost. Using high frequency isolation transformer, the converter size and weight can be drastically reduced.

In this work, we propose a highly efficient and compact bidirectional HF link inverter. With this topology, fewer switches are used, thus reduced switching losses. This paper provides description on hardware implementation of the prototype 1kVA inverter. The focus will be on the Deadbeat controller [2] implementation using the dSPACE DS1104 Digital Signal Processing (DSP) board. For completeness, other hardware components such as the gate drives, power circuit, control signals generation, signal conditioning and test-load banks is also described. Selected results from the experimental prototype will be presented.

II. POWER CIRCUIT TOPOLOGY.

The proposed HF link inverter power circuit is shown in Fig. 1. The timing diagrams of the key waveforms are illustrated in Fig. 2. There are basically three conversion stages: HF PWM bridge, active rectifier and polarity-reversing bridge. At the first stage, the HF PWM bridge converts the dc voltage into HF PWM voltage, v_{HF}. Then, the power is transferred to the second stage through the HF center-tapped transformer. At this stage, the HF PWM voltage will be rectified using a center-tapped active rectifier. The active rectifier enables bidirectional power flow. If the power is transferred from the source to the load, the diodes are utilized. If the power flows in the reverse direction, power switches S3 and $\overline{S3}$ are turned-on. The rectified PWM voltage, $v_{PWMrect}$, is then low-pass filtered to remove the high order harmonics and the rectified sinusoidal voltage, v_{rect} is obtained. Finally, using a polarity-reversing bridge, the second half of the rectified sinusoidal voltage waveform is inverted at zero-crossing, producing the sinusoidal output voltage, v_o.

Fig. 3 shows the timing diagram of the gate control signals. The PWM control signal for the HF PWM bridge, v_{pwm}, is produced by comparing a rectified sinusoidal modulating signal with a triangular carrier signal. The control signal v_s is used to control the power flow at the active rectifier stage. The frequency of v_s is half of v_{pwm}. The control signal for polarity-reversing bridge is denoted as v_u. Note that the polarity-reversing bridge is only operated at line-frequency (50Hz). The total number of power switches is reduced into ten, with only six switched at high frequency.

To achieve fast dynamic response, Deadbeat control technique is applied for closed-loop regulation of the inverter. The proposed Deadbeat controller sceme is illustrated in Fig. 4. It consists of inner current loop, outer voltage loop, and a feedforward controller.

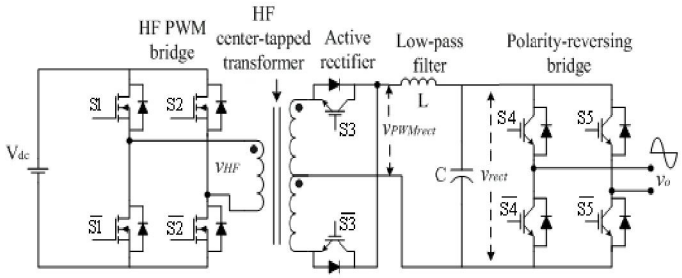

Fig. 1. The proposed bidirectional HF link inverter.

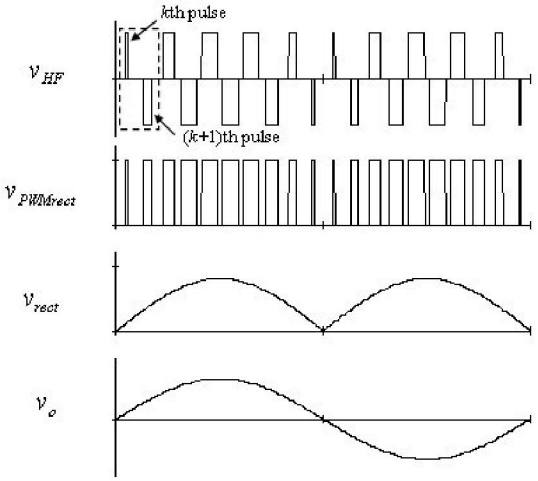

Fig. 2. Waveforms at conversion stages.

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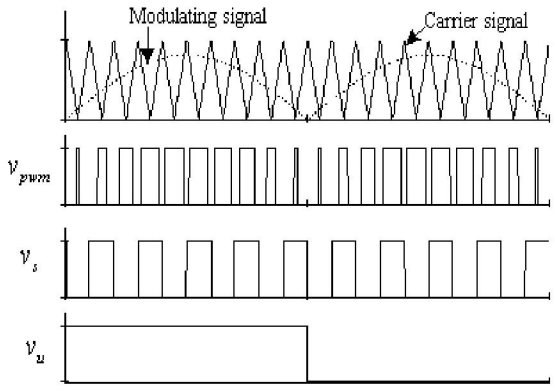


Fig 3. Gating signals

III HARDWARE IMPLEMENTATION

The block diagram of the overall system configuration is illustrated in Fig. 5. Details of each block will be described in the following subsections.

A. Power Circuit

The high-frequency PWM bridge is constructed using the APT15GP60BDF1 power IGBT. It is a low-loss switch with good switching capability. The transformer is wound on the ETD59 ferrite core. The switching frequency is set to be around 32KHz.The active rectifier's switches are built using the IRG4PH40K IGBT and STTA1212D ultrafast high voltage diode. These power switches can withstand 1200V. The polarity-reversing bridge is constructed using the IRG4PC40FD IGBT. Since the surge voltages on the transformer secondary have been dampened by the snubber before entering the polarity-reversing bridge, the chosen power switches are only rated at 600V. Using low voltage IGBT, the forward conduction losses can be minimised.

B Gate Drive Circuit

The gate drive circuit acts as interface between the gate control signals and the power switches. The isolated dc-dc converter, driven by the SG3526 pulse generator, produces a stable voltage supply for the gate driver. The miniature high-frequency transformer is designed such that there are two secondary centre-tapped windings. This ensures two units of gate drive power supply to be constructed with minimum components. The transformer is wound around the EFD12 core (3C90). The output from the transformer is set at $\pm 15V$ using LM78L15ACZ (+15V) and LM79L15ACZ (-15V) voltage regulators. Dead-time is necessary to provide protection against shoot-through fault of the inverter leg. Each power switch is driven by a Hewlett-Packard gate driver chip, HCPL3120. This chip has a built-in optocoupler with power output stage, suitable for driving medium power IGBT.

C. Feedback Circuit

Hall-effect sensors, i.e. the HY10-P current sensors, and LV25-P voltage sensor, are selected for feedback signals measurement. The Hall-effect sensors provide galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit). Furthermore, they are highly immune to external interference.

D Load Test-Rigs

To verify the performance of the controllers, the closed-loop inverter is tested under worst loading conditions. In practice, the triac in washing machines and rectifier in computer power supplies are among the critical loads. Hence, the triac load and full-bridge rectifier load test-rigs have been constructed for laboratory experiments.

E. DS1104 Digital Signal Processor Board

The DS1104 is a real-time digital signal processor board based on PowerPC technology (MPC8240 64-bit floating-point processor with PPC603e core running at 250MHz clock) [3]. It serves as a platform for rapid control prototyping. The DSP 1104 is used for feedback signal conditioning, implementing the control scheme and gate signal generation.

There are two ways of creating real-time applications for the DS1104 DSP. First is using the Real-Time Interface in MATLAB/Simulink environment. The other method is direct handcoding in C language. The handcoding method provides full access and control over the programming execution order. Furthermore, code optimisation can be performed if required. With these considerations, the control algorithm in this work is written using C code.

E1. Gate Signals Generation

There are three gate signals applied (as shown in Fig. 3) namely v_{pwm}, v_s and v_u. The v_{pwm} and v_u are generated using the PWM modulator in the slave DSP subsystem. As

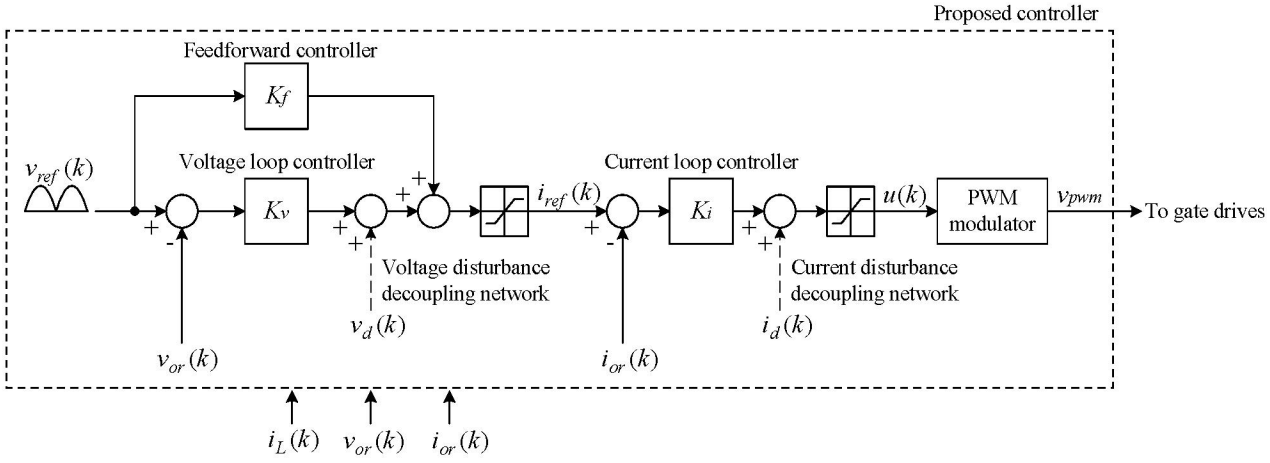
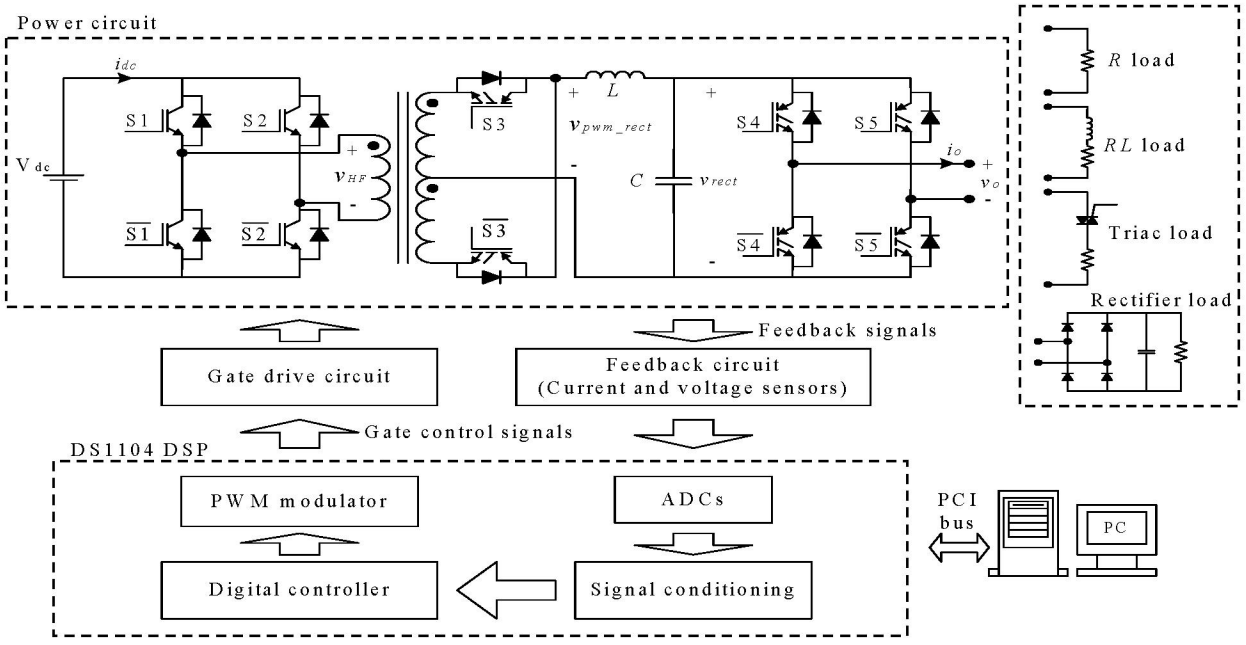


Fig 4: Proposed Deadbeat controller



the active rectifier's control signal v_s is half the frequency of v_{pwm}, it is generated using external frequency divider circuit. The frequency divider circuit is constructed using 74HCT112N JK flip-flop.

E2. Feedback Signal Conditioning

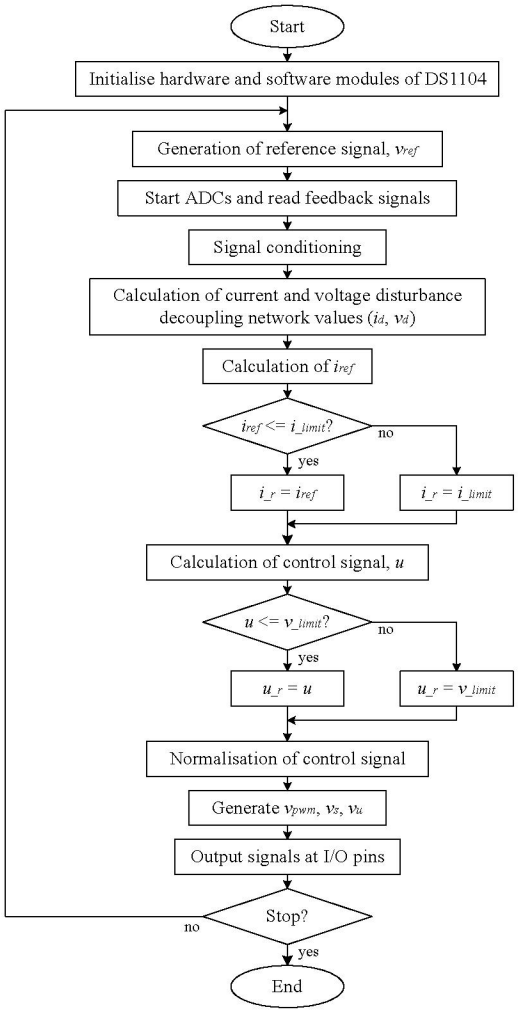
The feedback signals are sent into the DSP through the ADCs. There are two types of ADCs provided by DS1104, namely the 16-bit multiplexed ADCs (4 channels), and the 12-bit parallel ADCs (4 ADCs). This means five ADCs can be utilised simultaneously (1 x 16-bit + 4 x 12-bit). In this work, there are three feedback signals required, thus only the 12-bit parallel ADCs are used. In C code, to read the value at one ADC channel, the *ds1104_adc_read_ch* function is used. Before using the read function, the ADC must be started by means of *ds1104_adc_start* function. Both of these functions are placed in the timer's interrupt service routine. The feedback signals read by ADCs are sent through Infinite Impulse Response (IIR) digital filters for noise filtering. The IIR digital filters are designed using the bilinear transformation method.

E.3 Control Scheme

The PWM modulator in the slave DSP subsystem is used to generate the PWM signal for the controllers. In C code, this is performed by using the *ds1104_slave_dsp_pwm_duty_write* function, to set the PWM duty cycle for the related PWM channel. Prior to accessing the slave DSP, the communication between the master PowerPC (main processor) and slave DSP is initialised using the *ds1104_slave_dsp_communication_init* function. This initialisation function must be performed at the beginning of every application accessing the slave DSP features.

The enable signals for the input and output relays, gate drives, and snubber circuit, as well as the control signals for external frequency divider circuit, are generated using the digital I/O unit. In C code, single bits of the digital I/O unit can be set or cleared using the *ds1104_bit_io_set* and *ds1104_bit_io_clear* functions, respectively. At the main body of the program, the relevant digital I/O pins are initialised using the *ds1104_bit_io_init* function.

The proposed Deadbeat controller has been implemented. The flowchart below illustrates the algorithm for this controller. The algorithm is implemented in C code.



IV SELECTED RESULTS

Fig. 7 illustrates the simulation and experimental results of gating signals for the power switches. They are produced by the gate drive circuits through logical operations of the gate control signals. It can be seen that the voltage level of the gating signals have been stepped up to $\pm 15V$. This is to ensure the power switches are completely turn on/off.

Fig. 8 shows the performance of the digital filter using dS1104. The filter is tested by injecting high-frequency components (10KHz) to the fundamental signal. Fig.9 shows the test signal before and after the digital filter. From the results, it is clear that the high-frequency components have been filtered out by the digital filter to a negligible value.

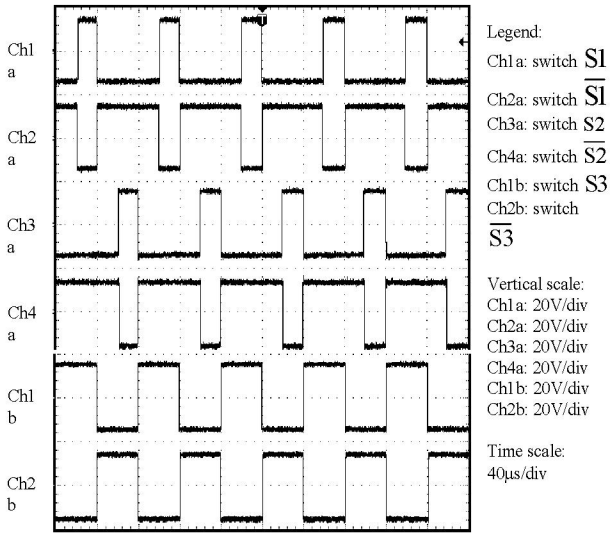


Fig. 7: Gating signals for power switches

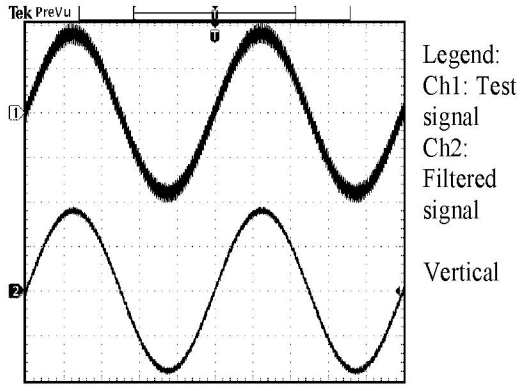


Fig. 8 : Test signal before and after digital filter. Vertical scale: output voltage 100V/div, output current 2A/div, Time scale: 4ms/div

Fig. 9 shows the output voltage waveform of the inverter under inductive load. As can be seen, the system is capable of carrying bidirectional power flow. The output voltage THD obtained is 2.2% . Fig. 10 shows the output waveforms under a step resistive load change. The voltage droop caused by the sudden load change can be recovered very quickly. The voltage transient can be reduced to 10% in about 0.32ms.

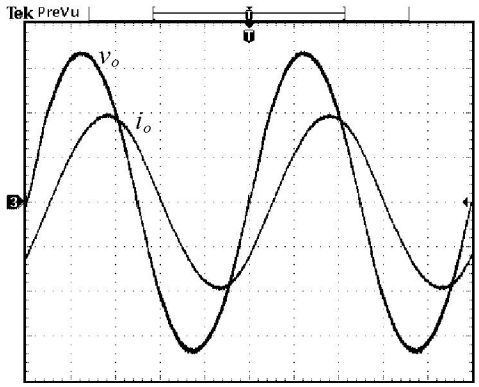


Fig. 9 : Output waveforms under inductive load. Vertical scale: output voltage 100V/div, output current 2A/div, Time scale: 4ms/div

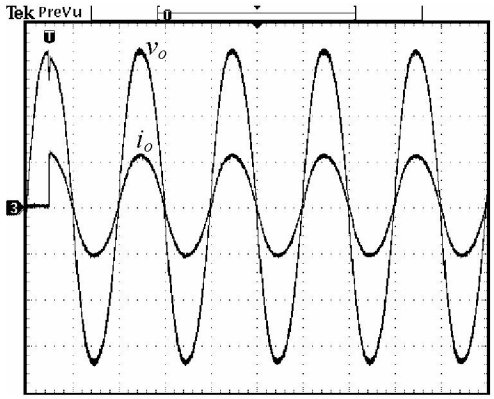


Fig. 10. Step response of the controller. Vertical scale: output voltage 100V/div, output current 2A/div, Time scale: 8ms/div

To test a worst case loading, the system is connected to a full-bridge rectifier. This type of load is considered to be the most severe type. It causes intense voltage distortion due to the highly distorted current. Fig. 10 shows the steady-state output waveforms under full-bridge rectifier load. As can be seen, the output voltage waveform has good quality without much distortion. The output voltage THD under this condition is 3.8%. This can be attributed to the improved robustness of the system.

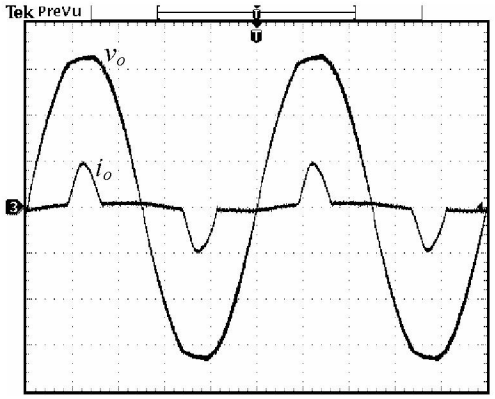


Fig. 10 Output waveforms under full-bridge rectifier load Vertical scale: output voltage 100V/div, output current 5A/div, Time scale: 4ms/div

Fig. 11 shows the measured efficiency of the inverter with resistive loads. It is observed that the

efficiency of the overall system is about 91%. Note that when the output power increases to 1kW, the inverter efficiency decreases to 90%. This can be attributed to the increased switching losses and the losses in the power transformer at high current operation.

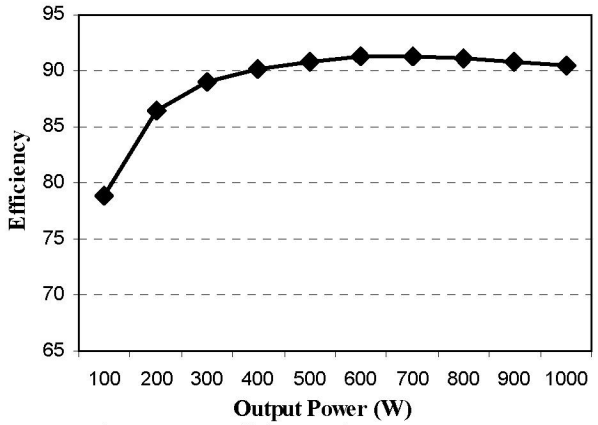


Fig. 11 Inverter efficiency against output power

V. CONCLUSIONS

This paper has described the design of a high-frequency link inverter based on the ds1104 DSP board. It is a compact, light-weight and low cost solution for dc/ac conversion. Using this topology, the number of power switches is reduced, thus increasing the overall system efficiency. The most important aspects of the design, i.e. the power circuit and the control algorithm have been described in detail. Other hardware components such as the gate drives, power circuit, control signals generation, signal conditioning and test-load banks is also described. Typical results from the experimental set-up are discussed.

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VII. REFERENCES

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VIII. BIOGRAPHIES

Zainal SALAM was born in Seremban, Malaysia in 1963. He received his secondary education from Victoria Institution, Kuala Lumpur. He obtained his B.Sc., M.E.E. and Ph.D. from the University of California, UTM and University of Birmingham, UK, in 1985, 1989 and 1997, respectively.

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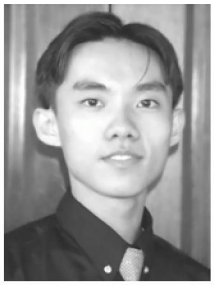

Leong Soon TOH was born in Penang, Malaysia in 1980. He received his secondary education from High School Bukit Mertajam, Penang. He received his B. Eng. (Electrical) and M. Eng (Electrical), both from Universiti Teknologi Malaysia in 2003 and 2006, respectively.

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