CHARACTERIZATION OF PLANAR AND VERTICAL N-CHANNEL MOSFET IN NANOMETER REGIME

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A project report submitted in partial fulfillment of the
requirements for the award of the degree of
Master of Engineering (Electrical – Electronics and Telecommunications)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

MAY 2007

"To my beloved family and friends, thanks for being there, throughout this journey"

ACKNOWLEDGEMENT

In the name of Allah, Most Merciful, Most Compassionate. It is by God's willing, I was able to complete this project within the time given. This project would not have been possible without the support of many people. Firstly, I would like to take this opportunity to thank my supervisor, Associate Professor Dr. Razali bin Ismail for his guidance, patience and support for me throughout the period of time in doing this project. My deepest gratitude also goes out to my examiners, Dr. Abu Khari A'ain and Dr Abdul Manaf for their constructive comments and suggestions in evaluating my project.

A very special thanks to my family and all my friends for always being there for me and giving their love and support when I most needed it. Lastly I would like to thank all staff and lecturers of Faculty of Electrical Engineering, Universiti Teknologi Malaysia for their help and support.

ABSTRACT

In recent years, there is more and more design on MOSFET that has been developed to fulfill the market need. This project focused on the comparison of planar and vertical n-channel MOS transistor characteristic with effective channel length of 100nm down to 50nm. Planar and vertical n-channel MOS transistors with effective channel length ranged from 50nm to 100nm has been developed. Simulation of the device design is done by using Silvaco-DevEdit. Short channel effect (SCE) is investigated through out the device simulation. SCEs affect on device and circuit performance in off-state leakage current and V_T roll-off. At the device simulation process, using Silvaco Atlas, the electrical parameter is extracted to investigate the device characteristic. Several design analysis are performed to investigate the effectiveness and robustness of the method in order to prevent the varying threshold voltage or short channel effect of a MOSFET device. A single channel vertical NMOS shows better V_T roll-off and better subthreshold swing at ~85mV/decade. On the other hand, planar NMOS has lower threshold voltage value which is suitable for low voltage devices. With these advantages from each NMOS analysis, one can decide which device to use to achieve required specification for specific usage in future.

ABSTRAK

Satu kajian telah dijalankan untuk membandingkan ciri-ciri antara MOSFET saluran-n jenis mendatar dan menegak. Setiap peranti mempunyai saluran efektif sepanjang 50nm hingga 100nm telah dibangunkan. Peranti telah direka menggunakan Slvaco-DevEdit. Kesan kurang sempurna dalam rekaan MOSFET seperti kesan saluran pendek telah dikaji. Kesan yang berlaku adalah seperti arus bocor dan kejatuhan voltan ambang. Pada simulasi peranti, menggunakan Silvaco-Atlas, parameter elektrikal telah diekstrak untuk megkaji ciri-ciri peranti. Beberapa analisa peranti dilakukan untuk menyiasat keberkesanan kaedah yang telah digunakan dalam mengurangkan perubahan voltan ambang atau kesan saluran pendek bagi sesebuah MOSFET. NMOS menegak bersaluran tunggal memperlihatkan kejatuhan voltan ambang yang lebih baik dan ayunan sub-ambang dalam lingkungan 85mV/dekad. Manakala, NMOS mendatar memiliki voltan ambang yang lebih rendah yang bersesuaian dengan peranti bervoltan rendah.

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LIST OF ABBREVIATION

ASB	-	Asymmetric Schottky barrier source/drain MOSFET
BTBT	-	Band-to-band tunneling
bVMOS	-	Vertical MOSFET with internal block layer
CMOS	-	Complementary MOS
CSB	-	Conventional Schottky Barrier MOSFET
DIBL	-	Drain induced barrier lowering
DITM	-	Drain-induced tunneling modulation
DOT	-	Drain on top
DT	-	Direct-tunneling
FILOX	-	Fillet local oxidation
GIDL	-	Gate-induced drain leakage
MOSFET	-	Metal-oxide semiconductor filed effect transistor
NMOS	-	N-channel MOSFET
PECVD	-	Plasma-enhanced chemical vapor deposition
PMOS	-	P-channel MOSFET
SCE	-	Short channel effect
SEG	-	Selective epitaxial growth
SOI	-	Silicon on insulator
SOT	-	Source on top

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CHAPTER 1

INTRODUCTION

This project uses Silvaco DevEdit and Atlas as a primary fabrication process and simulation tool. First part of the report will elaborate more on the project background and fabrication process will be discussed regarding the development of planar and vertical n-channel MOSFET. This chapter also mention on the objective and scope of the project.

1.1 Introduction

Future high performance devices for higher speed and lower power consumption would require active device dimensions in the sub-100 nm regime. Chip complexity, chip performance, feature size, and the numbers of transistors produced each year are a few of the parameters of the semiconductor industry that have changed exponentially over the last 50 years. The size reduction is in great improvement to MOSFET operation until the late 1990s with no deleterious consequences. The difficulties with decreasing the size of the MOSFET have always

been associated with the semiconductor device fabrication process. A steady path of constantly shrinking device geometries and increasing chip size has been followed by the integrated circuit industry for more than 30 years. This strategy has been driven by the increased performance that the smaller devices make possible and the increased functionality that larger chips provide.

Moore, one of the founders of Intel, observed in an article in the April 19, 1965 issue of Electronics magazine that innovations in technology would allow a doubling of the number of transistors in a given space every year (in an update article in 1975, Moore adjusted the rate to every two years to account for the growing complexity of chips), and that the speed of those transistors would increase. What is less well-known is that Moore also stated that manufacturing costs would dramatically drop as the technology advanced. Moore's prediction, now popularly known as Moore's Law, had some startling implications, predicting that computing technology would increase in value at the same time it would actually decrease in cost. This was an unusual idea at the time since, in a typical industry, building a faster, better widget with twice the functionality also usually means doubling the widget's cost. However, in the case of solid-state electronics, the opposite is true: Each time transistor size shrinks, integrated circuits (ICs) become cheaper and perform better.

There are two main reasons that smaller MOSFETs are desirable in today's world. First, smaller MOSFETs allow more current to pass and second, it has smaller gates, thus lower capacitance. These two factors bring to lower switching times and higher processing speeds. Logic gates incorporating smaller MOSFETs have less charge to move as smaller MOSFETs have lower gate capacitance and the amount of charge on a gate is proportional to its capacitance. There is another reason for scaled down MOSFETs, which is smaller MOSFETS can be packed more densely, resulting smaller chips and chips with more computing power in an area.

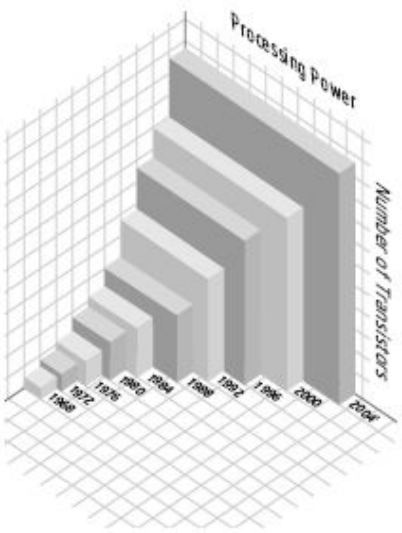

Figure1.1: Moore's Law on increasing performance

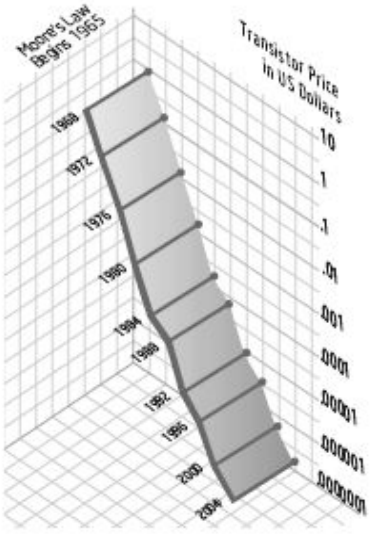

Figure 1.2: Moore's Law on decreasing cost

1.2 Objectives

The main objective of the project is to develop a planar and vertical n-channel MOSFET (NMOS) with a range of effective channel length of 100nm down to 50 nm. Many design aspects has to be considered when the MOSFET device is scaled down into deep submicron regime. Short channel effects will appear whenever the MOSFET device is scaled down and gate oxide has to be thin enough to increase the device performance.

The objectives of the study are listed as follows:

1. To develop planar and vertical n-channel MOSFET using TCAD.
2. To study the characteristic and to compare the performance between planar and vertical MOSFET.
3. To analyze planar and vertical NMOS in nanometer regime

1.3 Scope of Project

Basic design structure has been implemented in designing the device in this project. Generally, this project consists of two parts, which are the fabrication and the simulation process.

1) Process simulation

The process used to fabricate the planar and vertical NMOS transistor will be simulated using Silvaco-DevEdit. It is used to create the device structure, adding dopant, defining electrodes and creating the mesh. It uses an advanced mesh

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