SYNTHESIS AND MODELING OF RF INTEGRATED PLANAR SPIRAL INDUCTOR

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To my beloved parents, and Savior Jesus Christ.

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ABSTRACT

The recent development of the wireless market has increased the interest in the integrated inductor for Radio Frequency Integrated Chip (*RFIC*) applications. Though Electromagnetic (*EM*) simulation is available, it is usually expensive, slow and difficult to integrate into the *RFIC* design flow. Therefore, the alternative option of a generic, simple yet accurate procedure to design the inductor is very desirable. Based on the physical model, an integrated inductor synthesis procedure has been developed and implemented in Microsoft EXCEL. This synthesis tool is able to identify the maximum quality factor (*Q*) at the operating frequency (e.g. 1.8 GHz for mobile communication, 2.45 GHz for wireless Local Area Network (LAN)) of the desired inductor very quickly. An example of synthesizing a 3 nH inductor is demonstrated using this tool. Besides that, another type of integrated inductor model known as extracted model is also needed for circuit simulation. An improved model extraction procedure has been proposed in this research and has been embedded in another EXCEL file. This new procedure has reduced the number of terms required and proved to be more accurate even in the region beyond the Self-Resonant Frequency (*SRF*). The above two types of integrated inductor modeling were then "combined" into a new global integrated inductor model in SPICE, which is a compromise of accuracy (extracted model) and scalability (physical model). This model is accurate up to ~2 GHz, within an average error of 10 %. Using this new model, one can have the freedom to choose the value of inductance and more flexibility in circuit design. In addition, the layout optimization and circuit optimization can be done using the same model thus saving time and reducing cost. This is a novel integrated type of model that has never been published in any other research.

ABSTRAK

Perkembangan terkini pasaran tanpa wayar telah meningkatkan minat terhadap induktor bersepadu untuk aplikasi litar bersepadu frekuensi radio (*RFIC*). Walaupun tedapat simulasi elektromagnet (*EM*), ini biasanya mahal, lambat dan susah diimplementasi dalam aliran rekabentuk *RFIC*. Oleh itu, pilihan alternatif tatacara tepat yang generik tetapi mudah sangat diperlukan. Tatacara sintesis induktor bersepadu berasaskan model fizikal telah dibangunkan dan diimplemen menggunakan EXCEL. Alatan sintesis ini berupaya menentukan faktor kualiti (*Q*) optimum dengan pantas pada frekuensi operasinya (seperti 1.8 GHz untuk telekomunikasi bergerak dan 2.45 GHz untuk rangkaian kawasan tempatan (LAN) tanpa wayar). Satu contoh untuk sintesis induktor 3 nH ditunjukkan menggunakan alatan ini. Selain itu, model induktor bersepadu yang dikenali sebagai model terekstrak juga dibangunkan untuk simulasi litar. Tatacara pengekstrakan model yang telah diperbaiki dicadangkan dalam kajian ini dan dimasukkan ke dalam satu lagi fail EXCEL. Tatacara baru ini telah berjaya mengurangkan beberapa sebutan dan terbukti lebih tepat walaupun dalam julat frekuensi selepas frekuensi resonan diri (*SRF*). Kedua-dua jenis model induktor ini telah “digabung” untuk menghasilkan model induktor global dalam bentuk SPICE, yang merupakan krompomi di antara ketepatan (model terekstrak) dan kebolehskalaan (model fizikal). Model ini mempunyai ralat dalam lingkungan 10 %, tepat sehingga ~2.0 GHz. Dengan menggunakan model baru ini, seseorang boleh mengawal nilai induktan yang memberikan fleksibiliti rekabentuk litar. Tambahan pula, pengoptimuman bentangan dan pengoptimuman litar boleh dilakukan dengan model yang sama, seterusnya dapat menjimatkan masa dan mengurangkan kosnya. Ini merupakan model bersepadu baru yang belum pernah dilaporkan dalam kajian lain

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LIST OF ABBREVIATIONS

A	:	Ampere
Al	:	Aluminum
ASITIC	:	Analysis and Simulation of Spiral Inductor and Transformer for ICs
BPF	:	Band bass filter
CMOS	:	Complementary metal oxide silicon
DC	:	Direct current
DOE	:	design of experiment
EM	:	Electromagnetic
F	:	Farad
f_{max}	:	Maximum frequency
f_t	:	Cut-off frequency
GaAs	:	Gallium arsenide
GHz	:	Giga-hertz
GIIM	:	Global integrated inductor model
GMD	:	geometric mean distance
G-S-G	:	Ground-signal-ground probe pad
H	:	Henry
Hz	:	Hertz
IC	:	Integrated circuit
IP3	:	3^{rd} order intercept point
LC	:	Inductor, Capacitor
LNA	:	Low noise amplifier
LPF	:	Low pass filter
LRRM	:	Line-Reflect (open)-Reflect (short)-Match
LTCC	:	Low temperature co-fired ceramic
MOS	:	Metal on silicon

nH	:	Nano-Henry
PEEC	:	Partial element equivalent circuit
RF	:	Radio frequency
RFIC	:	Radio frequency Integrated Circuit
Si	:	Silicon
SISP	:	Spiral Inductor Simulation Tool
S-parameter	:	Scattering parameter
SPICE	:	General purpose circuit simulation program
SRF	:	Self-resonant frequency
VCO	:	Voltage controlled oscillator
vs.	:	Versus
Wb	:	Weber
µm	:	Micro-meter

LIST OF SYMBOLS

A	:	Voltage ratio when port 2 is open;
a	:	1st dimension of a rectangular in Greenhouse expression
a_1	:	Incident electromagnetic waves at port 1
a_2	:	Incident electromagnetic waves at port 2
B	:	Transfer impedance when port 2 is short-circuited;
b	:	2nd dimension of a rectangular in Greenhouse expression
b_1	:	Reflected electromagnetic waves at port 1
b_2	:	Reflected electromagnetic waves at port 2
C	:	Transfer admittance when port 2 is open;
C_1	:	Mohan's current sheet approximation 1st layout dependent coefficient
C_2	:	Mohan's current sheet approximation 2nd layout dependent coefficient
C_3	:	Mohan's current sheet approximation 3rd layout dependent coefficient
C_4	:	Mohan's current sheet approximation 4th layout dependent coefficient
C_{f1}	:	1st intermediate capacitance
C_{f2}	:	2nd intermediate capacitance
C_{ox}	:	Oxide capacitance
C_s	:	Series capacitance
C_{si}	:	Silicon substrate capacitance
C_{sub}	:	Capacitance per unit area
D	:	Current ratio when port 2 is short circuit.
d^+	:	average distance
d_1	:	Length of 1st line of two parallel lines
d_2	:	Length of 2nd line of two parallel lines
d_{avg}	:	Average diameter
D_{in}	:	Inner diameter
D_{out}	:	Outer diameter

d_s	:	intermediate diameter
G_{sub}	:	Conductance per unit area
h_{11}	:	Impedance seen looking into port 1 when port 2 is short-circuited;
h_{12}	:	Voltage ratio when port 1 is open;
h_{21}	:	Current ratio when port 2 is short-circuited;
h_{22}	:	Admittance seen looking into port 2 when port 1 is open.
I	:	Electric current
I_1	:	Applied current source at port 1
I_2	:	Applied current source at port 2
K	:	relative dielectric constant
K_1	:	Mohan's modified Wheeler 1st layout dependent coefficient
K_2	:	Mohan's modified Wheeler 2nd layout dependent coefficient
L	:	Inductance
l	:	Inductor length
L_{gmd}	:	Mohan's current sheet approximation inductance expression
L_{GMD2}	:	Greenhouse's inductance expression
L_{meas}	:	Measured inductance
L_{mon}	:	Mohan's monomial data fit inductance expression
L_{mwhe}	:	Mohan's modified Wheeler inductance expression
$L_{newphysics}$	:	Asgaran's new physics closed form inductance expression
$L_{physics}$	:	Jenei's physics closed form inductance expression
L_s	:	Series inductance
L_{self}	:	Self-inductance
L_{stot}	:	Self-inductance (Based on Asgaran's expression)
M^-	:	Negative mutual inductance
M^+	:	Positive mutual inductance
N	:	Integer part of n
n	:	Number of spiral inductor turns
P	:	Double factorial parameter in Asgaran's new physics expression.
Q	:	Quality
Q_i	:	Mutual inductance parameter
R_s	:	Series resistance

R_{si}	:	Silicon substrate resistance
R_{sk}	:	Resistance that have current crowding effects
R_{δ}	:	Resistance that have substrate current effects
s	:	Spacing between spiral inductor
S_{11}	:	Input reflection coefficients
S_{12}	:	Reverse transmission coefficients
S_{21}	:	Forward transmission coefficients
S_{22}	:	Output reflection coefficients
t	:	Inductor metal thickness
t_{ox}	:	Oxide thickness
V_1	:	Applied voltage at port 1
V_2	:	Applied voltage at port 2
w	:	Spiral inductor width
Y_{11}	:	Admittance seen looking into port 1 when port 2 is short-circuit
Y_{12}	:	Transfer admittance when port 1 is short-circuit;
Y_{21}	:	Transfer admittance when port 2 is short-circuited;
Y_{22}	:	Admittance seen looking into port 2 when port 1 is short-circuited.
Z_{11}	:	Impedance seen looking into port 1 when port 2 is open
Z_{12}	:	Transfer impedance when port 1 is open
Z_{21}	:	Transfer impedance when port 2 is open
Z_{22}	:	Impedance seen looking into port 2 when port 1 is open.
Z_{in}	:	input impedance
Z_o	:	Intrinsic impedance
M_{tot}^{-}	:	Asgaran's negative mutual inductance
M_{tot}^{+}	:	Asgaran's positive mutual inductance
t_{eff}	:	Effective thickness
$t_{oxM1-M2}$	:	Oxide thickness between the spiral metal and underpass metal
ε_{ox}	:	Oxide dielectric constant
δ	:	Skin depth
ϕ	:	Fill ratio

$\alpha 1$	:	monomial data fit coefficient for outer diameter
$\alpha 2$	:	monomial data fit coefficient for width
$\alpha 3$	:	monomial data fit coefficient for average diameter
$\alpha 4$	:	monomial data fit coefficient for number of turns
$\alpha 5$	:	monomial data fit coefficient for spacing
β	:	beta, monomial data fit coefficient
γ	:	propagation constant
μ	:	Permeability
μ_o	:	Free space permeability
π	:	22/7
ρ	:	Resistivity
σ_{Al}	:	Aluminum conductivity
σ_{Au}	:	Gold conductivity
σ_{Cu}	:	Copper conductivity
Φ	:	Magnetic flux
ω	:	radian frequency, rad/s
Ω	:	Unit of resistivity, ohm

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Chapter I

INTRODUCTION

The demand of consumer products such as the mobile phone, personal digital assistant or mobile computer with wireless feature has seen a tremendous growth recently. This has created a stronger demand for low cost, low power consumption, high volume implementation of radio frequency (*RF*) functions in consumer products.

Most of the current radio frequency integrated circuits (*RFIC*) are implemented in the matured Gallium Arsenide (GaAs) technology. However, the complementary metal-oxide-silicon (*CMOS*) process, which is currently in high volume production for digital signal processors, is also emerging as one of the options for *RFIC*s [Larson, 1998]. The latest research development in the *CMOS* technology has seen an increasing effort to migrate the *RF* applications onto the silicon (*Si*) process. Following this trend, higher level of integration of *RF*, analog and digital circuits using the conventional or innovative methods in *CMOS* process are expected to happen in the near future [Burghartz, 1997].

Previously, inductors were not considered as standard components, such as transistors, resistors or capacitors where models are included in the standard technology library. However, the demands for inductors models are increasing, as *RF* circuits on *Si* with acceptable performance are now feasible [Chan, *et al.*, 2001] [Wang, *et al.* 2002][Steyaert, *et al.* 2000]. Inductor models that are able to predict the behavior of inductor over a broad range of frequency are important for circuit simulation and layout optimization. Thus has arisen the need to develop a generic procedure that is able to produce good inductor models for *RFIC* applications.

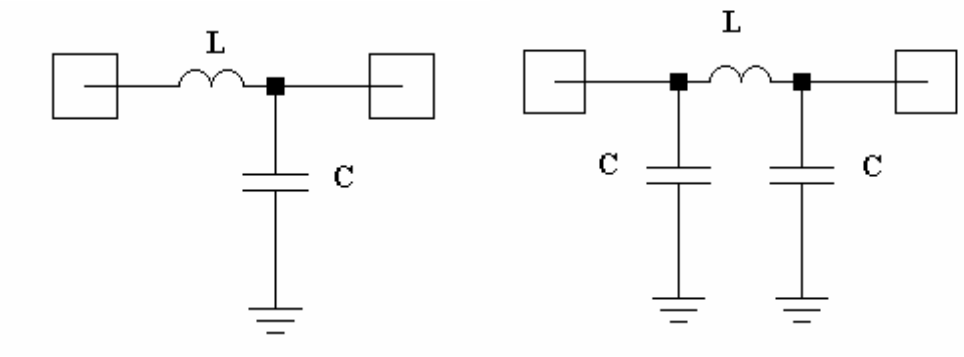
1.1. Research Background

As the *CMOS* technology continue to scale down to its next technology node, the performance of the transistor continue to improve, in term of cut-off frequency (f_t) and maximum frequency (f_{max}). For example, f_t for 0.18μm is reaching 50GHz, which allows for *RF* applications operating below 10GHz. Nevertheless, there are still some performance issues need to be solved, especially when the bottle neck passive element, the inductor, is included in *CMOS* process. In the next two sub-sections, the inductor's application, the issues due to the physical structure of the inductor in *CMOS* process and the motivation in this research will be discussed.

a.) Inductor's Application In *RF* Design

The inductor is an indispensable part of many *RF* circuit block. One of the applications of inductors is found in impedance matching. In *RF* systems, impedance matching is critical to ensure maximum power transfer from one circuit block to another circuit block when two circuit blocks are cascaded. Maximum

power transfer is obtained when the output resistance is equal to the input resistance and the output reactive parts are conjugated with the input reactive parts. The inductor is used as one of the components in the impedance-transforming network, such as the *LC* and π networks shown in Figure 1.1



(a) (b)

Figure 1.1: Typical impedance matching networks (a) *LC*-Network (b) π-Network

Besides that, inductors are also used in the design of the amplifier as tuned load, feedback circuit and shunt peaking element. Figure 1.2 shows the use of inductor as the shunt peaking element to extend the bandwidth of amplifier. Inductors are used as the feed back circuit in a mixer as shown in Figure 1.3. In Figure 1.4, the spiral inductor acted as an integral part of the switched resonator in a dual band monolithic *CMOS* voltage controlled oscillator.

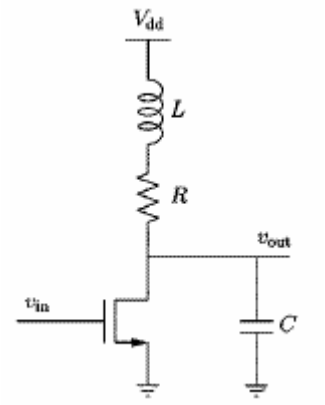


Figure 1.2: Shunt peaking in a common source amplifier [Mohan, *et al.*, 2000]

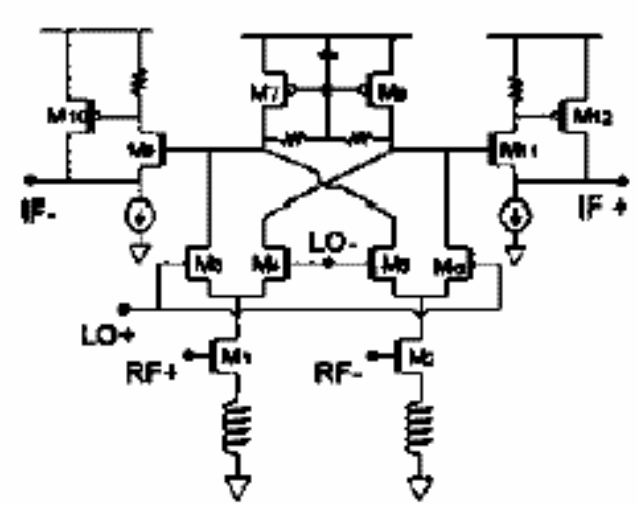


Figure 1.3: Schematic of mixer [Wang, *et al.*, 2002]

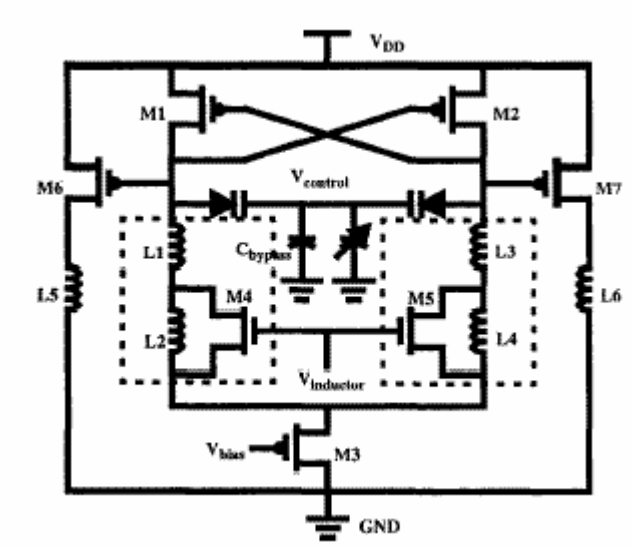


Figure 1.4: Schematic of a dual-band *VCO* [Yim, *et al.* ,2001]

The quality (*Q*) factor of the *CMOS* inductor is generally very low, around 8 to 15, which is not suitable for filter that requires high *Q* passive elements. Nevertheless, if the inductor is combined with transistor, the *Q* of the inductor can be drastically improved. In this case, the transistor acted as the negative resistance generator, which will reduce the real portion of the impedance of the inductor when connected to the transistor and thus increased the *Q*. This is then enabled the on-chip

inductors to be used to implement the *RF* filters, for example the band pass filter as shown in figure 1.5 [Sooranpanth and Wong, 2001].

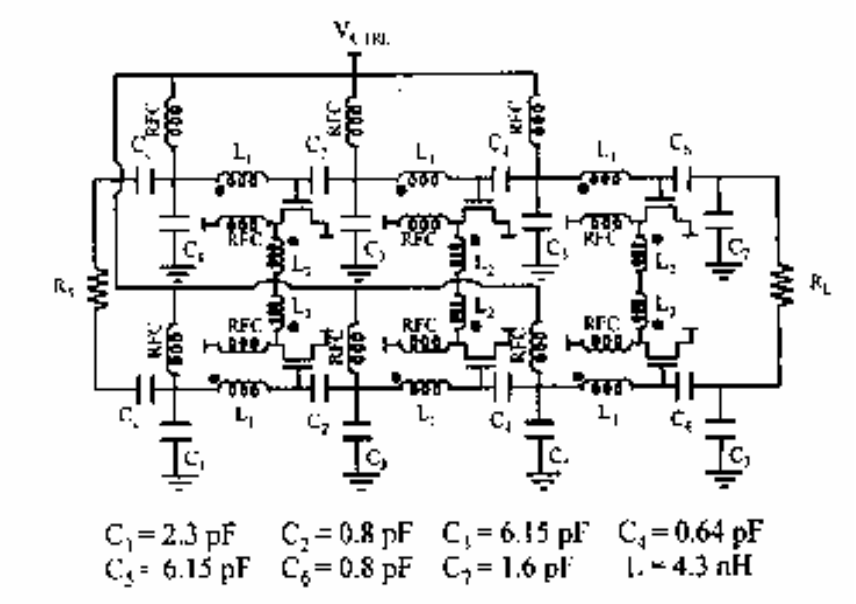


Figure 1.5 : 2140±30 MHz, 3rd order Chebyshev filter [Sooranpanth and Wong, 2001].

b.) Inductor On Silicon

Researchers are investigating the possibility in migrating the expensive GaAs process to the cheaper *Si IC* technology for *RF* applications. Inductor is one of the key devices in such an investigation. Unlike other devices, such as the capacitors and the transistors, the integrated inductor is relatively "new" in *RFIC*. Previously, the inductor is either realized off-chip or bond-wire. This has made the whole circuit to become bulky, difficult to control (for the case of bond-wire), less integrated and thus more expensive. The integrated inductors in *CMOS* usually have lower *Q*

factor, in the order 5 to 15, compared to capacitors, which are usually in the order of few hundreds in 1 to 2 GHz range.

A typical IC process in 0.18μm *CMOS* technology has six layers of Aluminum (*Al*) interconnects, as shown in Figure 1.6 shows the cross-sectional view of six layer metal in *CMOS* process. At the first glance, some may think that the inductor can be fabricated using any of the six layers. However, in reality, it is usually only the top layer or only a few layers at the top are used. Inductor on *Si* substrate suffers a few intrinsic *Q* limiting factors.

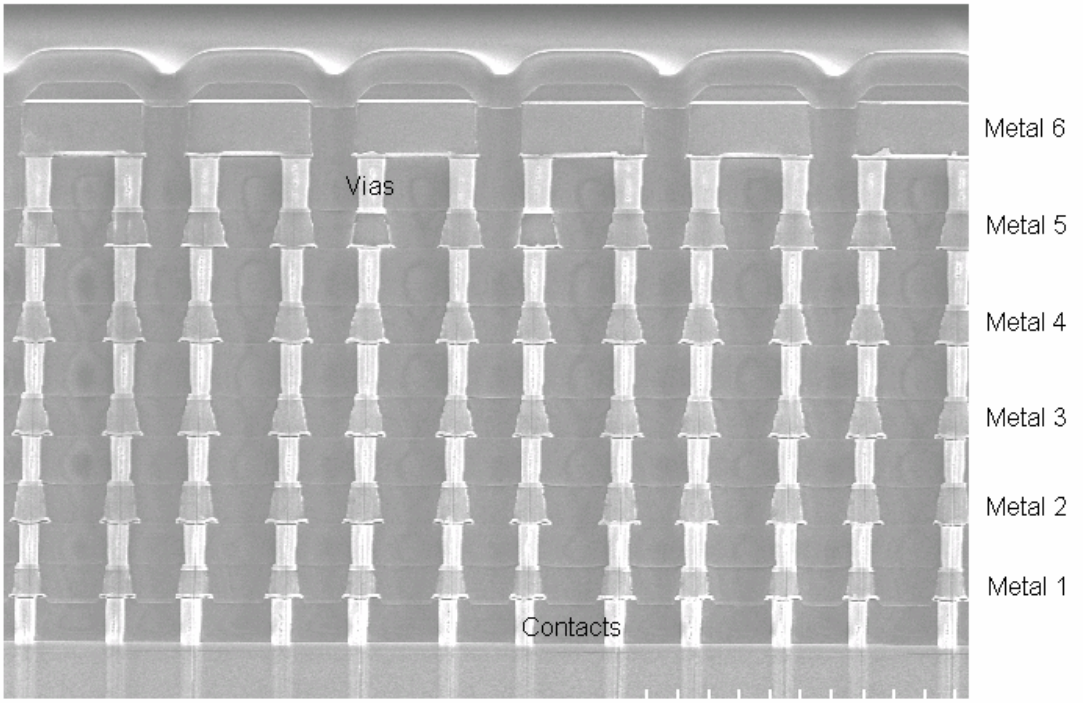


Figure 1.6: Cross-section of metal 6 layers aluminum metal in a typical *IC* process

Inductors are formed on the top metal to reduce the parasitic capacitance of the inductor. For example, to fabricate the circular spiral shown in Figure 1.7, metal 6 is used to draw the circular spiral inductor and metal 5 is used to draw the underpass metal.

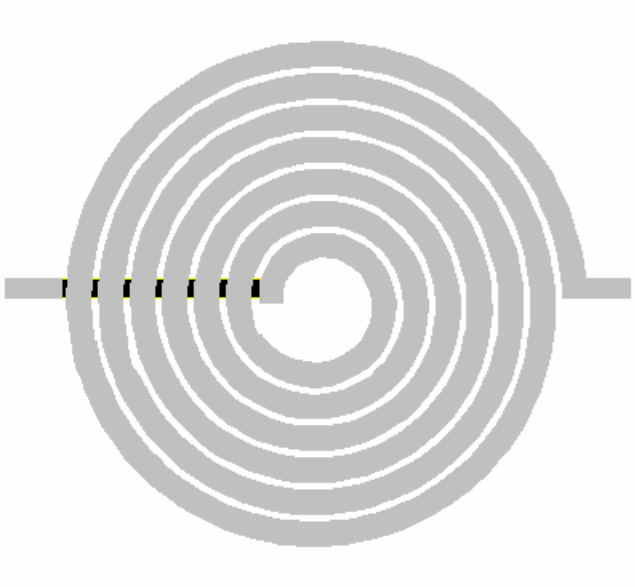


Figure 1.7: Circular spiral inductor

Most of the *IC* manufacturers, which are the foundries, also offer thicker top metal option for the construction of inductor, in 0.18 μm *CMOS* analog process, top metal (Aluminum) thickness is 2 μm, resulting the sheet resistance, around 15 mΩ/□ (mili-Siemen per square) [Keating, *et al.*, 2002]. Other metal layer, such as metal 5 and below, the metal thickness is more than 50% thinner. Higher resistances are expected for these metals and it is therefore going to cause the increase of the metal loss and subsequently decrease the *Q*-factor.

At higher frequencies, current crowding due to two effects, namely the skin effects and proximity effects. These effects will cause an uneven current distribution in the metal. In the skin effects, the center portion of the conductor will be enveloped by a greater magnetic flux than those on the outside. Consequently the self induced back electromagnetic flux will be greater towards the center of the conductor, thus causing the current density to be less at the center than the conductor surface. This extra concentration at the surface results in an increase in the effective resistance of the conductor as the frequency increases.

As for the proximity effects, it happens when there are two conductors arranged close proximity to one another, which is usually the case in the spiral inductor design. The proximity effect is associated with the magnetic fields of two conductors, which are close together. If each carries a current in the same direction, the halves of the conductors in close proximity are cut by more magnetic flux than the remote halves. Consequently the current distribution is not even throughout the cross-section, a greater proportion being carried by the remote halves. If the currents are in opposite directions, the halves in close proximity will carry the greater density of current.

In addition to resistance loss there is also substrate loss. In *CMOS* process, typically low resistivity substrate is used to prevent latch up in transistor, typically 10 Ohm-cm in p-type *Si* substrate as opposed to semi-insulating material in GaAs. This conductive nature of the *Si* substrate leads to two loss mechanisms. Firstly, the conductive nature of the *Si* substrate is causing capacitive current to flow to the nearby ground. The substrate is usually tied to a ground, and there is a potential difference between the inductor and the ground. A capacitive-like structure will exists between the inductor plane and ground and will cause capacitive coupling loss. Secondly, the eddy current is induced from the time-varying magnetic fields (from the inductor) and penetrates the substrate to ground.[Niknejad and Meyer, 2000].

The spiral inductor on *Si* substrate does not perform as good as the spiral inductor on high resistance substrate, such as in organic substrate or ceramic substrate. However, the idea of system-on-chip or application-on-chip that leads to very high integration *IC* design is pushing the industry toward implementation of inductor on *CMOS* process. *CMOS* process is relatively cheaper process compared to other process. With the advantage of current mature and mass production process, *RF* applications in *CMOS* process is a hot topic for *RFIC* world. Therefore, many researchers have begun to find ways to improve the inductor performance on *Si* substrate, such as introducing the lower resistance material, for example the copper interconnect; using shields to reduce the eddy current in the substrate; micromachining to remove the conductive substrate, and etc. All these efforts are

trying to integrate the *RF* section into the existing digital section on chip. Looking at the current research activities trend, the production of a full *RF* system build on *Si* substrate is coming nearer at our doorstep.

1.2 Objectives and scopes of research

The main objective of this research is to meet the needs of the coming implementation of integrated inductor in *CMOS* process. It is to provide know-how knowledge in the synthesis and modeling of integrated inductor. The inductor model will be developed and readied before the implementation of inductor application on *CMOS* process. Hence, the scopes of this research are to study and develop a generic procedure of both inductor synthesis and inductor modeling. The products of this research will include a simple and easy implementation of inductor synthesis and an extraction, optimization procedure for integrated inductor.

1.3 Thesis Organization

Chapter I presents the introductions of this research work, which includes the research background, research objectives and scope of research. Chapter II presents the discussions of previous works from literatures. The rest of the chapters cover three main parts of this thesis, the first part is devoted to the *RF* integrated planar spiral inductor synthesis. The focus of chapter III is on the physical model and the synthesis of planar spiral inductor. The details of the physical model of the inductor are reviewed. Comparisons of a few inductance expressions for square inductor are done. The most accurate closed form inductance expression is identified and described in this work. The optimum inductor design with the help of the contour

plot of *Q* is described. An example on synthesizing an inductor for 3nH is shown. The second part of the thesis is on the modeling and optimization of integrated spiral inductor, which is covered in Chapter IV. In this chapter, it is presented a new proposed model extraction procedure. The improvements of the new proposed method are highlighted. A generic model optimization methodology is included in this chapter. One of the wide-band modeling methods is also discussed. The third part describes a new global integrated inductor model. Chapter V presents a break through in inductor modeling. The physical modeling and extraction modeling are combined and produced the global integrated inductor model (*GIIM*). Chapter VI concludes the thesis. Recommendations and suggestions for future work are presented.