Modeling and Analysis of Ballistic Carbon Nanotube Field Effect Transistor (CNTFET) with Quantum Transport Concept

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To my beloved father, mother and sister.

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ABSTRACT

Aggressive scaling of CMOS has led to higher and higher integration density, the higher performance of devices, low power consumption and more complex function. However, it will eventually reach its limit in future. As device sizes approach the nanoscale, new opportunities arise from harnessing the physical and chemical properties at the nanoscale. Carbon Nanotubes are considered as the most promising carbon nanostructure material is realizing the nanoelectronic transistors back in year 1991. The objective of this project is to create a modeling of next generation field effect transistors (CNTFET) to model the characteristics of the devices. Modeling of semiconductor devices is critical in understanding factors which may affect their performance. This allows greater understanding of the underlying physics and aids optimization in both materials and lowers development costs by reducing the time and effect between design and fabrication of working prototypes. The overall project is uses the concept of a Carbon Nanotube technology along with its application in Carbon Nanotube field effect transistors, physic of Carbon Nanotube, and quantum transport theory to create an equivalent universal SPICE model. Numerical simulation studies are carried out by using MATLAB program to understand the device physic and the performances of transistor are compared with conventional MOSFET. Further analysis has been made on changing some transistor parameter (for example the oxide thickness, carbon nanotube diameter and etc) to further understand what controls and how to improve the transistor performance.

ABSTRAK

Pengskalaan peranti CMOS yang agresif terhadap skala nano telah membawa kepada peningkatan pelbagi faktor termasuk densiti integrasi, pencapaian prestasi peranti, kompleksiti fungsi dan penurunan kadar pengunaan kuasa. Akan tetapi, fenomena ini akan mencapai tahap di mana pengecilan skala tidak dapat lagi dijalankan. Pengecilan saiz peranti terhadap skala nano telah membangkitkan kaedah-kaedah untuk menaikkan lagi prestasi pada tahap skala nano secara fizikal and kimia. Nanotiub karbon dianggap sebagai bahan struktur nano yang terbaik dalam usaha merealisasikan transistor nanoelektronik pada tahun 1991. Objektif projek ini adalah untuk memodelkan ciri-ciri peranti transistor karbon nanotiub kesan medan generasi baru CNTFET. Pemahaman yang mendalam terhadap faktor-faktor adalah kritikal dalam pemodelan peranti semikonduktor yang mungkin mengubah tahap prestasi peranti tersebut. Dengan ini, pemahaman yang lebih mendalam dalam bidang fizik dan pengoptimasi bantuan dalam bahan dapat dicapai di samping mengurangkan kos dengan mengurangkan masa dan kesan di antara rekabentuk dan fabrikasi prototaip. Secara keseluruhan, projek ini menggunakan konsep teknologi karbon nanotiub dalam pengaplikasian dalam transistor karbon nanotiub kesan medan, sifat fizik karbon nanotiub dan teori kuantum pengangkutan untuk menghasilkan model SPICE yang setara. Simulasi telah dijalankan dalam MATLAB untuk memahami dengan dalam sifat fizik dan tahap pencapaian transistor berbanding MOSFET konvensional. Analisis yang lebih lanjut telah dijalankan dengan penukaran parameter transistor contohnya ketebalan oksida, diameter nanotiub karbon dan lain-lain untuk menyelidik faktor yang mengawal dan juga cara-cara yang dilakukan untuk meningkatkan tahap prestasi transistor.

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U_{sc}	Self-consistent potential at top barrier
q	Electronic charge
h	Planck's constant (eV-s)
I_D	Drain current
I_{on}	On-current
I_{off}	Leakage current
k_B	Boltzman's constant (eV/K)
E	Fermi level
T	Operating Temperature
H	Hamiltonian matrix
E_0	Permittivity of free space
m	Free electron mass
ρ	Density matrix

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CHAPTER 1

INTRODUCTION

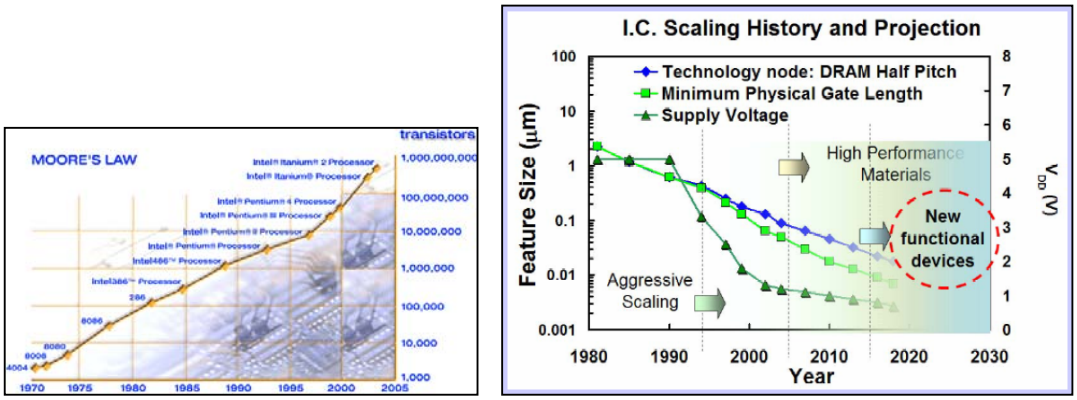
This project proposes a ballistic carbon nanotube field effect transistor modeling with applying quantum transport concept and analyzing the output of the transfer characteristic (I-V characteristic) with different parameter on input and comparing the result with conventional MOSFET. In this chapter, we will present the background and research motivation, scopes of project. The chapter will end with outline of the project report.

1.1 Background and Research Motivation

The progress in silicon technology continues to outpace the historic pace of Moore's Law, but the end of device scaling now seems to be only 10-15 years away. Therefore, it is of intense interest to find new, molecular-scale devices that might complement a basic silicon platform by providing it with new capabilities - or that might even replace existing silicon technology and allow device scaling to continue to the atomic scale. As device sizes approach the nanoscale, new opportunities arise from harnessing the physical and chemical properties at the nanoscale. Chemical

synthesis, self-assembly, and template self-assembly promise the precise fabrication of device structures or even the entire functional entity. Quantum phenomena and dimensional transport may lead to new functional devices with very different power/performance tradeoffs. New materials with novel electronic, optical, and mechanical properties emerge as a result of the ability to manipulate matter on a nanoscale. It is now feasible to contemplate new nanoelectronic systems based on new devices with completely new system architectures, for examples: - nanotubes, anowires, molecular devices, and novel device concepts for nanoelectronics.

Of the various material systems and structures studied so far, carbon nanotubes have shown particular promise owing to their nanoscale size and unique electronic properties. Recently carbon nanotube field effect transistors (CNTFETs) have been fabricated successfully. It is reported that they have shown better performance than present silicon transistors of equivalent size.



(a) (b)

Fig 1.1: (a) Moore's Law and (b) IC technology projection.

As the MOSFET gate length enters nanometer scale, however, short channel effect such as threshold voltage roll-off and drain-induced-barrier-lowering (DIBL) [1, 2] become increasingly significant, which limits the scaling capability of planar bulk or silicon-on-insulator (SOI) MOSFET. Several leakage current mechanisms in MOSFET such as reverse-bias p-n junction current, weak inversion current and drain induced barrier lowering (DIBL) current [3] are being introduced by short-channel

effect. Tunnelling effect in nano scale MOSFET is also impacting the performance of the transistor. Normally the separation between 2 transistors is made by inserting material that acts as a barrier. However, come to nano-scale transistor the transistor size and the distance between 2 transistor is also been scaled down, it cause the carries of 1 MOSFET cross the barrier and effect to another MOSFET are close to it. The tunnelling effect increasing exponentially as the barrier distance is decreased. Threshold voltage and gate oxide thickness are major issues/factor to introduce the leakage current in nano-scale MOSFET transistor.

Scaled down the conventional MOSFET not only bring to transistor performance issues but also to fabrication problem. The limitation of the MOSFET technology due to the fact that Zener breakdown will occur at source/substrate junction, lithography limitation and also the yield control for the product are the limitation to continue scaled the conventional MOSFET into smaller sizes.

The low carrier mobility in silicon (compared to carbon nonotube) maybe also degrades the MOSFET transistor performance. For those reasons, the new devices CNTFET, new channel materials, is being extensively explored.

This project work is used same 90nm technology transistor channel length to prove the CNTFET can provide better transistor performance compared to conventional MOSFET technology. The data collected from the simulation will be compared to conventional equivalent MOSFET technology and conclude with some analysis studies. With this data, the challenging for fabrication in sub-nanometer can be reducing. The experiments also will carry-out with differences parameter of voltage supply, diameter of Carbon Nanotube, oxide thickness and channel length to studies the effect of CNTFET transistor performance.

1.2 Scopes of Work

Based on available resources, limited time frame and expertise, this research project is narrowed down to the following scope of work:

1. Studying the quantum transport mechanism and applied the concept into ballistic CNTFET modeling by using MATLAB program.

2. Simulate the transfer characteristic and collecting data.

3. Analyze the simulation result and compared to conventional MOSFET transistor performance and conclude the output.

4. Input differences parameter of voltage supply, properties of Carbon Nanotubes, oxide thickness and channel length and studies the effect to CNTFET performance.

1.3 Outline of the Project Report

This report is organized into six chapters. The first chapter will covers the background, problem statement, objectives and the scopes of the project.

In chapter 2, we mainly are giving some brief introduction on physic of Carbon Nanotube and the reason of why choose Carbon Nanotube. Some of the detail of the physic for example hybridization, Carbon Nanotube Molecular structure, Chiral Vector and Metallic and Semiconducting Nanotube also will be covered in this chapter.

Chapter 3 will summarize the current Carbon Nanotube FETs and some future CNTFET concept being proposed by the researchers. Some of the current available technology for CNTFET manufacturing and a brief idea on Top gate CNTFET fabrication also will be covered.

Chapter 4 outlines some methodology of implementation for Ballistic CNTFET Modeling. The chapter will start with the basic theory of transport mechanism and drain current studies. The quantum transport solver NEGF formulism will also been covered in this chapter in order to provide a better understanding for the entire modeling. Step-by-step of implementation will be detail discuss in the following session, and hardware/software for this project will be listed as well.

Chapter 5 presents the studies of the simulation result and the analysis of this project.

Finally in Chapter 6, concludes the whole thesis and gives the direction or recommendation for future work.