HARDWARE CORE OF PIPELINED THINNING ALGORITHM

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Dedicated to my beloved mother, brother, sister, and wife and in the memories of my father.

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ABSTRACT

The process to associate a particular individual with an identity is known as personal recognition. One of the recognition system type is biometrics system. A biometric system is essentially a pattern recognition system that that performs authentication based on the individual's behavioural or physiological characteristics. One of the method is finger vein biometrics, which is an authentication technique that identify individuals and verify identity based on the images of human finger veins beneath the skin. There are a lot of process involved in a complete biometrics system. One of the process is thinning. Thinning or skeletonization is a process that extracts the vein patterns from binary image and produces 1-pixel wide output binary image as the result. Existing biometrics system have their own weaknesses and drawbacks such as not showing "aliveness" and also easy to be tampered with. Moreover, software implementation of biometrics system usually performed in an insecure environment and biometrics template stored in a central server. This is insecure and can cause leakage of information. Furthermore, thinning is a time consuming process, which takes a very long time to be completed in software implementation. So the objective of this work is to design a dedicated hardware core for thinning algorithm, implement and enhance the existing algorithm for better hardware performance, and apply pipeline architecture to the hardware design to further speed-up thinning process. This work will implement the algorithm in software and hardware. Hardware implementation of the algorithm is compared with software implementation in terms of accuracy and performance (speed). The hardware core designed managed to achieve a significant improvement in processing time. The work done in this project also managed to map a complex algorithm into hardware implementation and is the first one to implement thinning hardware design using System Verilog.

ABSTRAK

Proses yang digunakan unuk mengetahui identiti seseorang individu dikenali sebagai sistem pengenalan diri. Salah satu contoh sistem pengenalan diri ialah sistem biometrik. Sistem biometrik ialah sistem pengenalan bentuk yang melakukan pengesahan berdasarkan ciri kelakuan dan fisiologi seseorang. Salah satu daripada cara tersebut ialah sistem biometrik urat jari, yang merupakan teknik pengesahan individu berdasarkan kepada imej saluran darah di bawah kulit jari. Proses "thinning" ialah teknik yang mengekstrak bentuk urat jari dan menghasilkan imej keluaran dengan saiz 1 pixel. Sistem biometrik yang digunakan kini mempunyai kelemahan and kekurangannya yang tersendiri, seperti tidak menunjukkan "hidup" dan juga senang digodam. Malah, pelaksanan melalui perisian juga kebiasaannya dilakukan di dalam keadaan tidak selamat dan disimpan di dalam server. Ini adalah tidak selemat dan boleh menyebabkan pencurian maklumat. Lebih-lebih lagi, "thinning" ialah proses yang mengambil masa yang lama untuk dilaksanakan di dalam perisian. Justeru, objektif projek ini adalah mereka-bentuk perkakasan untuk algoritma "thinning", pelaksanaan dan peningkatan algoritma, dan juga pelaksanaan "pipeline" untuk meningkatkan prestasi perkakasan. Algoritma tersebut akan dilaksanakan di dalam perisian dan perkakasan. Pelaksanaan perisian akan disbandingkan dengan pelaksanaan perkakasan dari segi ketepatan and prestasi (kelajuan). Perkakasan yang direka berjaya mencapai anjakan paradigma dalam masa memproses. Projek yang dilaksanakan juga berjaya melaksanakn algoritma yang kompleks di dalam perkakasan dan juga merupakan projek pertama yang melaksanakan perkakasan "thinning" menggunakan "Sytem Verilog".

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LIST OF ABBREVIATIONS

PIN	-	Personal Identification Number
CMOS	-	Complementary Metal–Oxide–Semiconductor
FPGA	-	Field-Programmable Gate Array
HDL	-	Hardware Description Language
UDP	-	User Datagram Protocol
HDL	-	Hardware Description Language
RAM	-	Random Access Memory
FSM	-	Finite State Machine
FIFO	-	First-In First-Out
PC	-	Personal Computer
MU	-	Modification Unit
PTA	-	Parallel Thinning Algorithm
PTM	-	Parallel Thinning Module
DPRAM	-	Dual-Ported RAM
PPU	-	Pixel Processing Unit
DFG	-	Data Flow Graph
FBD	-	Functional Block Unit
MR	-	Mask Register
SIPO	-	Serial-In Parallel-Out
CU	-	Control Unit
DU	-	Datapath Unit
ASM	-	Algorithmic State Machine
IOBD	-	Input Output Block Diagram

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

The process to associate a particular individual with and identity is known as personal recognition. There are two traditional method that are widely used for recognition. These two methods are token-based and knowledge-based method. In token-based method, things possessed by the user is used for personal recognition such as ID card, keys, passport, or security tokens. In a knowledge-based method, something that the user knows is used for recognition such as Personal Identification Number (PIN), password, or pass phrase. A biometric system is essentially a pattern recognition system that that performs authentication based on the individual's behavioural or physiological characteristics [1]. Biometrics system is more reliable since the biometric characteristic cannot be lost or forgotten, difficult to replicate biometric features, and the system requires the person to be presented for the recognition process [2]. The overall process can be simplified as follows:

a. Biometric data acquisition from an individual
b. Feature extraction from the acquired data
c. Extracted feature comparison between the template and database
d. Executing an action based on the comparison result (grant access/identification)

Example of biometrics systems are face, iris, voice, and fingerprint. Other than these methods, the newer biometrics method is the finger-vein recognition. Finger Vein Biometrics is an authentication technique that identify individuals and verify identity based on the images of human finger veins beneath the skin. It is believed that the patterns of blood vein are unique to every individual, even among twins [3]. Finger vein biometrics provides are higher security means compared to other biometrics systems. For example, in voice recognition, vocal data can be stolen easily and allows for forgeries to be made with the stolen data. Similar problem can be seen in face recognition technique. Finger print biometrics is quite popular and well acknowledge across the society. However it has some weaknesses. The finger print pattern can easily be stolen and used for fraudulent. For iris biometrics, even though it provides high security, it is inconvenient because for an accurate iris recognition, it requires precise eye positioning during the recognition process. Moreover, the direct application of light into the eyes is unfriendly.

There are a lot of process involved in a complete biometrics system. One of the process is thinning, which is an important operation in the preprocessing stage of pattern recognition. Thinning or skeletonization is a process that extracts the vein patterns from binary image and produces 1-pixel wide output binary image as the result. [4]. Thinning is used to reduce the image data for storing and data processing. In a thinning process, a 3x3 window will be used to scan through the whole image and the necessary processing on the object pixel (center pixel) will be done based on its neighboring pixels.

1.2 Problem Statement

The rapid growth in the information technology has caused the authentication system to become something important in our daily life. The expectation from biometrics system are not just to have a system with better accuracy, but also to have a system that is able to produce an output at a very fast computation time.

Usually, the biometrics system are implemented in software. The software implementation of the biometrics system usually performed in an insecure environment and biometrics template stored in a central server [5]. This is insecure and can cause leakage of information. This can lead to a critical biometric information leakage issue [6]. A dedicated hardware design can be used to overcome this problem.

In a biometrics recognition system, thinning is one of the most compute intensive process. So thinning is a time consuming process. A very detailed calculation/processing is required to be applied on all the image pixels. This processing time is also dependent on the image size and the mask size used. It takes a very long time to be completed in software implementation. So, it needs to be accelerated in hardware by creating a dedicated hardware core for the processing.

The algorithm developed for thinning process are usually optimized for software implementation. Some of the works done involves applying thinning algorithm directly into the hardware without any enhancement and pipelining which causes the time improvement form software to hardware implementation is not so significant.

1.3 Objective

This project has three main objectives. First is to create a dedicated hardware core for the thinning algorithm. Second is to implement and enhance the existing thinning algorithm for better hardware performance. The final objective is to apply pipeline architecture to the hardware design to further speed-up the thinning process.

1.4 Scope

The scope of this thesis' work are:

i. The proposed Hardware Core of Pipelined Thinning Algorithm design is restricted on simulation model and not implemented on FPGA.
ii. The dedicated hardware core design is targeted for raw finger-vein image with the size of 240x160.
iii. The software simulation of the thinning algorithm is done using MATLAB and the hardware design is based on System Verilog Hardware Description Language (HDL).
iv. The hardware design simulation and functionality verification is done using Model Sim for waveform simulation, and MATLAB to display the obtained output image.
v. The targeted Device for Gate Level Simulation is Aria II GX.

1.5 Project Achievement

The achievements obtained from this project are:

i. This project will be the first one to create a hardware core design of the thinning algorithm using System Verilog.
ii. This project maps a complex thinning algorithm into hardware implementation and made enhancement to the algorithm so that it will be more suited for hardware implementation.

iii. The design achieved a significant improvement in terms of processing time and able to run at high frequency.

iv. High throughput at the output is achieved by applying pipelining to the design.

REFERENCE

[1] Jain, A. K., Ross, A. and Prabhakar, S. An Introduction to Biometric Recognition. *IEEE Transactions on Circuits and Systems for Video Technology*, 2004. 14(1): 4–20.

[2] Uludag, U., Pankanti, S., Prabhakar, S. and Jain, A. K. Biometric Cryptosystems: Issues and Challenges. *Proceedings of the IEEE*, 2004. 92(6): 948–960.

[3] Li, X. Y. and Guo, S. X. The Fourth Biometric - Vein Recognition. In: Yin, P. Y., ed. *Pattern Recognition Techniques, Technology and Applications*. InTech, Croatia, *1*, vol. 3. 2008.

[4] Yang, J., Shi, Y., Yang, J. and Jiang, L. A novel finger-vein recognition method with feature combination. *Image Processing (ICIP), 2009 16th IEEE International Conference on*. IEEE. 2009. 2709–2712.

[5] ENG, P. C. (2011). Finger-vein Biometric Authentication In A System-on-chip Based On Field Programmable Gate Arrays, Eng Pei Chee, Universiti Teknologi Malaysia, 1–183.

[6] Yang, S. L., Sakiyama, K. and Verbauwhede, I. M. A Compact and Efficient Fingerprint Verification System for Secure Embedded Devices. *Conference Record of the Thirty-Seventh Asilomar Conference on Signals, Systems and Computers*. 2003, vol. 2. 2058–2062.

[7] K.H. Mohamed, *Advanced RTL Design for FPGA with System Verilog*, Universiti Teknologi Malaysia, 2014, pp.89

[8] Lee, Y. H. (2013). *Finger-vein Biometric System Implemented In An Embedded Hardware Based On Field Programmable Gate Arrays*, Lee Yee Hui, Universiti Teknologi Malaysia, 1–156.

[9] Wang, L., Leedham, G. and Cho, S.-Y. Infrared imaging of hand vein patterns for biometric purposes. IET computer vision, 2007. 1(3): 113–122.

[10] Xu, H., Qu, Y., Zhang, Y., & Zhao, F. (2009, November). Fpga based parallel thinning for binary fingerprint image. In *Pattern Recognition, 2009. CCPR 2009. Chinese Conference on* (pp. 1-4). IEEE.

[11] Hermanto, L., Sudiro, S. A., & Wibowo, E. P. (2010, June). Hardware implementation of fingerprint image thinning algorithm in FPGA device. In*Networking and Information Technology (ICNIT), 2010 International Conference on* (pp. 187-191). IEEE.

[12] Hsiao, P. Y., Hua, C. H., & Lin, C. C. (2004, May). A novel FPGA architectural implementation of pipelined thinning algorithm. In *Circuits and Systems, 2004. ISCAS'04. Proceedings of the 2004 International Symposium on* (Vol. 2, pp. II-593). IEEE.

[13] Kim, K. H., Thien, P. C., Jin, S. H., Kim, D. K., & Jeon, J. W. (2008, August). Dedicated parallel thinning architecture based on FPGA. In *Multisensor Fusion and Integration for Intelligent Systems, 2008. MFI 2008. IEEE International Conference on* (pp. 208-213). IEEE.