RUN-TIME TRANSMISSION POWER RECONFIGURATION AND ADAPTIVE PACKET RELOCATION IN WIRELESS NETWORK-ON-CHIP

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To my beloved parents, who are always there throughout this journey.

To my late father, this thesis is dedicated to you.

We miss you a lot.

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ABSTRACT

Network-on-chip (NoC) is an on-chip communication network that allows parallel communication between all cores to improve inter-core performance. Wireless NoC (WiNoC) introduces long-range and high bandwidth radio frequency (RF) interconnects that can possibly reduce the multi-hop communication of the planar metal interconnects in conventional NoC platforms. In WiNoC, RF transceivers account for a significant power consumption, particularly its transmitter, out of its total communication energy. Current WiNoC architectures employ constant maximum transmitting power for communicating radio hubs regardless of physical location of the receiver radio hubs. Besides, high transmission power consumption in WiNoC with constant maximum power suffers from significant energy and load imbalance among RF transceivers which lead to hotspot formation, thus affecting the reliability of the on-chip network system. There are two main objectives covered by this thesis. Firstly, this work proposes a reconfigurable transmitting power control scheme that, by using bit error rate (BER) estimation obtained at the receiver's side, dynamically calibrates the transmitting power level needed for communication between the source and destination radio hubs. The proposed scheme achieves significant total system energy reduction by about 40% with an average performance degradation of 3% and with no impact on throughput. The proposed design utilizes a small fraction of both area and power overheads (about 0.1%) out of total transceiver properties. The proposed technique is generic and can be applied to any WiNoC architecture for improving its energy efficiency with a negligible overhead in terms of silicon area. Secondly, an energy-aware adaptive packet relocator scheme has been proposed. Based on transmission energy consumption and predefined energy threshold, packets are routed to adjacent transmitter for communication with receiver radio hub, with an aim to balance energy distribution in WiNoC. The proposed strategy alone achieves total communication energy savings of about 8%. A joint scheme of the reconfigurable transmitting power management and energy-aware adaptive packet relocator is also introduced. The scheme consistently results in an energy savings of 30% with minimal performance degradation.

ABSTRAK

Rangkaian-atas-cip (NoC) merupakan rangkaian komunikasi atas cip yang membolehkan komunikasi selari di antara semua teras untuk meningkatkan prestasi antara teras. NoC tanpa wayar (WiNoC) memperkenalkan jaringan komunikasi frekuensi radio (RF) jarak jauh dan jalur lebar tinggi antara sambungan yang mampu mengurangkan komunikasi pelbagai loncat yang berlaku kepada antara sambungan pada logam satah dalam platform NoC konvensional. Dalam WiNoC, sistem pemancar dan penerima RF melibatkan penggunaan kuasa yang ketara, terutamanya di bahagian pemancar, daripada keseluruhan tenaga komunikasi. Senibina WiNoC pada masa ini menggunakan kuasa pemancaran maksimum yang tetap bagi komunikasi antara hab radio tanpa mengambilkira lokasi fizikal hab radio penerima. Selain itu, penggunaan kuasa penghantaran yang tinggi dalam WiNoC dengan kuasa maksimum tetap mengalami masalah ketidakseimbangan tenaga dan beban antara hab radio RF yang ketara, yang membawa kepada pembentukan titik panas. Ini sekaligus menjejaskan kebolehpercayaan terhadap sistem rangkaian pada cip. Terdapat dua objektif utama yang dicakupi oleh tesis ini. Pertama, tesis ini mencadangkan satu kaedah kawalan kuasa pemancaran secara boleh laras berasaskan maklumat kadar ralat bit (BER) yang diperolehi daripada bahagian penerima. Kaedah ini menentukur tahap kuasa pemancaran yang diperlukan untuk komunikasi antara hab radio sumber dan destinasi bagi menjamin kebolehpercayaan penghantaran. Strategi yang dicadangkan ini mampu mengurangkan penggunaan sistem tenaga dengan ketara sekitar 40% dengan purata penurunan prestasi sebanyak 3% dan tiada kesan truput yang ketara. Dalam strategi yang dicadangkan, hanya sebahagian kecil lebihan kuasa dan luas kawasan daripada jumlah milikan pemancar dan penerima (kira-kira 0.1%) yang digunakan. Strategi yang dicadangkan adalah umum dan boleh digunakan pada mana-mana senibina WiNoC bagi meningkatkan kecekapan tenaga dengan lebihan luas kawasan silikon yang boleh diabaikan. Bagi objektif kedua, tesis ini mencadangkan satu skim penempat semula paket berkonsep sedar-tenaga di hab radio pemancar. Bercirikan penggunaan tenaga penghantaran dan ambang tenaga yang telah ditetapkan, paket dihalakan kepada hab radio pemancar bersebelahan untuk komunikasi dengan hab radio destinasi, mensasarkan pengagihan tenaga yang seimbang dalam sistem rangkaian. Strategi yang dicadangkan ini mampu memberikan pengurangan jumlah tenaga komunikasi sekitar 8%. Skim pengurusan bersama kawalan kuasa pemancar dan penempat semula paket berkonsep sedar-tenaga di radio hub pemancar juga diperkenalkan. Skim ini mampu memberikan penjimatan tenaga secara konsisten sebanyak 30% dengan penurunan prestasi yang minimum.

TABLE OF CONTENTS

CHAPTER	TITLE			PAGE
	DECLARATION			ii
	DEDICATION			iii
	ACKNOWLEDGEMENT			iv
	ABSTRACT			v
	ABSTRAK			vi
	TABLE OF CONTENTS			vii
	LIST OF TABLES			xii
	LIST OF FIGURES			xiv
	LIST OF ABBREVIATIONS			xix
	LIST OF APPENDICES			xxi
1	**INTRODUCTION**			**1**
	1.1	Introduction		1
	1.2	Problem Statement		3
	1.3	Research Objectives		4
	1.4	Scope of Work		4
	1.5	Research Contributions		5
	1.6	Thesis Organization		6
2	**LITERATURE REVIEW**			**8**
	2.1	Conventional Network-on-Chip and Its Design Issues		8
	2.2	Wireless Network-on-Chip		11
		2.2.1	WiNoC Topology	12
		2.2.2	WiNoC Routing and Data Transmission Protocol	17
		2.2.3	Modulation Techniques in WiNoC	20
		2.2.4	WiNoC Transceiver Systems	21
		2.2.5	On-Chip Antenna	24

	2.2.6	Selection of WiNoC Architectures	26
2.3	Multi-faceted WiNoC Design Consideration		29
2.4	Managing Power and Energy in NoC Platforms		29
	2.4.1	Power and Energy Issues in NoC	30
	2.4.2	Power and Energy Issues in WiNoC	32
2.5	Chapter Summary		35
3	**RESEARCH PROCESS**		**36**
3.1	Research Approach and Top-Level Perspective		36
3.2	Tools and Design Environment		40
	3.2.1	Quartus II	40
	3.2.2	Mentor Graphics ModelSim	41
	3.2.3	Synopsys Design Compiler	41
	3.2.4	Winoxim: A Noxim Extension	42
3.3	Criteria of Proofs		43
	3.3.1	Friis Transmission Equation	43
	3.3.2	Modelling WiNoC Transceiver Transmission Power	45
	3.3.3	Adaptive Energy Management	49
3.4	Design Verification		51
	3.4.1	Reconfigurable Transmission Power Management: Verification Parameters	51
	3.4.2	Adaptive Packet Relocator: Verification Parameters	52
	3.4.3	SPLASH-2 and PARSEC Benchmarks	53
3.5	Chapter Summary		54
4	**RECONFIGURABLE TRANSMITTING POWER MANAGEMENT**		**55**
4.1	Reconfigurable Transmitting Power Management Scheme		55
	4.1.1	Centralized Reconfigurable Transmitting Power Scheme	57
	4.1.2	Distributed Reconfigurable Transmitting Power Scheme	59
4.2	Architecture of Reconfigurable Transmitting Power Scheme		61

4.2.1 Centralized Reconfigurable Transmitting Power Management Scheme 62
4.2.1.1 Power Manager 62
4.2.1.2 Variable Gain Controller and Control Network 65
4.2.1.3 Implementation on WiNoC Platforms 66
4.2.2 Distributed Reconfigurable Transmitting Power Management Scheme 67
4.2.2.1 Reconfigurable Variable Gain Controller 68
4.2.2.2 Control Network 68
4.2.2.3 Implementation on WiNoC Platforms 70
4.3 Experimental Results and Analysis 72
4.3.1 Effects of Reconfiguration Periods 72
4.3.2 Effects of Reconfiguration States 76
4.3.3 Effects of Packet Injection Rates 77
4.3.4 Effects of Selection of The Reconfigurable Transmitting Power Scheme (Centralized versus Distributed) 81
4.3.5 Performance of SPLASH-2 and PARSEC Benchmark Suites 83
4.3.6 Effects of Packet Lengths on VGA Power Consumption 87
4.3.7 Effects of Area and Power Overheads 88
4.4 Chapter Summary 89

5 ADAPTIVE PACKET RELOCATOR 90
5.1 Adaptive Packet Relocator Scheme 90
5.1.1 Adaptive Packet Relocator 91
5.1.2 Joint Scheme: Adaptive Packet Relocator and Centralized Reconfigurable Transmitting Power 95
5.2 Architecture of Adaptive Packet Relocator Scheme 96
5.2.1 Adaptive Packet Relocator 97
5.2.1.1 Adaptive Packet Relocator Module 97
5.2.1.2 Control Network 98

5.2.2 Joint Scheme: Adaptive Packet Relocator and Centralized Reconfigurable Transmitting Power 99
5.2.2.1 Implementation on WiNoC Platforms 100
5.3 Experimental Results and Discussion 104
5.3.1 Results of Adaptive Packet Relocator Scheme 104
5.3.1.1 Effects of Energy Thresholds 104
5.3.1.2 Effects of Relocation Period 107
5.3.1.3 Effects of Packet Injection Rates 109
5.3.1.4 Performance of SPLASH-2 and PARSEC Benchmark Suites 112
5.3.2 Results of Joint Reconfigurable Transmitting Power and Packet Relocator Scheme 115
5.3.2.1 Joint Reconfigurable Transmitting Power and Packet Relocator: Effects of Reconfiguration Periods 115
5.3.2.2 Joint Reconfigurable Transmitting Power and Packet Relocator: Effects of Reconfiguration States 118
5.3.2.3 Joint Reconfigurable Transmitting Power and Packet Relocator: Effects of Energy Thresholds 120
5.3.2.4 Joint Reconfigurable Transmitting Power and Packet Relocator: Effects of Relocation Period 122
5.3.2.5 Joint Reconfigurable Transmitting Power and Packet Relocator: Packet Injection Rates 125
5.3.3 Comparative Performance Evaluation 129
5.4 Chapter Summary 131

6 CONCLUSIONS 132

6.1 Contributions of Thesis 132
6.1.1 Reconfigurable Transmitting Power Scheme 132
6.1.2 Adaptive Packet Relocator Scheme 133
6.2 Directions for Future Works 135

REFERENCES **136**
Appendix A 148

LIST OF TABLES

TABLE NO.	TITLE	PAGE
2.1	Comparison of bus based system with NoC.	9
2.2	WiNoC architectures characteristics working in different frequency ranges.	27
2.3	Current WiNoC architecture strategies on power and energy management.	33
3.1	3-bit code word representing seven power steps in the VGA look-up table.	49
3.2	SPLASH-2 and PARSEC benchmark suites used in this thesis.	54
4.1	SPLASH-2 and PARSEC benchmark suites energy dissipation comparison applied on WCube and iWise WiNoC architectures.	84
4.2	SPLASH-2 and PARSEC benchmark suites latency comparison applied on WCube and iWise WiNoC architectures.	85
4.3	Area and power overheads of the proposed centralized reconfigurable transmitting power design.	88
5.1	Individual reduced latency of SPLASH-2 and PARSEC benchmark suites when the adaptive packet relocator is applied on WCube and iWise WiNoC architectures for high PIR.	112
5.2	SPLASH-2 and PARSEC benchmark suites energy dissipation comparison applied on WCube and iWise WiNoC architectures.	113
5.3	SPLASH-2 and PARSEC benchmark suites latency comparison applied on WCube and iWise WiNoC architectures.	114
5.4	Individual reduced latency of SPLASH-2 and PARSEC benchmark suites when the joint scheme is applied on WCube and iWise WiNoC architectures for high PIR.	128

5.5 SPLASH-2 and PARSEC benchmark suites energy dissipation comparison applied on WCube and iWise WiNoC architectures. 130

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
2.1	Examples of commonly used two-dimensional NoC topologies.	10
2.2	A possible 4×4 WiNoC architecture	13
2.3	Possible radio hubs topology in WiNoC : (a) ring (b) star (c) tree (d) mesh	14
2.4	Examples of several WiNoC architectures for 64-core network size.	16
2.5	Packet protocol for WiNoC system. *dest_id* field contains the packet's destination subnet and core addresses.	20
2.6	OOK transceiver system block diagram.	23
2.7	Comparison of radiation patterns between zigzag and linear dipole antennas.	25
2.8	Baseline WiNoC platforms for the proposed reconfigurable transmitting power management strategy	28
3.1	Flow chart of the steps taken to achieve the objectives in this thesis.	39
3.2	Top level perspective of the work done in this thesis. Detailed explanations of the work are described in Section 3.2.	40
3.3	Friis transmission equation: geometrical orientation of transmitting and receiving antennas. Considering a spherical coordinate system, ϕ is the azimuthal angle in the XY plane, where the X axis is 0 and Y axis is 90. θ is the elevation angle where the Z-axis is 0 and the XY plane is 90.	44
3.4	Attenuation map of G_a for tiles *T0*, *T1*, *T4* and *T5*. Other maps are obtained using mesh-based symmetry structure.	46
3.5	Characterization of required received power (X-axis) for different data rate in dBm against BER (Y-axis) in OOK modulation scheme. The graph is obtained by manipulating combination of Eq. (3.6) and Eq. (3.7).	47

4.1	A possible centralized architecture for 2×2 WiNoC radio hubs.	58
4.2	System block diagram of the distributed reconfigurable transmitting power architecture.	61
4.3	Block diagram of the architecture implementing the proposed WiNoC scheme	63
4.4	Proposed power manager module: (a) Top level view. (b) Internal architecture.	64
4.5	Proposed power manager module implemented on two WiNoC architectures: (a) iWise. (b) WCube.	67
4.6	Control network architecture: (a) A possible floorplan for 3×3 radio hubs WiNoC (b) Internal architecture of the control switch block implementing token ring flow control	69
4.7	Implementation of the distributed power manager module on two WiNoC architectures supporting Figure 4.6: (a) iWise (b) WCube	71
4.8	The energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise between the baseline and the proposed centralized reconfigurable transmitted power design. Different RP values are used and verified using SPLASH-2 and PARSEC benchmark suites.	73
4.9	Analysis of performance in terms of energy savings for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise on WiNoC architectures verified with SPLASH-2 and PARSEC benchmark suites.	74
4.10	The latency impact of WiNoC architectures implementing the proposed design with varied RS: (a) WCube (b) iWise.	76
4.11	The latency overheads impact on WiNoC architectures implementing the proposed design with varied RS and verified using SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise.	77
4.12	Performance comparison in terms of energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise between the baseline WCube and iWise architectures for three different PIR categories.	78

4.13	The energy savings for (a) WCube (b) iWise and latency overheads analysis for (c) WCube (d) iWise on WiNoC architectures implementing the proposed design with three different PIR categories and verified using SPLASH-2 and PARSEC benchmark suites.	80
4.14	Detailed flits energy saving for three injection rate categories.	81
4.15	Performance analysis in terms of (a) energy savings and (b) latency impacts on WiNoC architectures between the centralized and distributed reconfigurable transmitted power schemes.	82
4.16	Performance analysis in terms of energy savings for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise using seven application files in the SPLASH-2 and PARSEC benchmark suites.	86
4.17	Power consumption per packet in VGA controller for different packet lengths of 10 flits.	88
5.1	Finite state machine implementing the proposed energy aware method.	93
5.2	Block diagram of the architecture implementing the proposed WiNoC scheme.	96
5.3	Proposed adaptive packet relocator module.	98
5.4	Network access control architecture: (a) A possible floorplan for 3×3 radio hubs WiNoC. (b) Control switch block implementing token ring flow control.	99
5.5	Baseline WiNoC platforms for the proposed the adaptive packet relocator strategy: (a) iWise (b) WCube	101
5.6	Implementation of hybrid reconfigurable transmitting power and adaptive relocator design on baseline WiNoC platforms: (a) iWise (b) WCube	103
5.7	Energy threshold in terms of energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise with the adaptive packet relocator design verified using seven application files in the SPLASH-2 and PARSEC benchmark suites.	105
5.8	Performance analysis in terms of energy threshold impact on WiNoC architectures with the adaptive packet relocator design verified using seven application files in the SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise.	106

5.9 Relocation periods in terms of energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise with the adaptive packet relocator design verified using seven application files in the SPLASH-2 and PARSEC benchmark suites. 108

5.10 Performance analysis in terms of energy overheads on WCube and iWise architectures with the adaptive packet relocator design as compared to their baseline architectures: (a) WCube (b) iWise. 109

5.11 Packet injection rates in terms of energy dissipation for (a) WCube (b) iWise and latency for (c) WCube (d) iWise with the adaptive packet relocator design verified using seven application files in the SPLASH-2 and PARSEC benchmark suites. 110

5.12 Performance analysis in terms of energy overheads on WiNoC architectures with the adaptive packet relocator design verified using seven application files in the SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise. 111

5.13 Performance analysis of SPLASH-2 and PARSEC benchmark suites in terms of energy overheads impact on WiNoC architectures with the adaptive packet relocator design verified using seven application files: (a) WCube (b) iWise. 114

5.14 Reconfiguration period in terms of energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise with the joint adaptive packet relocator with centralized reconfigurable transmitting power design verified using seven application files in the SPLASH-2 and PARSEC benchmark suites. 117

5.15 Energy savings on WiNoC architectures with the adaptive packet relocator design verified using seven application files in the SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise. 117

5.16 The reconfiguration state performance impacts in terms of energy dissipation for (a) WCube (b) iWise and latency for (c) WCube (d) iWise in WiNoC architectures implementing the proposed joint scheme with varied RS. 119

5.17 The energy savings impact on WiNoC architectures implementing the proposed joint scheme with varied RS and verified using SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise. 120
5.18 Energy thresholds in terms of energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise in WiNoC implementing the proposed joint scheme verified using seven application files in the SPLASH-2 and PARSEC benchmark suites. 121
5.19 Energy savings on WiNoC architectures implementing the proposed joint scheme verified using seven application files in the SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise. 122
5.20 Relocation period in terms of energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise implementing the proposed joint scheme verified using seven application files in the SPLASH-2 and PARSEC benchmark suites. 124
5.21 Performance analysis in terms of energy savings impact on WiNoC architectures implementing the proposed joint scheme verified using seven application files in the SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise. 125
5.22 PIR in terms of energy dissipation for (a) WCube (b) iWise and latency impacts for (c) WCube (d) iWise implementing the proposed joint scheme verified using seven application files in the SPLASH-2 and PARSEC benchmark suites. 126
5.23 Performance analysis in terms of energy savings impact on WiNoC architectures implementing the proposed joint scheme verified using seven application files in the SPLASH-2 and PARSEC benchmark suites: (a) WCube (b) iWise. 127
5.24 Performance analysis in terms of energy dissipation impact on WiNoC architectures implementing the proposed joint scheme verified using seven application files in the SPLASH-2 and PARSEC benchmark suites. 129

LIST OF ABBREVIATIONS

ASK-OOK	–	Amplitude Shift Keying - On-Off Keying
ADC	–	Analog to Digital Converter
BPSK	–	Binary Phase Shift Keying
BER	–	Bit Error Rate
CNT	–	Carbon-Nanotube
CMU	–	Central Monitoring Unit
CMOS	–	Complementary Metal-Oxide Semiconductor
CAD	–	Computer-Aided Design
Cs	–	Control Switch
dB	–	Decibels
DSM	–	Deep Submicron
DAC	–	Digital to Analog Converter
FDMA	–	Frequency Division Multiple Access
GHz	–	Gigahertz
HDL	–	Hardware Description Language
HEMT	–	High Electron Mobility Transistors
HFSS	–	High Frequency Structural Simulator
ID	–	Identification Number
IP	–	Intellectual Property
ITRS	–	International Technology Roadmap for Semiconductors
LNA	–	Low-noise Amplifier
MTTF	–	Mean-Time-to-Failure
MPSoC	–	Multiprocessor System-on-Chip
MWCNT	–	Multi-Walled Carbon Nanotube
NoC	–	Network-on-chip
OOK	–	On-Off Keying
PIR	–	Packet Injection Rate
pJ	–	pico Joule

PA	–	Power Amplifier
PARSEC	–	Princeton Application Repository for Shared-Memory Computers
PE	–	Processing Element
RF	–	Radio Frequency
RAW	–	Raw Architecture Workstation
R-VGA	–	Reconfigurable Voltage Gain Amplifier
RP	–	Reconfiguration Period
RS	–	Reconfiguration State
RTL	–	Register Transfer Language
SIA	–	Semiconductor Industry Association
SNR	–	Signal to Noise Ratio
SiGE HBT	–	Silicon-Germanium Heterojunction Bipolar Transistors
SA	–	Simulated Annealing
sub-THz	–	Sub-Terahertz
SoC	–	System-on-Chip
THz	–	Terahertz
UWB	–	Ultra Wideband
UCDB	–	Unified Coverage Database
VGA	–	Variable Gain Amplifier
VLSI	–	Very Large Scale Integration
VCO	–	Voltage Controlled Oscillator
VSWR	–	Voltage Standing Wave Ratio
WiNoC	–	Wireless Network-on-Chip

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	List of Publications	148

CHAPTER 1

INTRODUCTION

1.1 Introduction

Network-on-chip (NoC) architectures are made up of a large number of intellectual property (IP) blocks, or commonly known as cores [1, 2]. This platform facilitates cores communication parallelism to reduce execution time and achieve high performance. It was predicted that the rapid advancement in many-core SoC would make the number of processing cores to increase rapidly on a single die over the next few years [3]. With the continuous technology scaling and integration in many-core architectures, global wire delays increase greater than the gate delays. Furthermore, with faster clock rates, eighty percent of critical path delays are contributed by the interconnects [4], which results in multiple clock cycle delays for data traversing throughout the platform. This shows that it is an important measure in many-core architectures to find alternatives for the enabling solutions to the conventional interconnects. Therefore, many-core architectures have embarked on a perspective shift from computation-centric to communication-centric as the number of cores in a chip increases [5, 6].

Network-on-chip (NoC) is an on-chip communication network introduced to enable integration of multiple cores in on-chip ambience [2]. It allows parallel communication among all cores to improve inter-core performance. Several NoC designs ranging from application-specific to general-purpose platforms have been developed since the inception of NoCs such as $\times$pipes [7], Æthereal [8] and Proteo [9]. Despite the advantages of NoC, the increasing number of cores in many-core architectures limits the NoC performance in terms of latency and power consumption. Although the interconnect frequency becomes higher with the aggressive very large scale integration (VLSI) technology scaling and growing computational complexity demand, high power consumption of the total system power mainly due to NoC's

multi-hop communication nature has emerged.

Future deep submicron (DSM) technologies, operating frequency, transistor density and design complexity of many-core system-on-chip (MPSoC) will continue to make latency, power and temperature dissipation a major design concern [6]. High power density per-core is resulted from increasing number of transistors that contributes to hot spot formation at respective cores which accelerates static power dissipation and mean-time-to-failure (MTTF) problems in SoC, which lead to reliability issues. Some NoC prototypes significantly show NoCs taking substantial portion of system power e.g ~40% in RAW chip [10] and ~30% in Intel 80 core teraflop chip [11]. In addition to that, International Technology Roadmap for Semiconductors (ITRS) predicts that the industry will need to explore new on-chip communication perspective because the wire-based interconnects will no longer improve performance metric in the future many-core architectures [4]. Hence, several improved NoC architectures have been proposed such as 3D NoCs [12, 13], photonic NoC [14–16] and wireless NoC (WiNoC) [17–20].

WiNoC introduces long-range and high bandwidth radio frequency (RF) interconnects that can possibly reduce the multi-hop communication of the planar metal interconnects in conventional NoC platforms. On average, implementing WiNoC architecture improves about 20% performance and 30% energy savings over the fully wired NoC links [17, 21]. For instance, WCube and Ultra Wideband (UWB) designs reduce latency by about 20% - 45% and 23% respectively [20, 22]. Besides improving the performance and energy metrics, WiNoC overcomes the scalability problem in traditional NoC as the network size increases with time. Advances in Complementary Metal-Oxide Semiconductor (CMOS) technology has shown possible integration of antenna operating in millimeter-wave range frequency and transceivers onto a single chip [23]. Furthermore, carbon-nanotube (CNT) antenna operating in optical frequencies has also been explored [24]. Researchers have proven potential communication hybrid between the prominent NoCs and wireless module. A group of cores can be clustered together for integration with the top layer wireless transceiver module to reduce communication hops especially between distant cores as compared to the conventional wired links NoC. The wireless links network in WiNoC is augmented to the traditional NoC interconnect network. Several WiNoC designs, namely McWiNoC [20], iWise [19] and mmSwNoC [18] employ this cluster-based concept.

1.2 Problem Statement

Power and energy management continue to play an important role in the on-chip communication issue, even for WiNoC. Despite the improvement in communication performance over the conventional NoCs, the major contribution of WiNoC power consumption is due to the radio transmitter front-end connected to the antenna. It has been shown that RF transmitter front-end dissipates about 50% in [25] and about 74% in [26] for the network size of 128, 256 and 512 cores from the total WiNoC transceiver power consumption. Current WiNoC efforts employ the maximum transmitting power for each transmitter regardless of the physical location of the receiver antenna.

Previous works in the context of WiNoCs are based on fixed transmitting power regardless of the physical location of destination nodes that is able to guarantee a certain reliability level (in terms of bit error rate (BER) in the worst case scenario) such as in [19, 20, 27]. However, some receiver locations may be oversupplied by the transmitting power, leading to the waste of energy. Mineo *et al*. [28] proposed a configurable transmitter with transmission power based on physical location of the receiver. It has been shown that such transmitters allow significant power saving with a negligible impact in terms of area and delay. However, the transceiver power manager has to be configured offline by means of an extensive characterization phase which requires either time consuming field solver simulations or direct measurement of real context. This one-off configuration technique requires robust and accurate field solver simulator of radiating fields in CMOS substrates, and many commercial field solver simulators have not been rigorously tested or verified in on-chip integration level [29]. Another approach is by Ganguly *et al*. [18], who proposed a dynamic voltage and frequency scaling technique based on predictive core switching rate implemented at the wired link layer of WiNoC without considering reliability level at the wireless link.

Another important aspect in WiNoC is the energy distribution. High transmission power consumption with constant maximum power makes WiNoC suffers from significant energy and load imbalance among RF modules which leads to hotspot formation, thus affecting the reliability requirement of the network system. Computation and communication loads vary over time depending on various intrinsic and extrinsic factors such as power saving mode specification, data streaming and long duration of data transmission. These features necessitate extra computation and communication run-time efforts causing load imbalance and potential hotspot formation.

The communication density grows higher as distant cores communicate, inextricably linked to heavy resource utilization and eventually cause high energy consumption. A task migration scheme based on predictive task allocation to balance the energy distribution in WiNoC has been proposed through thermal management in [30]. However, both wired and wireless links must be considered in this scheme which results in complexity in terms of implementation. Consequently, besides transmitting power management, other characteristics such as dynamic energy management on WiNoC platform which can offer improvement in energy distribution while satisfying system reliability constraint must be considered in the search of the power and energy optimization in WiNoC system.

1.3 Research Objectives

As the power and energy management issues in WiNoC have been highlighted in the Section 1.2, the objectives focus mainly at addressing the transmitting power as well as managing the energy issues in order to achieve optimized power and balanced energy distribution in WiNoC. The principal objectives of this thesis can be summarized as below:

1. To design a reconfigurable transmission power management module in WiNoC platform to achieve energy saving with limited performance degradation.
2. To design an adaptive energy-aware packet relocator module to achieve improved energy distribution in WiNoC platform.
3. To design and verify a joint reconfigurable transmission power management and energy-aware packet relocator module on WiNoC platform by integrating designs in (1.) and (2.) to achieve energy saving and energy distribution on WiNoC platforms.

1.4 Scope of Work

The work in this thesis uses a combination of tools mostly obtained from open source repositories. These available NoC repositories open up new exploration for new NoC paradigm such as 3D NoC [31], hardware/software cosimulation [32] and WiNoC [33]. The works in this thesis have been benchmarked with benchmark suites

from an open source repository. These multithreaded workloads [34] are used in the simulator to evaluate the energy and latency parameters achieved as compared to the baseline parameters. The scope of this thesis are summarized as follows:

1. The proposed designs are developed in SystemC and modeled using the extended version of Noxim simulator [33] that supports wireless communication.
2. Attenuation map based on the communication between source and destination radio hub for the 64-core network size is used throughout the work in this thesis. This work is based on the work of Mineo *et al.* [28].
3. The proposed designs are implemented on two WiNoC architectures namely WCube [22] and iWise [19] These architectures are developed on the conventional mesh-based NoC. However, the proposed designs are also implementable on other WiNoC platforms.
4. The works are evaluated based on real traffic that cover various application domains such as high performance computing, media processing, animation and data mining.
5. The network size in consideration is set to 64 cores, to suit the utilized benchmark suites which support the network size.
6. Power and area overheads occupied by the designs are analysed using Synopsis Design and Power Compiler. The power metric is used in the simulation that contributes a fraction of the total power consumption of the designs.

1.5 Research Contributions

This work proposes two novel designs to realize the thesis objectives. Each following subsection describes brief contributions achieved by the three thesis objectives. Further research contributions are discussed in detail in Chapter 6.

1. Reconfigurable Transmission Power

   This work proposes a mechanism for reducing the power dissipation of transmitters in WiNoC architectures, given a certain reliability requirement expressed in term of maximum allowable error rate. A power management scheme that is able to dynamically tune the transmitting power of each communicating transmitter-receiver pair to meet this requirement with minimum energy consumption has been employed. The power manager is an independent

entity which regulates the transmitting power in part or for the whole WiNoC. By allowing the self-calibration scheme on WiNoC, the network is able to self-organize power consumption to achieve reliability. Significant energy savings have been achieved as this design is utilized on WiNoC platforms used.

2. Adaptive Packet Relocator

   In this part of work, a dynamic energy management on WiNoC platform is proposed to offer energy consumption improvement while satisfying system reliability constraint. An energy-aware packet relocator scheme has been proposed which, based on transmission energy consumption and predefined energy threshold, packets are routed to adjacent transmitter for communication with destination radio hub, aiming at energy distribution in the network system. Hence, WiNoC is able to self-organize the energy distribution. Energy distribution has been achieved as the energy-aware design is utilized on WiNoC platforms used. In addition to that, distributed and lower energy dissipation have been observed when both designs are integrated in WiNoC system operation.

1.6 Thesis Organization

This thesis is organized in six chapters. The rest of the thesis are organized as follow.

Chapter 2 introduces the background studies of WiNoC designs and theories such as the topology, data routing and transmission protocol as well as WiNoC transceiver system. It covers the literature information needed to implement the proposed designs in this thesis. Power and energy management issues in the conventional NoC as well as WiNoC are reviewed to highlight the significance of the proposed works.

Chapter 3 highlights the design methodologies implemented in this thesis. The first part of the chapter explains the research approach and top level overview to provide the overall perspectives of the works to achieve the objectives. The rest of the chapter detail out the research perspective mentioned in the first part such as tools and platforms, formulations and terminology used in analyzing the experimental results of the works. Design verification method using common benchmark suites is also presented at the end of the chapter.

Chapter 4 specifically presents the first objective of this thesis which is the proposed reconfigurable transmitting power scheme. The technique aims at achieving energy savings with limited performance degradation. Introduction to the theory on obtaining the required transmitting power to guarantee a certain error rate using a basic modulation technique is presented, followed by the detailed implementation of the proposed design on two WiNoC architectures. Verification has been done using SPLASH-2 and PARSEC benchmark application suites [35, 36] and comparison analysis are presented.

Chapter 5 discusses the energy management strategy in WiNoC platforms. The background theories that lead to the implementation of the proposed work are presented, followed by the detailed architecture of the proposed packet relocator module on two WiNoC architectures. The platforms are benchmarked using SPLASH-2 and PARSEC benchmark application suites [35,36]. In the final part of the chapter, an integration of the power management with the energy aware packet relocation schemes is introduced, analysed and compared against baseline architectures to determine the best energy management approach in WiNoC platforms.

Finally, Chapter 6 presents the conclusions of the work in this thesis. It highlights the contributions to knowledge achieved in terms of energy savings as well as performance degradation when the proposed designs are implemented on WiNoC platforms. The directions for future work are discussed to serve as a basis for future research in the low-power and distributed energy issue in WiNoC architectures.

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