

A COMPLEMENTARY METAL OXIDE SEMICONDUCTOR  
LOW NOISE AMPLIFIER USING INTEGRATED ACTIVE INDUCTOR

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## ABSTRACT

Low Noise Amplifier (LNA) is a very important component in a receiver system. It provides the smallest noise and high gain to decrease the noise of the subsequent stages and the whole system. As System On Chip (SOC) is very important nowadays, active inductor is an alternative to the designer to have an integrated design. Furthermore, active inductor can be tuned to obtain the required inductance and Q-factor values. Instead of using passive inductor such as spiral and bonding wire which need bigger die area, active inductor can be employed to save die area but this comes at the cost of higher current consumption and noise. This thesis presents the study of active inductor architecture, how active inductor can combine with LNA and evaluation on LNA performance when active inductor is added. This will help designers to have better understanding on how to use active inductor in their design. This research proposes the Common Gate LNA architecture and is designed with 1.2  $\mu\text{m}$  CMOS process, operating at 850 MHz. The voltage gain and noise factor obtained are 24.7 dB and 8.26 dB respectively. Two active inductors are used as gain control, input and output matching of LNA. However, the LNA consumes 163.8 mW where 75% percent of power consumption is contributed by active inductor.

## ABSTRAK

Penguat Hingar Rendah (LNA) adalah komponen yang amat penting dalam sistem penerimaan. Ia menyediakan hingar yang paling rendah dan gandaan yang tinggi untuk merendahkan hingar pada peringkat yang berikutnya dan dalam keseluruhan sistem. Memandangkan Sistem Atas Cip (SOC) semakin penting pada akhir-akhir ini, induktor aktif merupakan alternatif kepada pereka untuk mencapai rekebentuk bersepadu. Lebih-lebih lagi, induktor aktif boleh diubah suai untuk mendapatkan nilai induktor dan faktor-Q yang diperlukan. Berbanding dengan induktor pasif seperti pular dan wayar ikatan yang memerlukan ruang yang besar, induktor aktif boleh digunakan untuk menjimatkan ruang ital tetapi terpaksa memerlukan penggunaan arus dan hingar yang tinggi. Tesis ini membentangkan induktor aktif, bagaimana induktor aktif boleh digabungkan dengan LNA dan mengkaji LNA apabila induktor aktif digabungkan. Ini dapat membantu pereka untuk lebih memahami bagaimana hendak menggunakan induktor aktif dalam proses merekabentuk. Kajian ini menggunakan asas LNA Pintu Sepunya dengan proses 1.2  $\mu\text{m}$ , beroperasi pada 850 MHz. Gandaan voltan dan faktor hingar diperolehi sebagai 24.7 dB dan 8.26 dB. Dua induktor aktif digunakan sebagai kawalan gandaan, padanan masukan dan keluaran untuk LNA. LNA ini didapati menggunakan 163.8 mW, di mana 75% daripadanya adalah disumbangkan oleh induktor aktif.

## TABLE OF CONTENTS

<b>CHAPTER</b>	<b>TITLE</b>	<b>PAGE</b>
	<b>DECLARATION</b>	ii
	<b>ACKNOWLEDGMENT</b>	iii
	<b>ABSTRACT</b>	iv
	<b>ABSTRAK</b>	v
	<b>TABLE OF CONTENTS</b>	vi
	<b>LIST OF TABLES</b>	ix
	<b>LIST OF FIGURES</b>	x
	<b>LIST OF SYMBOLS</b>	xiii
	<b>LIST OF APPENDICES</b>	xv
<b>1</b>	<b>INTRODUCTION</b>	1
	1.1 Introduction	1
	1.2 Problem Statement	2
	1.3 Objective of The Research	3
	1.4 Design Target	3
	1.5 Methodology	3
	1.6 Scope of Work	4
	1.7 Thesis Outline	4

<b>2</b>	<b>ACTIVE INDUCTOR AND LNA ARCHITECTURE STUDY</b>	<b>5</b>
2.1	Introduction	5
2.2	Active Inductor	5
2.2.1	Active Inductor Motivation	6
2.2.2	Active Inductor Architecture	7
2.2.2.1	Basic Active Inductor	10
2.2.2.2	Cascode Active Inductor	11
2.2.2.3	Regulated Cascode Active Inductor	12
2.2.2.4	Differential Active Inductor	13
2.3	Low Noise Amplifier	14
2.3.1	LNA Architecture	15
2.3.1.1	Common Source Amplifier	15
2.3.1.2	Shut-shunt Feedback Amplifier	17
2.3.1.3	Inductive Source Degeneration Amp	18
2.3.1.4	Common Gate Amplifier	19
2.4	Comparison of LNA Architecture Performance	20
<b>3</b>	<b>ACTIVE INDUCTOR AND LNA DESIGN</b>	<b>21</b>
3.1	Introduction	21
3.2	Proposed Active Inductor	22
3.2.1	Small Signal Analysis	24
3.2.2	Active Inductor Design	29
3.3	LNA design with Active Inductor	30

<b>4</b>	<b>SIMULATION RESULT</b>	<b>34</b>
	4.1 Introduction	34
	4.2 Active Inductor Analysis	35
	4.2.1 Analysis on Inductance & $f_0$ Tuning	36
	4.2.2 Analysis on Q-factor	41
	4.2.3 Analysis on Noise	43
	4.2.4 Summary of Analysis	44
	4.3 LNA with Active Inductor Analysis	47
	4.3.1 LNA with Active Ls sweep	48
	4.3.2 LNA with Sweep Active Ld	51
	4.3.3 LNA with Sweep Cd	54
	4.4 Final Design – LNA with Active Inductor	57
	4.5 LNA Comparison – Active vs Passive/Ideal Inductor	64
	4.6 Comparison of LNA design	71
<b>5</b>	<b>CONCLUSION AND FUTURE WORK</b>	<b>72</b>
	5.1 Conclusion	72
	5.2 Future Work	75
	<b>REFERENCES</b>	<b>76</b>
Appendix A	SPICE Transistor Parameter	79
Appendix B	Active Inductor Inductance Extraction from Impedance Simulation	81
Appendix C	Proposed LNA and Active Inductor Calculation	83
Appendix D	SPICE file for LNA with Active Inductor	97

## LIST OF TABLES

TABLE NO.	TITLE	PAGE
2.1	Common Source Amplifier Performance	16
2.2	Shunt-shunt feedback Amplifier Performance	17
2.3	Inductive Source Degeneration Amplifier Performance	18
2.4	Common Gate Amplifier Performance	19
2.5	Comparison between All Architectures	20
3.1	Summary of proposed active inductor analysis	28
3.2	Active inductor transistors sizes	29
4.1	Active inductor transistor size	35
4.2	Design Variable for Inductance Tuning	36
4.3	Summary of different width on M1, 2, 3 & 4	40
4.4	Summary of different W/L on M11, 12, 13 & 14	42
4.5	W = 222 um summary	46
4.6	Performance summary of LNA with active inductor	62
4.7	Comparison between LNA with active and passive inductor	69
4.8	LNA design comparison from other research	71



## LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
2.1	Basic Gyrator-C Topology	7
2.2	Active inductor Model	8
2.3	Circuit of Basic Active Inductor	10
2.4	Circuit of Cascode Active Inductor	11
2.5	Circuit of Regulated Cascode Active Inductor	12
2.6	Circuit of Differential Active Inductor	13
2.7	LNA in a receiver	14
2.8	Common Source Amplifier Circuit	15
2.9	Shunt-shunt feedback amplifier circuit	17
2.10	Inductive Source Degeneration Amplifier Circuit	18
2.11	Common Gate Amplifier Circuit	19
3.1	Proposed active inductor	22
3.2	Small signal analysis	24
3.3	Simplified small signal analysis	25
3.4	A sample waveform of an active inductor	26
3.5	Simplified model of proposed active inductor	27
3.6	Inductive Source Degeneration with Active Inductor	30
3.7	Common Gate with Active Inductor	31
3.8	Architecture for LNA with active inductor	32
4.1	Sweep width of M1, 2, 3 & 4	37
4.2	Sweep Ibias (0.6 mA – 2.5 mA) with W=50 um	38

4.3	Sweep Ibias (0.6 mA – 2.5 mA) with W=500 $\mu$ m	39
4.4	Q-factor improvement	42
4.5	Noise with W = 50 $\mu$ m	43
4.6	Noise with W = 500 $\mu$ m	43
4.7	Inductance result with W = 222 $\mu$ m	45
4.8	Noise performance with W = 222 $\mu$ m	45
4.9	Z <sub>in</sub> when sweep Active Ls	48
4.10	Z <sub>out</sub> when sweep ActiveLs	48
4.11	Gain when sweep ActiveLs	49
4.12	PM when sweep ActiveLs	49
4.13	Noise when sweep ActiveLs	50
4.14	Z <sub>in</sub> when sweep ActiveLd	51
4.15	Z <sub>out</sub> when sweep ActiveLd	51
4.16	Gain when sweep ActiveLd	52
4.17	PM when sweep ActiveLd	52
4.18	Noise when sweep ActiveLd	53
4.19	Z <sub>in</sub> when sweep Cd	54
4.20	Z <sub>out</sub> when sweep Cd	54
4.21	A <sub>v</sub> when sweep Cd	55
4.22	PM when sweep Cd	55
4.23	Noise when sweep Cd	56
4.24	Final Design (simplified)	57
4.25	Final Design	58
4.26	LNA with Active L (A <sub>v</sub> )	59
4.27	LNA with Active L (PM)	59
4.28	LNA with Active L (Z <sub>in</sub> & Z <sub>out</sub> )	60
4.29	LNA with Active L (NF)	60
4.30	Layout of LNA with active inductor	62
4.31	Simulation setting for LNA with Passive L	64
4.32	A <sub>v</sub> Comparison	66
4.33	PM Comparison	66
4.34	Z <sub>in</sub> Comparison	67
4.35	Z <sub>out</sub> Comparison	67

4.36 NF Comparison

68

**LIST OF SYMBOLS**

LNA	-	Low Noise Amplifier
SoC	-	System on Chip
CG	-	Common gate
Q-factor	-	Quality Factor
$f_0$	-	Frequency of operation
NF	-	Noise factor
$Z_{in}$	-	Input impedance
$Z_{out}$	-	Output impedance
$A_v$	-	Voltage gain
dB	-	Decibel
W	-	Watt
PM	-	Phase margin
$L$	-	Inductance
$C$	-	Capacitance
$R$	-	Resistance
$R_L$	-	Inductor loss
$g_m$	-	Transconductance output
$g$	-	Output conductance
W/L	-	Transistor width and length
Active Ls	-	Active inductor at source
Active Ld	-	Active inductor at drain
$r_o$	-	Output resistance
$V_E$	-	Early voltage

$I_D$	-	Saturation current
$g_{ds}$	-	Output conductance
$C_{gd}$	-	Transistor inductance value – gate to drain
$C_{db}$	-	Transistor inductance value – drain to bulk
$C_{gs}$	-	Transistor inductance value – gate to source

**LIST OF APPENDICES**

<b>APPENDIX</b>	<b>TITLE</b>	<b>PAGE</b>
A	SPICE Transistor Parameter	79
B	Active Inductor Inductance Extraction from Impedance Simulation	81
C	Proposed LNA and Active Inductor Calculation	83
D	SPICE file for LNA with Active Inductor	97

## **CHAPTER I**

### **INTRODUCTION**

#### **1.1 Introduction**

System on Chip (SOC) design is becoming more popular nowadays. The idea to integrate the whole circuits system in a single chip has given a good advantage to the manufacturer to have smaller integrated circuit (IC) as most of the design is becoming more complex and integrated. Furthermore, they can reduce manufacturing cost and save die area.

Active inductor is one of the key elements to achieve smaller die area. Moreover, its capability to tune the inductance and Q-factor values have increased the design programmability to achieve better performance of the design. Previously, passive inductor such as spiral and bonding wire have widely used by designers. However, their usage have limits the performance as they need bigger die area and provide fix values of inductance and Q-factor. Even though active inductor gives an alternative method to provide SOC design, we need to face the drawback of active inductor as it increases power consumption and introduces higher noise. Therefore, careful design is very important to make sure the noise can be limited with moderate power consumption.

To study the idea to integrate active inductor with other circuits, Low Noise Amplifier (LNA) is chosen. LNA is very important in a receiver system which receives weak signals from an antenna and amplifies the signal to the subsequent stages. Since the signal at the antenna is comparatively weak, a good gain and Noise Factor (NF) are necessary. The noise of the whole system is reduced by the gain of the LNA and the noise of the LNA is injected directly into the received signal. Thus, the LNA needs both high gain and low noise to ensure good performance of the receiver is achieved.

To achieve better noise performance, Common-Gate (CG) architecture is suggested. Its ability to avoid noisy component at the input signal is the main key to integrate active inductor with LNA[1]. Moreover, as this architecture needs high inductance value, active inductor is becoming more reliable to use rather than passive inductor. Since noise performance is important for the LNA, a new technique is presented to shrink the noise of the active inductor and LNA. Some of the design issues such as discussion and analysis on how to improve the design performance, the design trade-off and recommendation are briefly explained in this thesis.

## **1.2 Problem Statement**

Since active inductor is a noisy circuit, a good architecture and careful design consideration needed to achieve the required performance of LNA. A good architecture for the LNA is also essential to make sure the active inductor can be replaced and can work properly as the passive inductor. As active inductor is tuneable by current, higher power consumption will be one of its drawbacks. Even though die area can be saved, some other issues need to be studied such as frequency and inductance tuning capability, noise optimization, impedance matching, narrow-band implementation and stability. Thus the problem statement of this research is what should the LNA architecture be if it were to be integrated with active inductor.



### 1.3 Objective of The Research

The objectives of this research are listed below:

- i. To analyze and understand an active inductor.
- ii. To study and analyze the performance of a LNA which uses active inductor
- iii. To design and analyze performance of Complementary Metal Oxide Semiconductor (CMOS) Common Gate LNA with On-Chip active inductor. Design is based on 1.2 um CMOS process.

### 1.4 Design Target

Design target for this research are:

- |                           |               |
|---------------------------|---------------|
| a. Input/Output Impedance | → 50 $\Omega$ |
| b. Gain ( $A_v$ )         | → >10dB       |
| c. Phase Margin (PM)      | → > 60        |
| d. Noise Factor (NF)      | → < 8dB       |
| e. Power Consumption      | → < 100mW     |

### 1.5 Methodology

The methodology of this research is listed as follows:

- i. Literature survey on CMOS LNA and active inductor architectures and designs.
- ii. Study the noise impact for the LNA and active inductor circuit.

- iii. Design the circuit of active inductor using S-Edit software. The design consideration and analysis are done.
- iv. Design the circuit of LNA using S-Edit software.
- v. All simulations and study are done using T-Spice and W-Edit software.
- vi. Integrate active inductor with LNA and study the effect of active inductor to the LNA.
- vii. Design the layout of the LNA and Active inductor using L-Edit software.
- viii. Performance analysis on schematic and layout levels design

## **1.6 Scope of Work**

The scopes of work of this research are as follows:

- i. To study active inductor performance based on tuning range, Q-factor and noise performance.
- ii. To study the effect of active inductor to LNA performance
- iii. Layout design for active inductor and LNA with performance analysis

## **1.7 Thesis Organization**

Chapter I presents the overview of the project. Chapter II reviews active inductor and LNA architecture. Chapter 3 proposes an active inductor design and presents how to integrate it to the LNA. Chapter 4 analyses design the performance based on gain, phase margin (PM), impedance matching, tuning capability and noise optimization. Chapter 5 concludes the research and proposes the future work that could improve the LNA performance, especially on power consumption and noise optimization.