Performance Analysis of Single and Dual Channel Vertical Strained SiGe Impact Ionization MOSFET (VESIMOS)

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***Abstract*— In this work, single and dual channel SiGe layer for Vertical Strained Silicon Germanium (SiGe) Impact Ionization MOSFET (VESIMOS) has been successfully analyzed. Presence of the SiGe channel, it improved the I_{ON}/I_{OFF} ratio, sub- threshold slope for the Dual Channel VESIMOS. Germanium has high impact ionization rates to ensure that the transition from OFF state to ON state is abrupt. It is found that Single Channel (SC) VESIMOS for 10% to 30% Ge mole fraction operate in Conventional MOSFET mode at VDS=1.75V. However, Dual Channel (DC) VESIMOS with the same content was operated in Impact Ionization (II) mode. For DC VESIMOS Ge=30%, it has a fastest switching speed of sub-threshold value, S=10.98 mV/dec compare to others simulated devices. It observed that drain current for SC and DC VESIMOS increase sharply initially due to presence of Germanium. However, breakdown voltage of the SC device was decrease from B_V=2.9V to 2.5V by increasing the composition of Ge from 10% to 30%. The same characteristics were found for DC VESIMOS with B_V= 2V to 1.6V by varying the Ge composition. Ge content justified the appearance of second SiGe channel and affecting the breakdown voltage. A better performance in threshold voltage, V_{TH}, S value and I_{ON}/I_{OFF} ratio were found for DC as compared to SC VESIMOS. The V_{TH}=0.6V and I_{ON}/I_{OFF} = 1×10^{13} were measured for DC VESIMOS with Ge=30% that justified the advantage of SiGe channel on VESIMOS device. These improvements were mainly affected the enhancement of electron mobility in SiGe layer from 600 m^2/V-s (first channel) to 1400 m^2/V-s (second channel). The electron mobility was increased due to splitting of conduction band valley into six fold in which the electron mass are reduced in out of plane direction and thus enhanced the mobility of electron. This was evidence that DC VESIMOS operate with low power and better performance compare to other devices.**

Keywords— Vertical Strained SiGe Impact Ionization MOSFET (VESIMOS), threshold voltage, sub-threshold slope, breakdown voltage, electron mobility.

I. INTRODUCTION

Over several decades, aggressive scaling down of electronic devices into Nano-scaled has an enormous transformation in semiconductor industry. Developer was facing several challenges to improve the device performance and package density when the semiconductor devices beyond sub-100nm [1- 2]. Low switching speed, high voltage supply requirement, high leakage current, and etc. was ordinary facing by the developer in Nano-scaled devices. MOS technology has facing theoretically sub-threshold slope, S limit of 60mV/dec at room temperature [3-6]. By scaling the bias voltage continuously, the sub-threshold slope will increase and further causing the increment of leakage current and power consumption [7]. In order to solve the sub-threshold limit, a device based on the drift mechanism of carrier's theory instead of diffusion MOSFETs (IMOS) has been developed successfully [8-12]. However, IMOS required high drain voltage (V_{DS}) to operate it and hot carrier effect was occurs when the electrons started to destroy the gate oxide of the MOS [13-14]. To overcome the problem, Vertical Impact Ionization MOSFET was introduced. It's different from the lateral IMOS, where the vertical IMOS does not based on the avalanche breakdown. However, II generating the holes and charge the p-floating body which it lead the drain current in the sub-threshold region increase rapidly. High voltage supplied is required in order to operate the vertical IMOS.

Strained SiGe technology has been used to improve the mobility recent years to scaling down the devices [15]. SIGe has smaller band gap compare to the Silicon and higher II rates in SiGe region [16-17]. To incorporate the advantages of vertical IMOS and strained SiGe technology, vertical strained SiGe IMOS have been proposed recently. There is a 4.2% of difference between the lattice constants of Si and Ge atoms [18]. The mismatch of Si and Ge was lifts both conduction and valence band degeneracy increasing the mobility of electrons and holes [1]. However, thickness of the SiGe layer and composition of the Ge is a critical parameter. If SiGe layer is above the critical thickness, it will cause misfit defects of SiGe layer [19]. Ge mole fraction, x in $Si_{1-x}Ge_x$ must be select in appropriately to avoid the performance of the device reduce [20]. However, the main limitation of using the SiGe technology is devices facing a low breakdown

voltage. The degradation of breakdown voltage was highly affecting the short channel with threshold voltage roll-off and increasing in sub- threshold slope [21].

This paper presents the effect of electrical characteristics for single (SC) and dual channel (DC) strained SiGe layer in the Vertical Strained SiGe Impact Ionization MOSFET (VESIMOS). Dual channel strained SiGe proposed to reduce the sub-threshold slope swing, reducing the supply voltage and increase the I_{ON}/I_{OFF} ratio of the device. It could overcome the short channel effects in conventional MOSFET and hot carriers effects in lateral IMOS. Enhancement of the electron mobility and the fraction of Ge will affect towards the performance of the VESIMOS. Besides that, increasing of the Ge mole fraction and the thickness of the strained layer will affect the breakdown voltage of the device. Higher breakdown voltages will favorable because it could maintain the life time of the device. Therefore, degradation of the breakdown voltage is a highly important short channel effect of nano-scaled device.

II. Device Structure

Fig. 1 shows the detailed cross sections of the DCVESIMOS which simulated for the device performance using Silvaco's package [22]. This structure comprises of an n+ doped drain region and source region, a SiGe layer is grown in the drain intrinsic zone and in the source intrinsic zone, a highly doped delta p+ layer in between the intrinsic region and double sided gates [23]. Formation of SiGe layer at drain intrinsic region will cause the impact ionization occurs strongly [24]. However, highly doped delta p+ layer will create a potential barrier and without applying a high drain – source voltage, high electric fields can be achieved in the intrinsic zone near the drain.

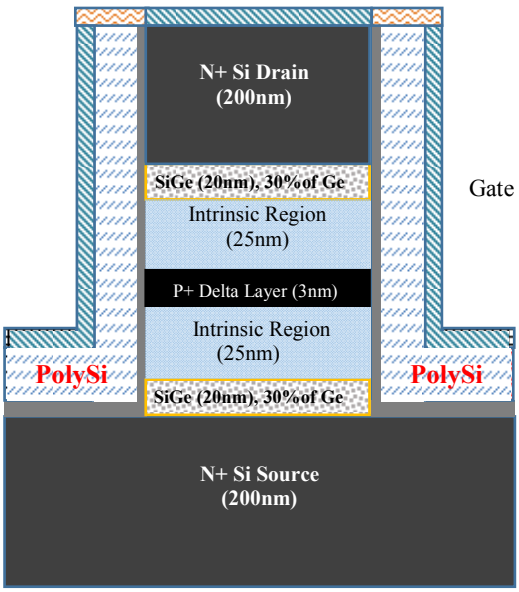

Fig. 1. Double layer SiGe VESIMOS device structure with dimension of L=93nm, d=200nm, respective thickness of source, intrinsic region, P+ delta layer, SiGe layer, drain and both layer fraction of Ge is 30%.

III. Device Concept

There are three operating modes of VESIMOS: conventional MOSFET, impact ionization mode, and bipolar transistor mode. II rates were limited by the V_{DS} and insufficient electric field in conventional MOSFET mode. The barrier was affected by the V_{GS} and electron channel is form at gate region which between the intrinsic zone and p+ delta layer. Impact ionization rate will be occurs in the drain side intrinsic zone while the V_{DS} is increase. This is mainly cause by the electric field in drain intrinsic region was increased. Therefore, it was due to the potential barrier is decreased by V_{GS} and it allows the electron across from drain to source region.

In II mode, extremely fast rise of the current in the sub- threshold region was encouraged in reducing the sub-threshold slope value. Unlike lateral IMOS, impact ionization rate does not rise the current. However, it based on the holes which generated by the II and it accumulated in delta p+ layer region to charge the body of device and causing a dynamic reduction of threshold voltage when switching ON the device. Therefore, a better sub-threshold slope and I_{ON}/I_{OFF} ratio was obtained.

The impact ionization rates were affected by the electric field in the drain intrinsic zone. II rate was increased exponentially by increasing the V_{DS} and it leads the holes current at the delta p+ layer increase. However, gate will loses its control over the drain current while delta layer cannot contain with the surge of holes current. This was causing the device operate in Bipolar Junction Transistor mode (BJT).

IV. Device Simulation

The shape and thickness of the SiGe layer and the thickness of the P+ delta layer will affects the performance of the VESIMOS [25]. Therefore, an optimum thickness of the P+ delta layer and the doping concentration was selected to obtain quality sub-threshold slope. Changes of the Germanium content will also affect the mobility in the device [26]. The strain level is related to the Ge mole fraction. The higher of the Ge mole fraction the higher of the strain level obtain in the layer. Investigation on the performance of variation Ge mole fraction from 10% to 30% for SC VESIMOS was successfully carried out. The position of the SiGe layer will need to determine carefully to achieve the higher rates of the impact ionization in the drain intrinsic region.

VESIMOS was based on the impact ionization with drift current mechanism concept, which involves high electric field. Doping concentration is required to obtain a better characteristic of the device. The source and drain was n-doped with Antimony and Phosphorus with a doping concentration of 2.1×10^{18} /cm^3 respectively. Doping concentration of P+ delta layer and intrinsic region are 1.0×10^{19} /cm^3 and 1.0×10^{19} /cm^3 respectively.

Poisson's equation and continuity equation numerically was used to investigate the electrical characteristics of the device

within the explicit defined meshes [22]. By computing the Poisson's equation, it allows to observe the electrical potential energy and electronic band structures. Current densities of the electronics and holes can be calculated by using the continuity equations. Boltzmann transport framework is use to solve the continuity equation and Poisson's equation. In the self-consistent process it will show the relationship between the current density of the electrons or holes and carrier concentration as well as quasi-Fermi potential. Selberherr's model is a local impact ionization model [27]. Generally, Selberherr's model is applied for the device simulation especially vertical impact ionization MOSFET. The drift – diffusion transport model with the Boltzmann carrier transport frame work was applied to predict the transfer characteristic of the device.

V. Device Performance And Analysis

The performance of the VESIMOS was analyzed by invoking its transfer characteristic that examined by biasing the drain voltage, V_{DS} and ramping the gate voltage, V_{GS} at defined bias steps for both single and dual channel.

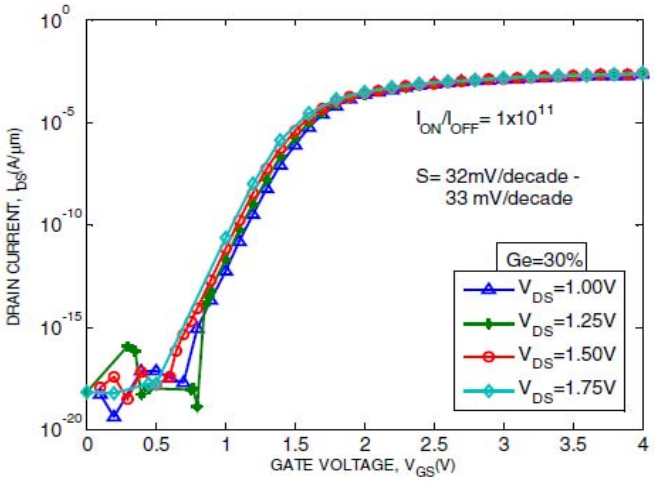

Fig. 2. Transfer Characteristics, I_D-V_G of VESIMOS for $Si_{0.7}Ge_{0.3}$

Fig. 2 shows transfer characteristics of SC VESIMOS with Ge=30% at V_{DS}=1V to 1.75V. For all V_{DS} supplied, the SC VESIMOS is found to be worked in conventional MOSFET mode only. This is due to limited V_{DS} supply that did not produce enough energy to create electron hole pair for avalanche breakdown mechanism occurring at PN junction near the drain. This occurrence was also applied for SC VESIMOS with Ge=20% and 30%. For both SC VESIMOS with Ge=10% and 20%, the off state current, I_{OFF} is below the noise level of 10^{-15}μA/μm and the on state current, I_{ON} is 10^{-3} μA/μm, which lead a I_{ON}/I_{OFF} ratio of 1×10^{12}. The sub-threshold voltage, S=23mV/dec to 32 mV/dec and S=28mV/dec to 33mV/dec were measured for SC VESIMOS with Ge=10% and 20% respectively. For Ge=30%, the S=32mV/dec to 33mV/dec and I_{ON}/I_{OFF}= 1×10^{11} were obtained.

Fig. 3 shows the comparison of transfer characteristic between SC and Dc VESIMOS with different Ge mole fraction at V_{DS}=1.75V. The SC VESIMOS is found to be operated in conventional MOSFET due to the limited of drain supply voltage for the electron to overcome the delta P+ potential barrier. However, DC VESIMOS is found to work in II mode due to sufficient energy to create an electron hole pair. DC VESIMOS with Ge=30% has lowest sub-threshold slope value of S=10.98mV/dec and trifle higher threshold voltage compare to other devices. This significant result was affected by the dual strained SiGe layer which able to enhance the electron mobility based on the splitting of the valley that will be discussed later in [28-29].

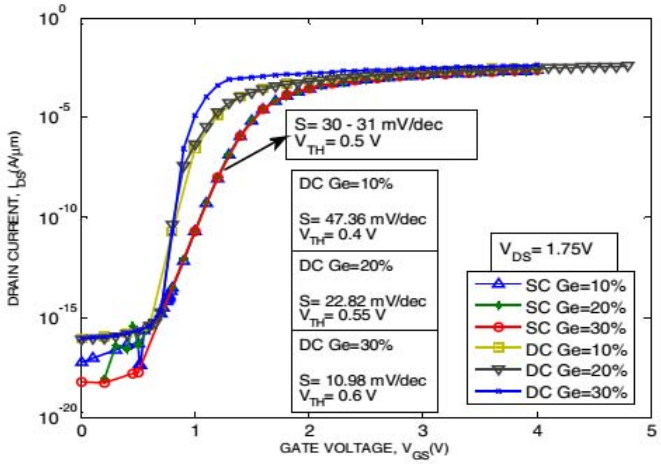

Fig. 3. Comparison of transfer characteristics, I_D-V_G of variation Ge mole fraction for SC and DC VESIMOS at V_{DS}=1.75V

Breakdown voltage of the VESIMOS was analyzed by invoking its output characteristic that examined by biasing the gate voltage, V_{GS} and ramping the drain voltage, V_{DS} at defined bias steps for both single and dual channel devices.

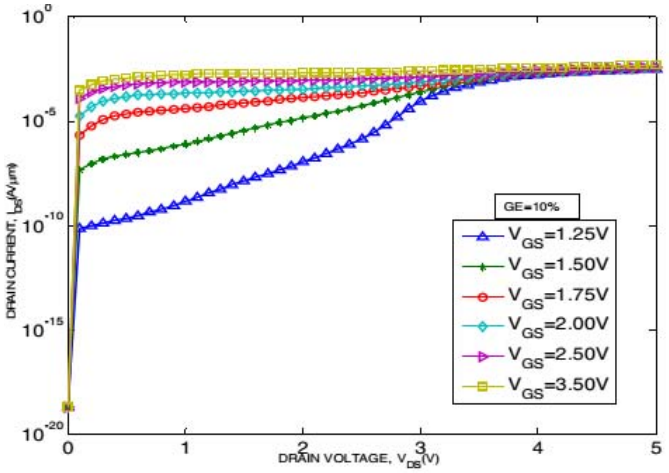

Fig. 4. Output Characteristics, I_D-V_D of VESIMOS for $Si_{0.9}Ge_{0.1}$ at different V_{GS}

Fig. 4 shows the output characteristic of SC VESIMOS with Ge=10% by supplying different V_{GS}. It can be seen that the drain current grew enormously initially, and then increase considerably before going into saturation for V_{GS}<1.75V. Breakdown voltage was occurred at V_{DS}>3.5V. The same occurances was also applied for SC VESIMOS with Ge=20% and 30%. The sharp rise of initial drain current was attributed

to the presence of the Germanium. Germanium has great and symmetric II rates, which ensures that the transition from OFF state to ON state is abrupt [8].

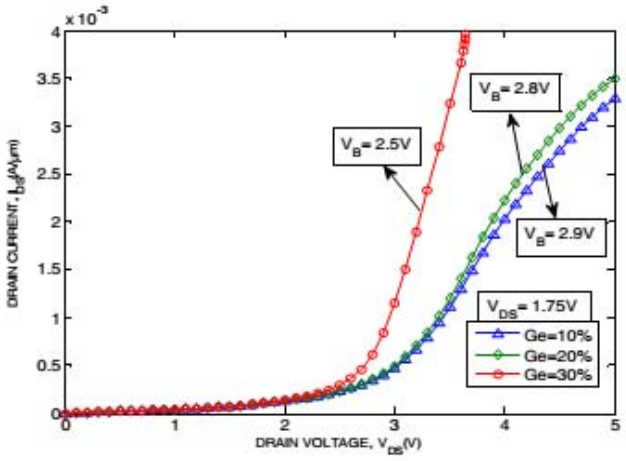

Fig. 5. Output Characteristics, I_D-V_D of variation Ge mole fraction for Single Channel VESIMOS

Fig. 5 shows the output characteristics of SC VESIMOS with variation of Ge mole fraction at V_{GS}=1.75V. The breakdown voltage for Ge=10% is 2.9V, 2.8V of breakdown voltage for Ge=20% and lowest breakdown voltage, 2.5V for Ge=30%. It can be seen that the breakdown voltage was decreased when there is an increase of the Ge mole fraction. The same occurrences was also applied for DC VESIMOS at V_{GS}=1.75V as depicted in Fig. 6.

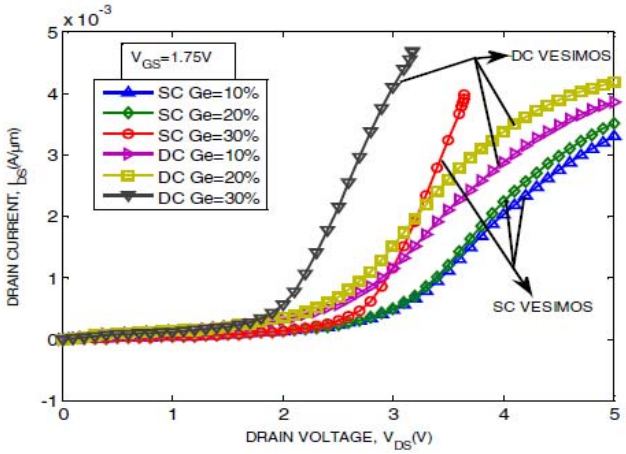

Fig. 6. Comparison of output characteristics, I_D-V_D of variation Ge mole fraction for Single Channel and Double Channel VESIMOS

It is shown that DC VESIMOS breakdown voltage was lower compare to SC VESIMOS due to the appearance of second channel of SiGe layer. The breakdowns voltages are reduce rapidly by increasing the mole fraction of Ge and appearance of second layer. The lower band gap of the semiconductor materials and the thickness of the channel lead to low breakdown voltage [30]. Lower breakdown voltage is not beneficial because it could potentially reduce the lifetime of the device. However, faster switching speed and lower I_{ON}/I_{OFF} ratio were obtained with the presence of second SiGe layer.

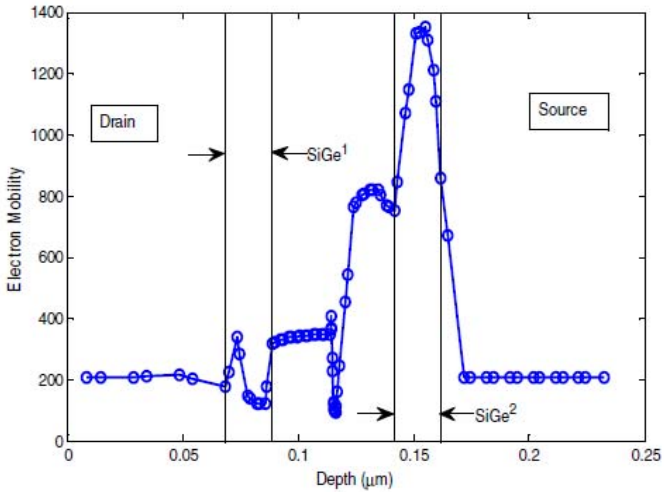

Fig. 7. Electron mobility versus depth of double SiGe VESIMOS for V_{DS}=1.75V

Fig. 7 shows the electron mobility versus the depth of DC VESIMOS which taken as cut line in Fig. 1. SiGe layer could enhance the electron mobility and the mobilities in strained layer depend on the transport direction which is perpendicular or parallel to the original SiGe growth [15], [28], [29], [31]. Si and Ge have indirect band gaps with values of 1.12eV and 0.66eV at room temperature, respectively. Conduction band and valence band of semiconductors consists of number of sub bands. Due to compressive strain, SiGe takes the lattices constant of the underlying Si substrate.

The electron mobility is a direction dependent in which the electron mobility increased in the out of plane direction and decreased when in plane direction due to splitting of the valleys in a conduction band into lower four-fold and higher two-fold states (Fig.8) [1]. The shaded regions in Fig. 8 are the four fold out-of-plane valleys and the unshaded regions are lowered below the two fold in-plane valleys. The two out-of-plane valleys (lower transport mass) drop in energy and hence, the electrons move to populated these lower mass valleys.

In VESIMOS, the electrons are moved towards the drain region while holes are transported in opposite direction when a bias was applied. Initially, electron mobility in the drain region is approximately 200m^2/V-s. From the observation, electron mobility increased sharply in both strain SiGe region where the electrons mobility increased up to 350 m^2/V-s for first SiGe layer and approximately 1400 m^2/V-s for second SiGe layer. Based on the observation, electrons mobility will decrease while at in plane direction due to heavy longitudinal electron and the electron mass are reduce at out of plane direction and cause the electron mobility to be increased. While the electron mobility increase with the selected voltage supply (V_{DS}=1.75V), electron able to overcome the potential barrier energy level and cause the device to operate in II mode.

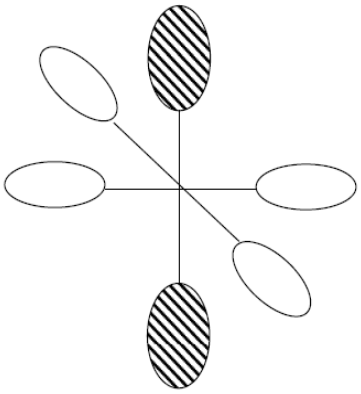

Fig. 8. Splitting of the six-fold degeneracy of the conduction band in compressively strained SiGe.

TABLE I.

PERFORMANCE COMPARISON OF SINGLE & DUAL STRAINED CHANNEL VESIMOS

	SC	**SC**	**SC**	**DC**	**DC**	**DC**
Ge^1	10%	20%	30%	10%	20%	30%
Ge^2	-	-	-	10%	20%	30%
V_{TH}(V)	0.55	0.53	0.51	0.4	0.55	0.6
B_V(V)	2.9	2.8	2.5	2.0	1.8	1.6
S (mV/dec)	31.4	30.64	30.61	47.36	22.82	10.98
I_{ON} (µA/µm)	10^{-3}	10^{-3}	10^{-4}	10^{-3}	10^{-3}	10^{-3}
I_{OFF} (µA/µm)	10^{-15}	10^{-15}	10^{-15}	10^{-16}	10^{-16}	10^{-16}
Ratio (I_{ON}/I_{OFF})	10^{12}	10^{12}	10^{11}	10^{13}	10^{13}	10^{13}

Table I summarize the performance comparison of SC and DC VESIMOS. It can be observed that the device performance has improved in term of sub-threshold by increasing the Ge mole fraction for DC devices. Besides that, the OFF state current for DC devices is much smaller compare to SC devices with the appearance of second SiGe layer. This significant result was due to the dual channel which able to enhance the electron mobility to improve the Ion/Ioff. In order to decrease the OFF state current, it involved two main criteria, which are energy gap and drain voltage. Decreasing of the source voltage and smaller band gap energy lead to the decrease the OFF state current. Due to lower band gap energy, thickness of composition layer, and appearance of second layer to improve the Ion/Ioff, it results in the reduction of the breakdown voltage severely. Therefore, DC VESIMOS required low supply voltage to operate the device and a faster switching speed obtained compare to SC VESIMOS. A low OFF state current was observed in DC VESIMOS where the device has a low leakage current. This proved that DC VESIMOS can be operated with low power and has a better performance compare to other devices.

TABLE II.

PERFORMANCE COMPARISON OF IMOS WITH DIFFERENCE TECHNOLOGIES

	DC VESIMOS	**[13]**	**[32]**	**[23]**
Device	Dual Layer SiGe	Single Layer SiGe	DP-VESIMOS	VESIMOS
S (mV/dec)	10.98	9.8	23.7	20
I_{ON}/I_{OFF}	10^{13}	10^{12}	10^{10}	10^{8}
V_{Th} (V)	0.6	0.88	1.37	-

Table II summarize the main results achieved with the vertical device with those of the single layer SiGe [13], Dielectric Pocket VESIMOS [32], and vertical MOSFET [23]. The threshold voltage of vertical MOSFET was unstable and has lower ON/OFF current ratio compare to the single layer SiGe VESIMOS. However, it solved the hot carrier effect which occurred in the lateral IMOS. The ON/OFF current ratio of DC VESIMOS is necessary to improved up to a factor of 5 and at the same time the threshold voltage observed is significantly improved compare to other technology. Lastly, the highest ON/OFF current ratio leads to a low power consumption and leakage current in the device.

VI. Conclusion

SC and DC VESIMOS were successfully been simulated and analyzed by using the TCAD simulation tools. It was found that SC VESIMOS has no improvement in sub-threshold slope when the Ge composition increased. However, with the appearance of the second SiGe layer, sub-threshold slope and the OFF state current of the device were improved. Instead, the breakdown voltage of the devices was affected by the composition of Ge and appearance of second SiGe layer. For DC VESIMOS with Ge=30%, it is prominent operate at impact ionization mode with lower V_{TH}=0.6V, I_{ON}/I_{OFF}= $1\times10_{13}$ and lower sub threshold voltage of S=10.98mV/dec compared to SC VESIMOS. This is due to DC able to enhance the electron mobility based on the splitting of conduction band valley philosophy. With the lower band gap energy, thickness of composition layer, and appearance of second channel was lead to improve the I_{ON}/I_{OFF} and sub-threshold slope, however it occasioned reducing the breakdown voltage. Therefore, DC VESIMOS able to operate with low power and better performance characteristics compare to SC VESIMOS.

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