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Research Article

Design and Performance Analysis of 1-Bit FinFET Full Adder Cells for Subthreshold Region at 16 nm Process Technology

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The scaling process of the conventional 2D-planar metal-oxide semiconductor field-effect transistor (MOSFET) is now approaching its limit as technology has reached below 20 nm process technology. A new nonplanar device architecture called FinFET was invented to overcome the problem by allowing transistors to be scaled down into sub-20 nm region. In this work, the FinFET structure is implemented in 1-bit full adder transistors to investigate its performance and energy efficiency in the subthreshold region for cell designs of Complementary MOS (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission Gate (TG), and Hybrid CMOS (HCMOS). The performance of 1-bit FinFET-based full adder in 16-nm technology is benchmarked against conventional MOSFET-based full adder. The Predictive Technology Model (PTM) and Berkeley Shortchannel IGFET Model-Common Multi-Gate (BSIM-CMG) 16 nm low power libraries are used. Propagation delay, average power dissipation, power-delay-product (PDP), and energy-delay-product (EDP) are analysed based on all four types of full adder cell designs of both FETs. The 1-bit FinFET-based full adder shows a great reduction in all four metric performances. A reduction in propagation delay, PDP, and EDP is evident in the 1-bit FinFET-based full adder of CPL, giving the best overall performance due to its high-speed performance and good current driving capabilities.

1. Introduction

The latest and innovative silicon technology processes have led to the rapid growth of modern integrated chip (IC). The development has enabled commercial IC foundry and global semiconductor industry to produce compact, high performance, low power, and robust microprocessor. The core of each microprocessor is the central processing unit (CPU) where the arithmetic logic unit (ALU) is located and forms the fundamental building block. ALU can perform logical operation and basic arithmetic, namely, addition, subtraction, multiplication, and division. Essentially, the aforementioned arithmetic operation can be summed up as follows: addition, negative addition, repeated addition, and repeated negative addition. In the digital system, it is crucial to have a full adder that is low in power consumption, of high speed, energy efficient, and reliable [1]. Compared to conventional MOSFET technology, the new FinFET technology can be implemented in 1-bit full adder, to prolong silicon downscaling and enhance the device performance and energy efficiency of full adder.

There are four types of cell designs used for FinFET-based full adder in this study, which are the Complementary MOS (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission Gate (TG), and Hybrid CMOS (HCMOS). The circuit development and simulation were performed using HSPICE and Cosmoscope. The design libraries were adapted from the Predictive Technology Model (PTM) for

conventional FET technology and BSIM CMG Models for FinFET technology. The four metric performances of 1-bit full adder were analysed: the propagation delay, average power dissipation, power-delay-product (PDP), and energy-delay-product (EDP) based on all four cell designs.

The ITRS reported an issue on the scaling process of MOSFET to 32 nm in year 2006. The issue emphasized that scaling planar bulk CMOS into a smaller size faced a lot of challenges due to the high doping that was needed, band-to-band tunneling across the junction, and difficulty in adequately controlling short channel effect (SCE). However, the problem of scaling MOSFET into the nanoscale region was solved by implementing new structures such as an ultrathin body fully depleted silicon-on-insulator (SOI) and multiple-gate FET (FinFET) [2].

2. FinFET Overview

The degradation of the device performance was the result of the scaling process of MOSFET as it approached the technology limit at 20 nm. The new alternative structure, FinFET, replaces the conventional MOSFET which allows transistors to be scaled down and may contribute to more advantages over the conventional MOSFET, such as a larger drain current, smaller switching voltage, and significantly less static leakage current. The FinFET technology was developed by Liu; well-known researchers of the University of California, Berkeley [3]. FinFET which normally refers to a nonplanar with multiple-gate is built on a SOI or bulk silicon wafer that can be fabricated using an existing CMOS compatible technology such as lithography [4]. The microprocessor manufacturers such as Motorola, AMD, and IBM widely use the FinFET term to define their double-gate development efforts. A FinFET with insulator material across the top of the channel is a dual-gate transistor although it is a Tri-Gate structure. Those with a thin insulator on top and on the sides are called Tri-Gate transistor. In September 2012, the full-service semiconductor foundry, GlobalFoundries, planned to offer a 14 nm process technology FinFET three-dimensional transistor in the year 2014 [5]. In October 2012, the Taiwan Semiconductor Manufacturing Company (TSMC) planned to make 20 nm chips in 2013 and 14 nm FinFET chips in 2014 [6].

FinFET is also called multigate device where its mode of operation is almost similar to the conventional MOSFET transistor. FinFET also has a source, drain, and gate terminal to control the flow of current. The only feature that makes FinFET differ from MOSFET is the channel between source and drain of FinFET. The channel of FinFET on top of the silicon substrate is designed as a three-dimensional bar, which is called a "fin." The three-dimensional bar design makes the gate of FinFET fully covered around the channel, as shown in Figure 1, to form several gate electrodes on each side. These electrodes may contribute to reduce leakage effects and improve drive current. Based on the design structure, the fin height of a single-fin FinFET must be half of the effective channel width, W_{eff} [10]. However, if the W_{eff} is large, FinFET can be built by utilizing multiple parallel fins

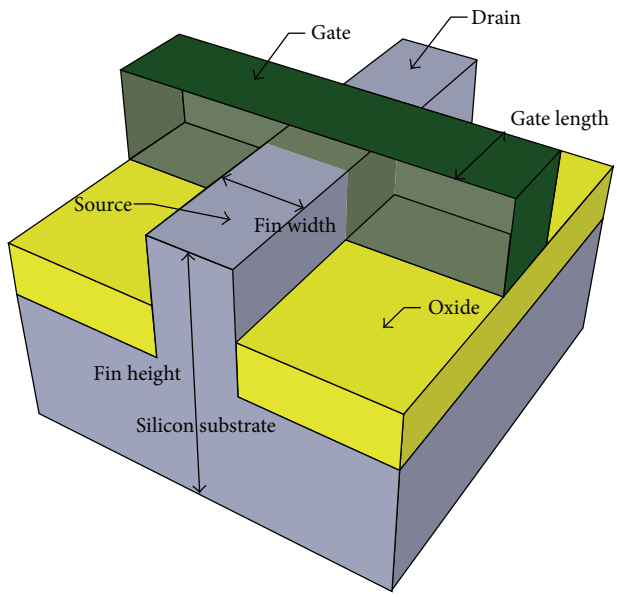

Figure 1: Basic structure of FinFET model.

to provide higher drive current strengths per unit area than planar devices. The W_{eff} of FinFET is given by

$$W_{\text{eff}} = \text{NFIN} \times (\text{TFIN} + 2\text{HFIN}), \quad (1)$$

where NFIN is the number of fins aligned in parallel, while TFIN is the thickness of the fin and HFIN is the height of the FIN (HFIN) [11].

3. Subthreshold Conduction

In theory, the current-voltage relationship suggests that the drain current, I_{DS}, of a transistor is ideally zero as the gate-to-source voltage, V_{GS}, is lower than the threshold voltage, V_{th} [12]. However, the drain current is not necessarily zero when $V_{\text{GS}} < V_{\text{th}}$. The current that exists in this region is called the subthreshold current and the transistor is in a weak inversion mode [12, 13]. The current does not drop abruptly but drops gradually to zero and it is said that the transistor is partly conducting voltage in the subthreshold region [14]. In this region, the diffusion of carriers controls the flow of the drain current instead of drift mechanism [12]. Most digital applications do not need subthreshold current because it deviates the ideal behavior of the transistor [14], causes leakage current, and limits the performance of the circuit [15]. Conversely, the carriers in the subthreshold region have become more significant in the performance of the device as the technology has evolved into the nanoscale region and runs on low power technology [15, 16].

4. The 1-Bit Full Adder Cell Designs

One of the most basic arithmetic operations used in any digital electronic system is addition. The common adder cell

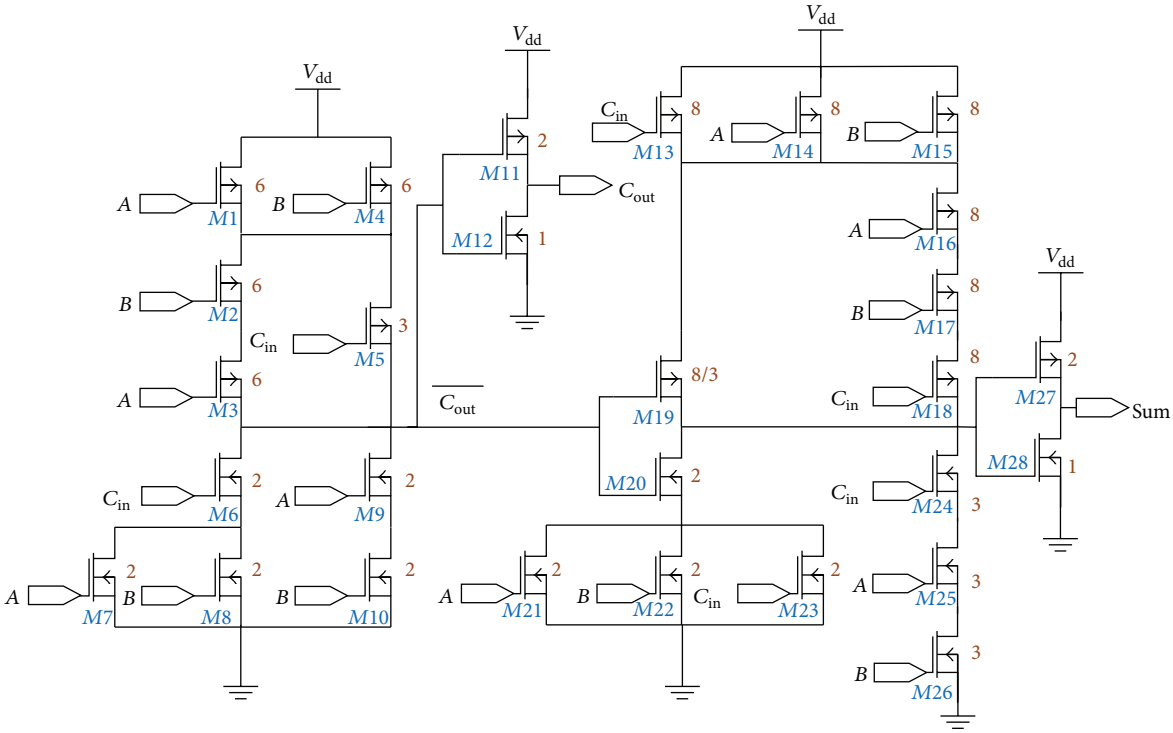

Figure 2: CMOS 1-bit full adder circuit (adapted from [7]).

Table 1: The truth table of 1-bit full adder.

Input			Output	
A	B	C_{IN}	C_{OUT}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

used is the full adder, where three inputs are added together to produce two outputs as shown in the following equations:

$$\text{Sum} = A \oplus B \oplus C_{IN} \quad (2)$$

$$C_{OUT} = A \cdot B + C_{IN}(A \oplus B). \quad (3)$$

Both (2) and (3) are generated from the truth table of 1-bit full adder as tabulated in Table 1.

Numerous types of 1-bit full adder cells with different numbers of transistors and performance tradeoffs in speed and power are designed and identified. With any cell design, there are advantages and disadvantages that are observed in this simulation work. The four types of 1-bit full adder cell designs are Complementary MOS (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission Gate (TG), and Hybrid CMOS (HCMOS).

4.1. 1-Bit Complementary MOS (CMOS) Full Adder. The CMOS full adder has 28 transistors which consists of PMOS and NMOS transistors [17]. This type of full adder is designed by implementing (2) and (3) as shown in Figure 2. The design is very reliable in subthreshold voltage due to its high noise margin [7]. CMOS full adder consumes more energy, has high number of input loads, and requires more silicon area in wafer because of its high transistor count. There is also additional delay at Sum which is generated from $\overline{C_{out}}$ to the input of transistors M19 and M20 of Figure 2 [8].

4.2. 1-Bit Hybrid CMOS (HCMOS) Full Adder. This full adder design is the combination of transmission gates, pass-transistors, PMOS, and NMOS transistors as proposed in [18]. It consists of 20 transistors as shown in Figure 3. This design has overcome several disadvantages that have been identified in previous cell designs. This design has a lower transistor count and high noise immunity and it has been revealed that HCMOS full adder has less power dissipation when compared to CPL full adder [18]. On the other hand, this hybrid design also has its advantages including a relatively lower propagation delay than CPL, TG, and CMOS full adder. It is also revealed that the power-delay-product (PDP) of HCMOS full adder is the lowest of them all.

4.3. 1-Bit Complementary Pass-Transistor Logic (CPL) Full Adder. Another type of 1-bit full adder cell is CPL, which has 32 transistors in this cell design as shown in Figure 4. It is made of NMOS pass-transistors and has cross-coupled

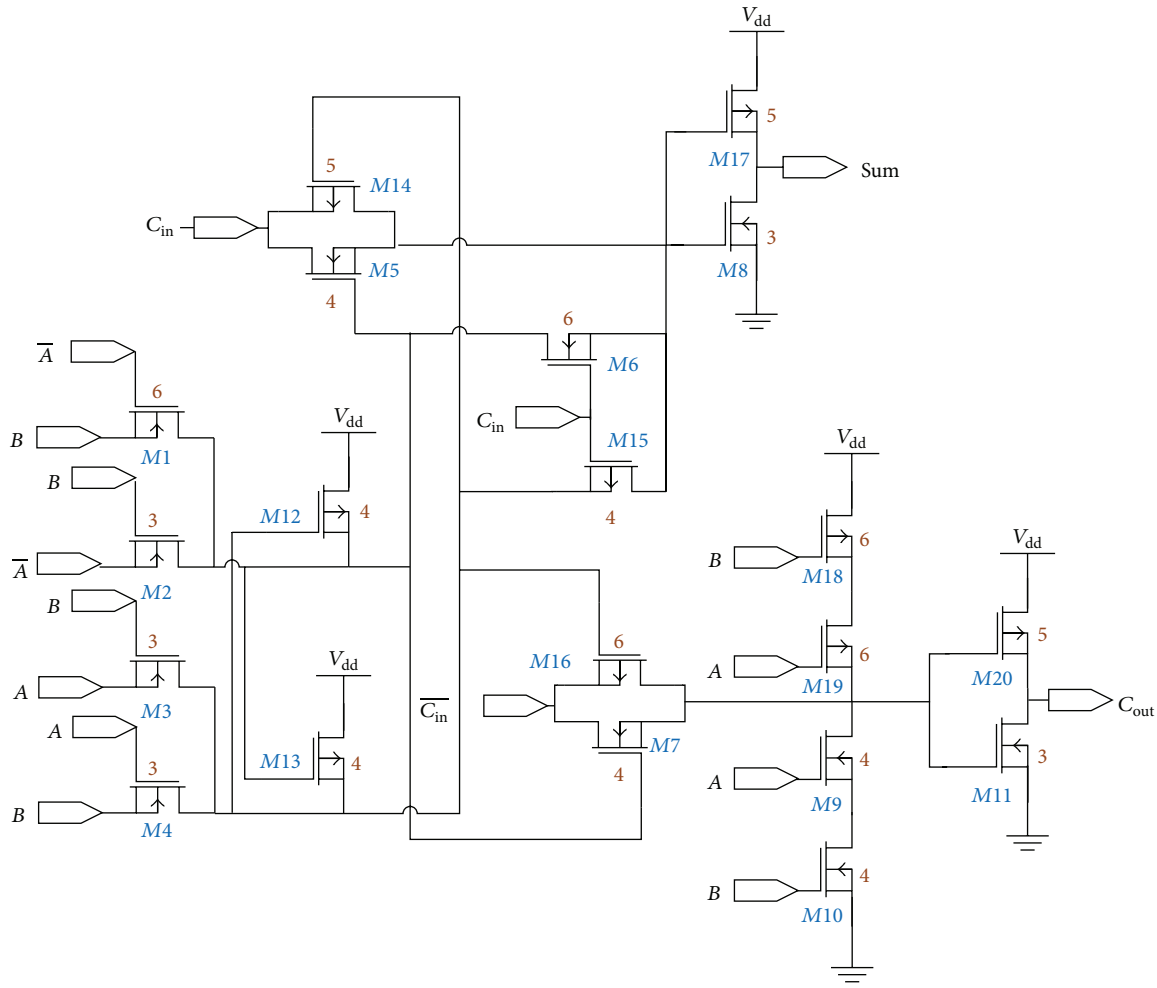

Figure 3: HCMOS 1-bit full adder circuit (adapted from [8]).

PMOS transistors added to the design to achieve level restoration [17]. This cell design provides high-speed performance and full swing operation and has a good driving capability because of the static inverters' output [18]. However, the disadvantage of the CPL full adder is that it has many intermediate nodes and variable C_{out} with its complement is generated at the outputs [8]. Overloading inputs in the design may cause high capacitance [8], while a high transistor count may contribute to a higher power dissipation [18].

4.4. 1-Bit Transmission Gate (TG) Full Adder. As illustrated in Figure 5, this full adder has 20 transistors, which consists of transmission gates, PMOS, and NMOS transistors. High-speed operation and low power dissipation performance are contributed by the transmission gate transistors used in the design [18]. The TG full adder circuit is simple compared to CMOS and CPL with fewer transistors, fewer intermediate nodes, lower input loading, and balanced generation of output. However, the TG full adder has higher power dissipation compared to CMOS full adder [7]. Previous work [17] has shown that the propagation delay may increase excessively if the TG full adder is cascaded in series.

5. Transistor Sizing

The current-voltage (I-V) characteristics of both n-type and p-type transistors are used to determine the size of a single n-type and p-type transistor in both MOSFET and FinFET technologies. The I-V characteristics are simulated to get a fairly optimum positive and negative drain current of n-type and p-type transistors and to obtain an almost symmetrical graph for the constructed logic gates. The 16 nm length is set for both MOSFET and FinFET to offer an insight into the device performance of next generation 16 nm process.

A high performance transistor with low power is essential for future technology and thus the bias voltage of MOSFET and FinFET is set in the range from 0 V (initial voltage) to 0.2 V (final voltage) for NMOS and vice versa. The I-V characteristics are computed by initially defining the parameters of MOSFET and FinFET. Next, the bias point is inserted to evaluate the output current for every input current. An appropriate number of bias point should be set to reduce the computation time. The iteration is finished once it reached the final voltage. Thus, the I-V characteristics are plotted. The parameters that can deliver the optimum performance of transistor are chosen.

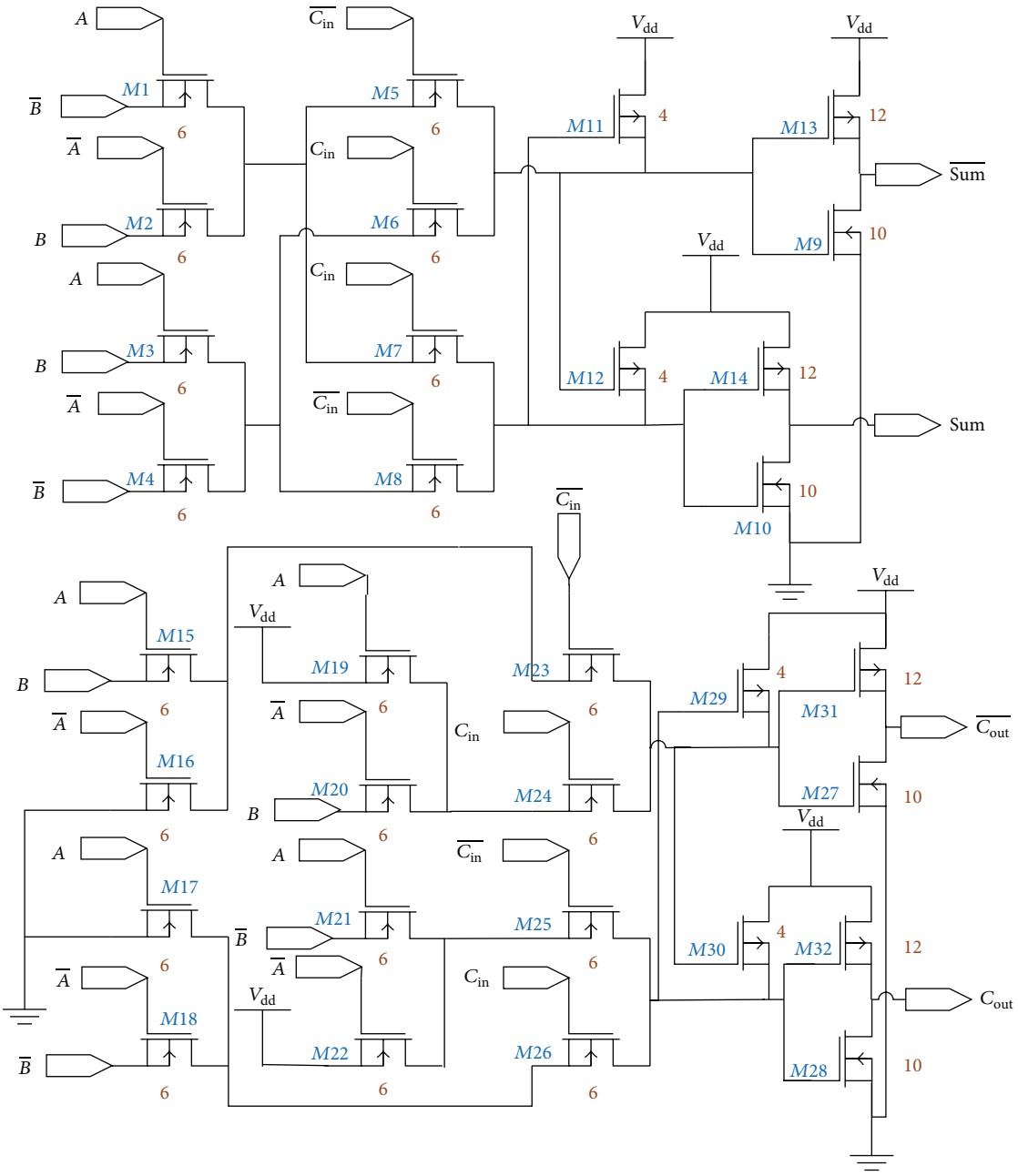

Figure 4: CPL 1-bit full adder circuit (adapted from [8]).

Figure 6 shows the combination of the I-V characteristics of both n-type and p-type MOSFET (i.e., PMOS and NMOS) transistors. For MOSFET, the gate length of both n-type and p-type transistors is kept constant at 16 nm. The transistors were simulated in HSPICE to obtain the optimized parameter of width with a specific amount of current flowing through the drain, approximately at 61.5 nA and 48 nA for n-type and p-type, respectively. The optimized parameter of width of both n-type and p-type MOSFET is tabulated in Table 2.

The parameters in Table 2 are used for a single transistor for both n-type and p-type transistors. However, a full adder cell design has several transistors connected in series or in parallel. In this case, the size of the transistors must be increased so they have the same conductance as that of n-type or p-type single transistor. For example, as shown in Figure 2, the CMOS full adder has several transistors connected in

Table 2: Optimized parameters for PMOS and NMOS transistors (MOSFET).

Transistor	Width (nm)	Length (nm)
PMOS	16.00	16.00
NMOS	32.00	16.00

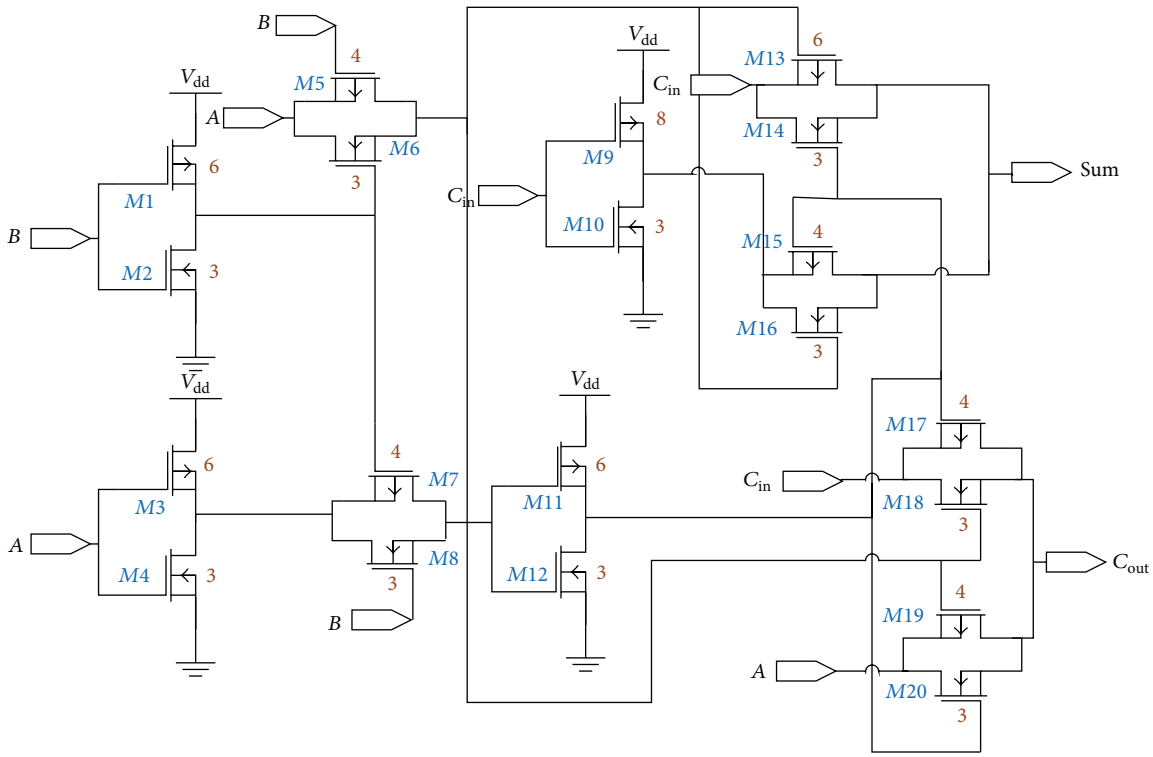

Figure 5: TG 1-bit full adder circuit (adapted from [9]).

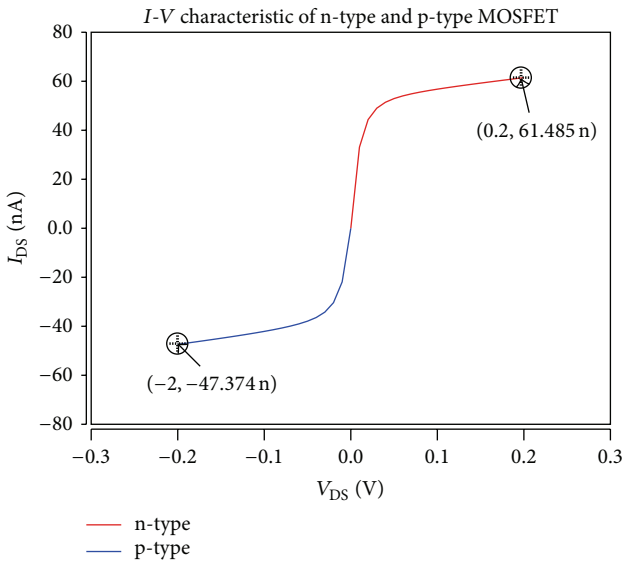

Figure 6: Graph of I_{DS} versus V_{DS} of MOSFET.

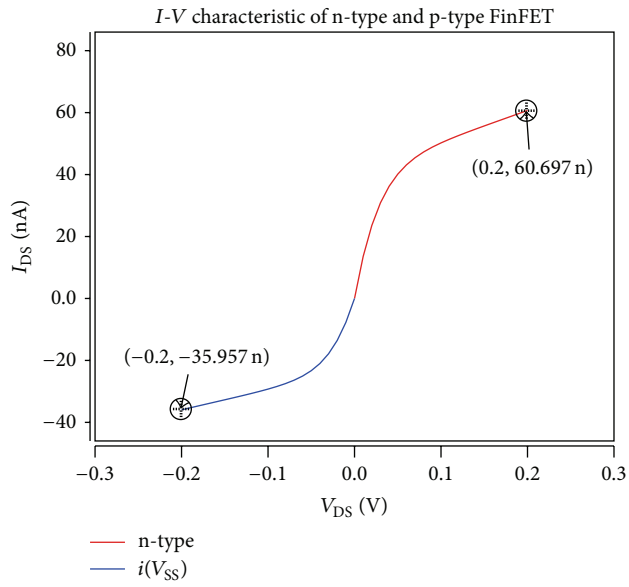

Figure 7: Graph of I_{DS} versus V_{DS} of FinFET.

series or in parallel. The size of transistors in parallel must be equal, while the size of transistors in series must be increased according to the logical effort. The same concept must be applied for the rest of the cell designs.

The plots of I_{DS} versus V_{DS} of both n-type and p-type FinFET are as shown in Figure 7. The gate length, L, of both n-type and p-type FinFET is kept the same as MOSFETs. The parameters such as the height of fin (HFIN), the thickness of fin (TFIN), and the number of fins (NFIN) are chosen carefully to obtain a matching drain current of n-type and p-type FinFET against MOSFET. From our simulation, we suggest that the respective values of TFIN and HFIN for all n-type and p-type channel to be kept consistent as shown in Table 3 for simplicity in computational and fabrication process. The chosen TFIN and HFIN provide the closest

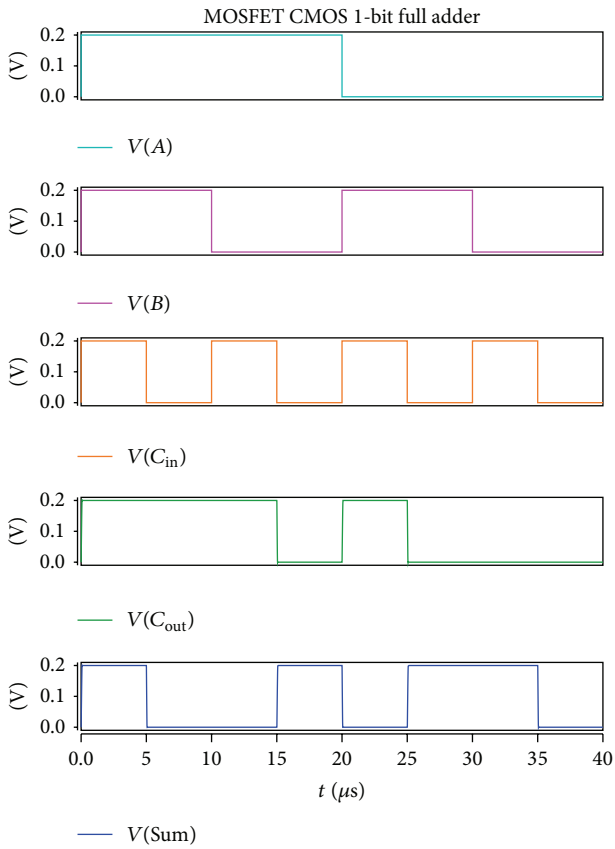

Figure 8: Input and output waveforms of MOSFET-based CMOS full adder.

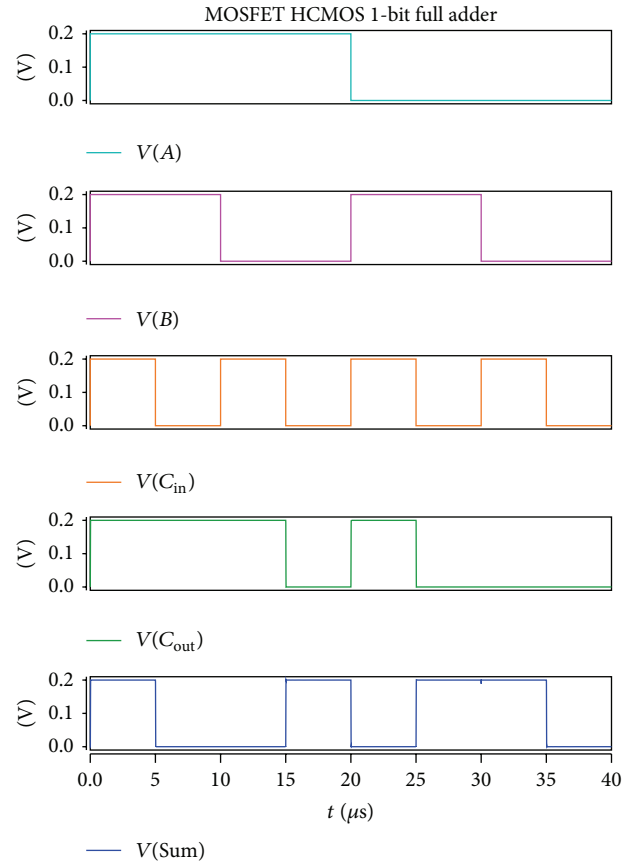

Figure 9: Input and output waveforms of MOSFET-based HCMOS full adder.

matching drain current of a MOSFET when NFIN of FinFET is varied from 1 to 10. The tradeoff of this simulation method would be that there is slight discrepancy of drain current for n-type compared to p-type. Table 3 tabulates the values of parameters of FinFET transistors.

The parameters in Table 3 are used for a single transistor of both p-type and n-type FinFET transistors. The sizing of transistors in series or in parallel must be increased so that they have the same conductance as the corresponding transistor in the circuit design. For FinFET, the NFIN are increased to yield a larger effective width, W_{eff}, as in a MOSFET. This trend is observed from Table 4 where the discrete number of NFIN in FinFET can be increased to match the current of a MOSFET. Note that (1) is used to calculate the sizing of transistors in series or in parallel by multiplying the discrete value of NFIN.

6. 1-Bit Full Adder Waveforms

The output waveforms of all four types of 1-bit full adder cell designs are as shown in Figures 8–11. All of the figures show the input and output waveforms generated from the HSPICE simulation. The output Sum and C_{OUT} produced are as expected in the truth table as tabulated in Table 1.

For FinFET technology, the input and output waveforms of 1-bit CMOS, CPL, TG, and HCMOS full adder are illustrated in Figures 12, 13, 14, and 15, respectively. Similar as in MOSFET full adder, the outputs generated are as expected in the truth table. In Figures 12 and 13, the outputs generated show some glitches because of a high transistor count in CMOS and CPL full adder cell design [7, 18]. The output waveforms of TG full adder in Figure 14 showed an obvious delay in rising and falling due to the transmission gate transistors used in the cell design. The propagation delay of transmission gates full adder will increase if the gates are cascaded in series [17], whereas the waveform of HCMOS full adder (Figure 15) is comparable to Figure 14 because the transmission gate transistors are also present in the cell design of CMOS and CPL transistors [18].

Table 3: The values of parameters for n-type and p-type FinFET transistors.

Types of FinFET	n-type	p-type
Number of fins, NFIN	1	1
Gate length, L (nm)	16.00	16.00
Height of fin, HFIN (nm)	10.00	17.00
Thickness of fin, TFIN (nm)	10.00	17.00

Table 4: The values of drain current of FinFET and MOSFET transistors.

Number of transistors in series	MOSFET		FinFET			
	Width (nm)	Current (nA)	TFIN (nm)	HFIN (nm)	NFIN	Current (nA)
n-type						
1	16.00	61.49	10.00	10.00	1	65.79
2	32.00	97.08	10.00	10.00	2	131.57
3	48.00	166.23	10.00	10.00	3	197.36
4	64.00	235.19	10.00	10.00	4	263.14
8	128.00	510.75	10.00	10.00	8	526.29
10	160.00	648.18	10.00	10.00	10	657.86
p-type						
2	32.00	47.37	17.00	17.00	2	63.32
4	64.00	116.38	17.00	17.00	4	126.64
5	80.00	150.86	17.00	17.00	5	158.30
6	96.00	185.33	17.00	17.00	6	190.00
8	128.00	254.26	17.00	17.00	8	253.30
8/3	42.66	70.377	17.00	19.00	2	70.77
9	144.00	288.73	17.00	17.00	9	283.90
12	192.00	392.11	17.00	17.00	12	379.90

Table 5: Propagation delay of MOSFET and FinFET full adder.

Full adder	Propagation delay (s)	
	MOSFET	FinFET
CMOS	3.08×10^{-8}	4.93×10^{-9}
HCMOS	9.39×10^{-9}	1.75×10^{-9}
CPL	1.97×10^{-8}	1.93×10^{-9}
TG	2.82×10^{-8}	2.93×10^{-9}

Table 6: Average power dissipation of MOSFET and FinFET full adder.

Full adder	Average power dissipation (W)	
	MOSFET	FinFET
CMOS	2.30×10^{-9}	8.41×10^{-10}
HCMOS	1.40×10^{-9}	3.17×10^{-10}
CPL	1.69×10^{-9}	5.23×10^{-10}
TG	1.74×10^{-9}	7.41×10^{-10}

7. Metric Performance Analysis

In this study, four metric performances were analysed: propagation delay, average power dissipation, power-delay-product (PDP), and energy-delay-product (EDP). These metrics were measured in 1-bit full adder of CMOS, HCMOS, CPL, and TG for both MOSFET and FinFET technology. Each of the cell designs is implemented to determine the optimal tradeoff between delay-energy-power in planar and nonplanar transistors for modern digital systems [14].

The bar graph of the propagation delay of both MOSFET-based and FinFET-based full adder is illustrated in Figure 16, which is tabulated from Table 5. Based on Figure 16, the 1-bit CPL full adder shows the most improved performance compared to other full adder cell designs because this design has high-speed performance with full swing operation [18]. The FinFET-based full adder showed a large reduction in delay and provided the device with high-speed performance, which is better than the conventional MOSFET-based full adder. These results showed that FinFET has better and faster switching speed due to the presence of multiple gates in the FinFET structure [9] and drives more current through the transistor compared to the MOSFET structure [17].

The average power dissipation in MOSFET-based and FinFET-based full adders is tabulated in Table 6 and the graph is plotted in Figure 17. The average power dissipation for FinFET-based full adder reduced greatly compared to MOSFET-based full adder, which can be seen in Figure 17. The presence of multiple gates in the FinFET structure reduces the short channel effects (SCE). This enhances the subthreshold slope, which increases the gate oxide thickness. An increase in oxide thickness will lessen the gate leakage current, thus reducing the total power dissipation.

The power-delay-product (PDP) is used to measure the average energy consumed per switching event while the energy-delay-product (EDP) is another important metric that unifies a measure of performance and energy. The equations of PDP and EDP are as follows:

$$\text{PDP [J]} = \text{Propagation Delay} \times \text{Average Power Dissipation} \quad (4)$$

$$\text{EDP [Js]} = \text{PDP} \times \text{Propagation Delay}. \quad (5)$$

The values of propagation delay and average power dissipation of both MOSFET and FinFET full adder as tabulated in Tables 5 and 6 are calculated according to (4) and (5) and then the values are tabulated in Table 7.

The values of PDP and EDP for both MOSFET-based and FinFET-based full adder were tabulated in Table 7. In Figure 18, we observed that FinFET-based full adder has a

Table 7: Power-delay-product (PDP) and energy-delay-product (EDP) of MOSFET and FinFET full adder.

Full adder	Power-delay-product, PDP (J)		Energy-delay-product, EDP (Js)	
	MOSFET	FinFET	MOSFET	FinFET
CMOS	7.09×10^{-17}	4.14×10^{-18}	2.18×10^{-24}	2.04×10^{-26}
HCMOS	1.31×10^{-17}	5.54×10^{-19}	1.23×10^{-25}	9.67×10^{-28}
CPL	3.32×10^{-17}	1.01×10^{-18}	6.55×10^{-25}	1.94×10^{-27}
TG	4.90×10^{-17}	2.17×10^{-18}	1.38×10^{-24}	6.34×10^{-27}

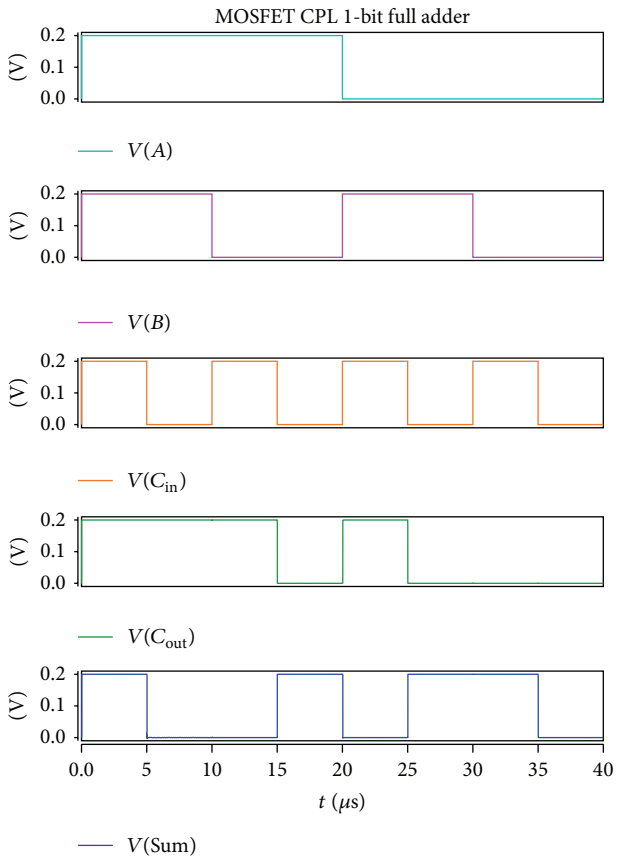

Figure 10: Input and output waveforms of MOSFET-based CPL full adder.

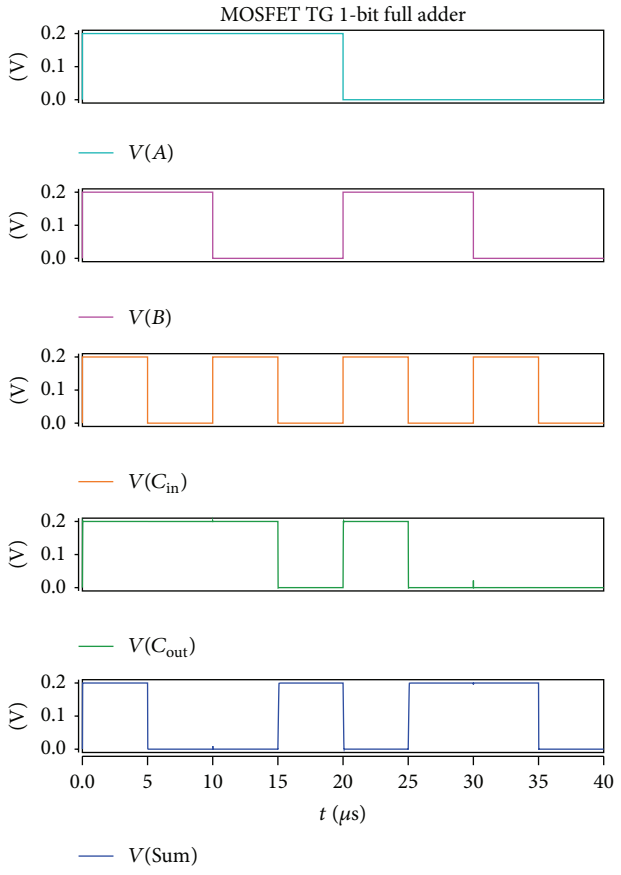

Figure 11: Input and output waveforms of MOSFET-based TG full adder.

large reduction in PDP compared to MOSFET-based full adder. This indicates that the average energy consumed per switching event for FinFET is efficiently better than that of MOSFET because of the low average power dissipation during its operation.

Figure 19 shows the bar graph for EDP of both MOSFET-based and FinFET-based full adder. In Figure 19, the EDP of FinFET-based full adder shows a better performance compared to MOSFET-based full adder. Based on (5), the EPD was measured by taking the square of propagation delay. Since the propagation delay of FinFET-based full adder was the lowest compared to MOSFET-based full adder, this contributed to the lowest EDP, thus giving more advantages to FinFET-based full adder, which had the largest improved performance and energy efficiency. By comparing all four types of full adder cell designs, CPL full adder showed the best PDP and EDP due to its characteristics, namely, high speed of performance and full swing operation. The speed of full adder cell can be improved at the cost of an increased power consumption.

8. Conclusions

All four types of 1-bit full adder cells of MOSFET and FinFET were tested and simulated in HSPICE to analyse its metric performances such as propagation delay, average power dissipation, power-delay-product (PDP), and energy-delay-product (EDP). Based on the findings, the 1-bit FinFET-based full adder was shown to be the lowest and optimal tradeoff in all metric performances compared to the MOSFET-based full adder. This proved that, by using FinFET technology in

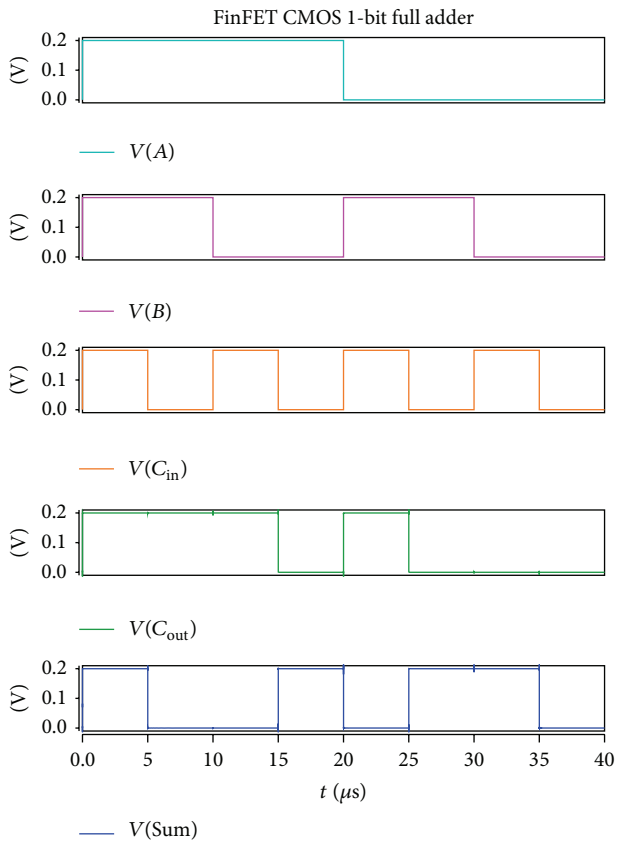

Figure 12: Input and output waveforms of FinFET-based CMOS full adder.

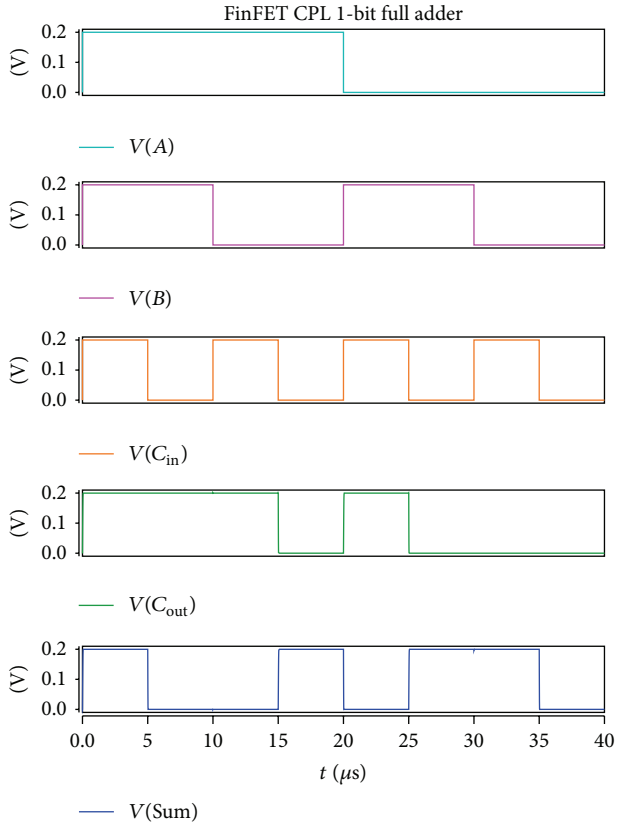

Figure 13: Input and output waveforms of FinFET-based CPL full adder.

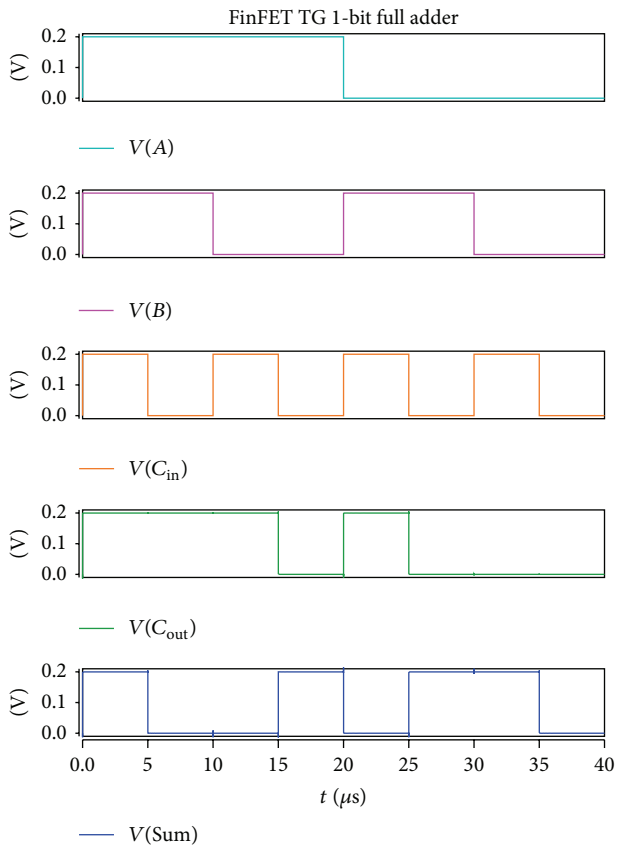

Figure 14: Input and output waveforms of FinFET-based TG full adder.

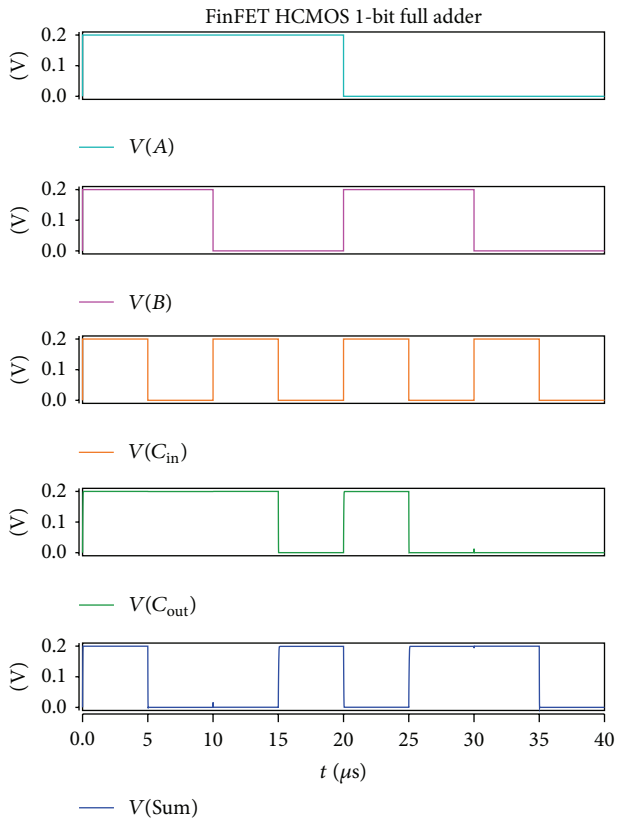

Figure 15: Input and output waveforms of FinFET-based HCMOS full adder.

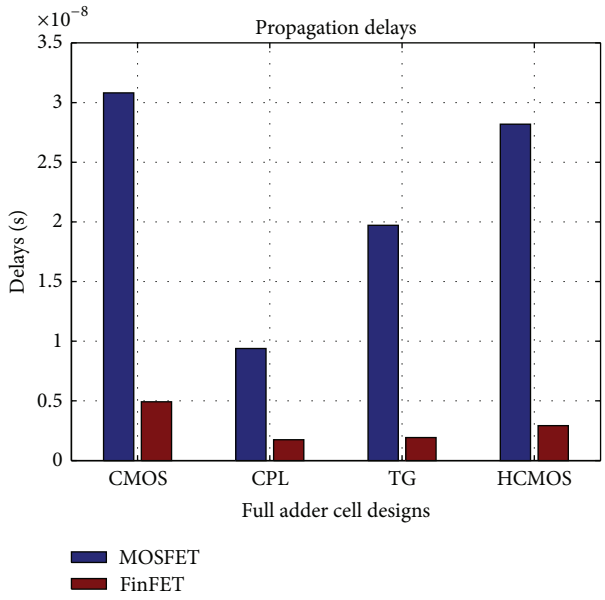

Figure 16: Propagation delays of MOSFET- and FinFET-based full adder.

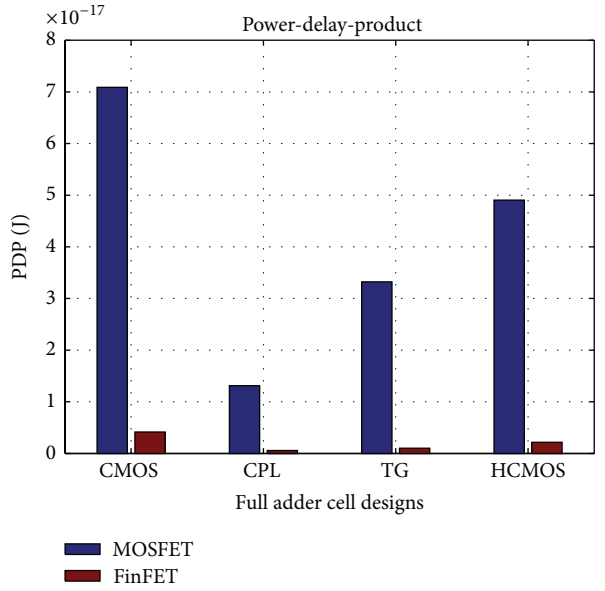

Figure 18: The power-delay-product (PDP) of MOSFET- and FinFET-based full adder.

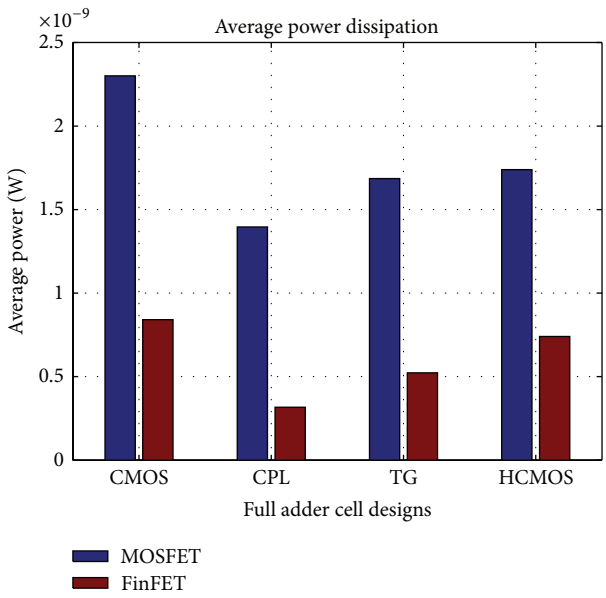

Figure 17: Average power dissipation of MOSFET- and FinFET-based full adder.

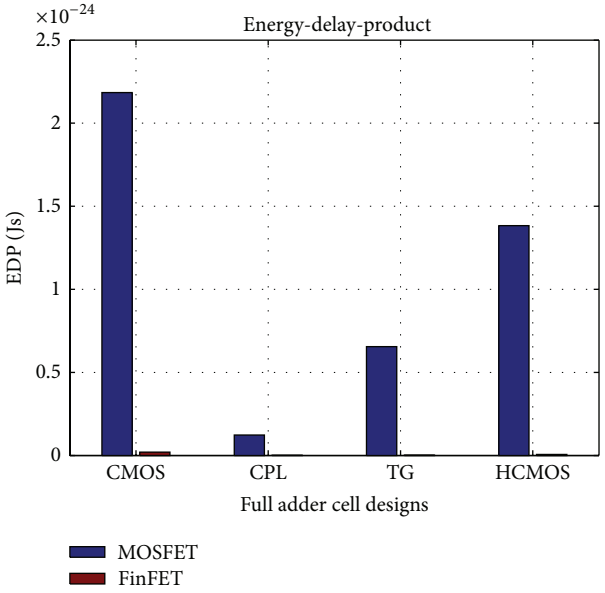

Figure 19: The energy-delay-product (EDP) of MOSFET- and FinFET-based full adder.

1-bit full adder circuitry, it will improve the performance of the device. However, the cell design also contributes to how good the 1-bit full adder performs, as discussed earlier. The 1-bit FinFET-based full adder has a reduced propagation delay and average power dissipation, PDP, and EDP, thus giving FinFET technology great advantages in energy efficiency and performances for 16 nm technology. It was also verified that the 1-bit complementary pass-transistor logic (CPL) FinFET-based full adder performed very well with a reduced amount of PDP and EDP compared to other cell designs because of its high-speed performance and full swing operation.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publicaton of this paper.

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References

[1] W. Lim, H. C. Chin, C. S. Lim, and M. L. P. Tan, "Performance evaluation of 14 nm FinFET-based 6T SRAM cell functionality for DC and transient circuit analysis," *Journal of Nanomaterials*, vol. 2014, Article ID 820763, 8 pages, 2014.

[2] ITRS, International Technology Roadmap for Semiconductor (ITRS)—updated, 2006, http://www.itrs.net/ITRS%201999-2014%20Mtgs,%20Presentations%20&%20Links/2013ITRS/Summary2013.htm.

[3] T. J. K. Liu, "FinFET—history, fundamentals and future," in *Proceedings of the Symposium on VLSI Technology Short Course*, University of California, Berkeley, Calif, USA, June 2012.

[4] X. Huang, W.-C. Lee, C. Kuo et al., "Sub 50-nm FinFET: PMOS," in *Proceedings of the International Electron Devices Meeting (IEDM '99)*, pp. 67–70, IEEE, Washington, DC, USA, December 1999.

[5] D. McGrath, "Globalfoundries looks leapfrog fab rivals with new process," *EE Times*, 2012.

[6] R. Merritt, *TSMC Taps ARM's V8 on Road to 16 nm FinFET*, 2012, http://www.eetimes.com/document.asp?doc_id=1262655.

[7] S. Panda, A. B. B. Maji, and A. Mukhopadhyay, "Power and delay comparison in between different types of full adder circuits," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, vol. 1, pp. 168–172, 2012.

[8] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 1, pp. 20–29, 2002.

[9] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*, Springer, 2007.

[10] T.-J. King, "FinFETs for nanoscale CMOS digital integrated circuits," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD '05)*, pp. 207–210, IEEE, November 2005.

[11] L. Dhulipalla and A. Lourts Deepak, "Design and implementation of 4-bit ALU using FINFETS for nano scale technology," in *Proceedings of the International Conference on Nanoscience, Engineering and Technology (ICONSET '11)*, pp. 190–195, November 2011.

[12] D. A. Neamen, *Semiconductor Physics and Devices*, McGraw Hill, 2003.

[13] P. E. Allen, D. R. Holberg, P. E. Allen, and P. Allen, *CMOS Analog Circuit Design*, Holt, Rinehart and Winston, New York, NY, USA, 1987.

[14] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, vol. 2, Prentice hall, Englewood Cliffs, NJ, USA, 2002.

[15] C. Fonstad, "MOSFETs in the sub-threshold region (i.e. a bit below VT)," in *Microelectronic Devices and Circuits*, C. Fonstad, Ed., vol. 6, pp. 1–17, MIT OpenCourseWare: Massachusetts Institute of Technology, 2009.

[16] F. Moradi, D. T. Wisland, T. V. Cao, A. Peiravi, and H. Mahmoodi, "1-bit sub threshold full adders in 65nm CMOS technology," in *Proceedings of the 20th International Conference on Microelectronics (ICM '08)*, pp. 268–271, December 2008.

[17] A. Islam, M. W. Akram, and M. Hasan, "Variability immune finFET-based full adder design in subthreshold region," in *Proceedings of the International Conference on Devices and Communications (ICDeCom '11)*, pp. 1–5, February 2011.

[18] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1309–1321, 2006.