Title: Two-dimensional (2D) transition metal dichalcogenide semiconductor field-effect transistors: the interface trap density extraction and compact model

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Abstract: A surface potential-based low-field drain current compact model is presented for two-dimensional (2D) transition metal dichalcogenide (TMD) semiconductor field-effect transistors that takes into account the effect of interface trap states on device current-voltage (Ids-Vgs) characteristics and transconductance gm. The presence of interface trap states detrimentally affects device Ids-Vgs performance. Minimal work exists on the extraction of trap states (cm-2 eV-1) of MoS2/high-K dielectric/metal-gate stacks. Additionally, there is a lack of compact models for 2D TMD MOSFETs that can take into account the effect of trap states on device Ids-Vgs performance. This study presents a method to extract the interface trap distribution of MoS2 MOSFETs using a compact model. Presented as part of the model is a surface potential/interface trap charge self-consistent calculation procedure and a drain current expression that does not need numerical integration. The model is tested against reported experimental Ids-Vgs data, and excellent agreement is found between the experiment and the model.