AN ENHANCED SIMULATED ANNEALING APPROACH FOR CYLINDRICAL, RECTANGULAR MESH, AND SEMI-DIAGONAL TORUS NETWORK TOPOLOGIES

NORAZIAH BINTI ADZHAR

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Universiti Teknologi Malaysia

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To my beloved father and mother,

To my family and friends,

To all muslim ummah.

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All praise is to Allah سُبْحَانَهُ وتَعَال, the truth and the only God deserved of All Praises and Submissions. Peace and blessing to the blessed and chosen prophet, Muhammad ﷺ, who is the messenger and the teacher of truth. There is no power except by the power of Allah and I humbly return my acknowledgement that all knowledge belongs to Allah. I thank Allah for granting me this opportunity to broaden my knowledge in this field. Nothing is possible unless He made it possible.

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ABSTRACT

A multiprocessing system has processor-memory modules in a network which is always referred to as net. In many cases, the modules are placed in a regular arrangement such as rectangular grid, bus, star and hypercube. In this research, we proposed one conceptual model and two network topologies for routing the elements of the network. In the first model, a static single-row network was transformed into a dynamic three-dimensional cylindrical model. This new routing model has its axis perpendicular to single-row planes, which gives the advantage of allowing unlimited connections between the pairs of elements based on the program requirements. The single-row routings in each network were produced optimally using the earlier model called Enhanced Simulated Annealing for Single-row Routing (ESSR). In the second part of this research, mesh network topology which consists of an array of square cells was proposed as our routing platform to achieve a complete automatic routing. The problem was further split into two cases; first, a fully gridded network to minimize the number of layers and second, the obstacle avoidance network model. Dijkstra's shortest path algorithm was used to provide the shortest path for each net. The arrangement was further refined using a simulated annealing method. From this technique, the minimum number of layers was produced to complete the routing with lower energy level and to provide the best path if it exists, with the presence of obstacles. The last part of this research is an extension of our previous work, where a more scalable and regular network called semi-diagonal torus (SD-Torus) network was used as a routing platform instead of the mesh network. The performance of SD-Torus network was much better compared to torus and mesh networks in terms of energy level and the number of routed nets. The network topology performed complete routing up to 81 nodes with 80 nets in 9×9 network size. This technique maximizes the number of nets through the minimum energy. The simulations for each network are developed using Microsoft Visual C++ 2010 programming language.

ABSTRAK

Sebuah sistem multipemprosesan terdiri daripada pasangan modul prosesor-memori dalam sebuah rangkaian yang sering dirujuk sebagai jaring. Dalam kebanyakan kes, modul ini disusun dalam susunan yang tetap seperti grid segi empat tepat, *bus*, torus dan hiperkiub. Dalam penyelidikan ini, kami mencadangkan satu model konseptual dan dua topologi rangkaian bagi menghalakan setiap elemen di dalam rangkaian. Dalam model yang pertama, sebuah rangkaian baris tunggal yang bersifat statik telah dijelmakan menjadi sebuah model silinder tiga dimensi yang dinamik. Model laluan yang baharu ini mempunyai paksinya serenjang kepada satah baris tunggal yang mempunyai kelebihan untuk membenarkan jumlah sambungan tanpa had bagi setiap pasangan elemen, bergantung kepada keperluan program. Laluan baris tunggal bagi setiap rangkaian dihasilkan secara optimum melalui program terdahulu yang dipanggil Simulasi Penyepuhlindapan yang dipertingkatkan bagi Laluan Baris Tunggal (ESSR). Dalam bahagian yang kedua bagi kajian ini, rangkaian topologi mesh yang terdiri daripada susunan sel segi empat sama dicadangkan menjadi landasan laluan bagi mencapai laluan automatik yang lengkap. Masalah ini kemudiannya dibahagikan kepada dua kes, kes pertama, model bergrid penuh untuk meminimumkan bilangan lapisan dan kes kedua, model penghindaran halangan. Algoritma laluan terpendek Dijkstra diguna pakai untuk menghasilkan laluan terpendek bagi setiap jaring. Susunan setiap jaring pula ditapis lagi menggunakan kaedah simulasi penyepuhlindapan. Daripada teknik ini, lapisan minimum dapat dihasilkan bagi melengkapkan laluan dengan tahap tenaga yang lebih rendah dan juga memberi laluan terbaik jika wujud walaupun dengan kehadiran halangan. Bahagian terakhir penyelidikan ini merupakan lanjutan kepada kajian terdahulu kami, di mana rangkaian yang lebih mudah diskalakan dan beraturan tetap yang dinamakan Rangkaian Torus Separuh Perpenjuru (SD-Torus), digunakan sebagai landasan laluan menggantikan rangkaian mesh. Prestasi rangkaian SD-Torus adalah lebih baik dibandingkan dengan rangkaian torus dan mesh dari segi tahap tenaga dan bilangan jaring yang dihalakan. Topologi rangkaian ini melaksanakan laluan lengkap sehingga 81 nod dengan 80 jaring di dalam rangkaian bersaiz 9×9. Teknik ini memaksimumkan jumlah sambungan jaring melalui tahap tenaga yang minimum. Simulasi bagi setiap rangkaian dibina menggunakan bahasa pengaturcaraan Microsoft Visual C++ 2010.

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N_x	-	Array of mesh-connected processors in x-axis.
N_y	-	Array of mesh-connected processors in y-axis.
R	-	Successful routed nets.
a_{ij}	-	Matrix representing sequence number and nets.
m	-	Total number of nets.
i	-	Sequence number.
j	-	Nets.
E	-	Energy.
d_{ij}	-	Total number of communication links used to connect source and target node.
N_i	-	Net i.
N_j	-	Net j.
Q	-	Level of congestion.
Q_u	-	Upper street congestion.
Q_l	-	Lower street congestion.
D	-	Interstreet crossing or dogleg.
A	-	Adjacency matrix.
x	-	Eigenvector of A.
λ	-	Eigenvalues of A.
I	-	Identity matrix.
T_s	-	Spanning tree of G_s.
T	-	Temperature.
L_i	-	Netlist.

T_k	-	Temperature.
S_i	-	Source node.
T_i	-	Target node.
$p \times p$	-	Network size.

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CHAPTER 1

INTRODUCTION

1.1 Research Background

A Printed Circuit Board (PCB) is a board made from glass reinforced plastic with copper tracks, which is the backbone of electrical devices. Traditionally, embedded applications in multimedia, wireless communications or networking have been implemented for PCBs. A PCB system is a composition of discrete integrated circuits (ICs) such as General Purpose Processors, Digital Signal Processors and many more [1]. The revolutionary changes in technologies have help humans in developing more sophisticated electronic devices. Nowadays, electronic devices such as computers, laptops, smartphones, tablet computers with touch screen display and virtual keyboards have no doubt become common tools in our daily lives. Not just that, but in the context of solving large-scale scientific problem, the demand for the use of supercomputers has increased. This fastest type of computer can perform at or nearly the highest operational rate for computers. A supercomputer is very efficient in solving scientific problems that involve three interactive disciplines: theories, experiments and computations. It has been used to solve various complex problems in the field of weather forecasting, structural analysis, electronic circuit design, advanced automation, artificial intelligent, as well as socioeconomics. Its computational part is cheaper, faster and produces more accurate results. Therefore, the demand for research and development in integrated circuit and automated design has also increased rapidly.

This advancement in technologies has been made possible thanks to the evolution of integrated circuits. The first transistor was invented by William Shockley, John Bardeen and Walter Brattain at Bell Laboratories on 16th December 1947 [2]. This was the most important invention in electronics event as it was later made possible for the invention of integrated circuit and microprocessor. A single-transistor integrated circuit was then invented by Jack Kilby in 1958 at Texas Instruments [3]. At first, ICs version in 1962 was just a simple device with two to four digital gates per package. Later on, in 1975, the ICs itself had undergone a great advancement. It was produced with 2000 gates and 4000 bits of memory per package. Such remarkable changes have increased the requirement for electronic circuits. Figure 1.1 illustrates the expansion for the demand.

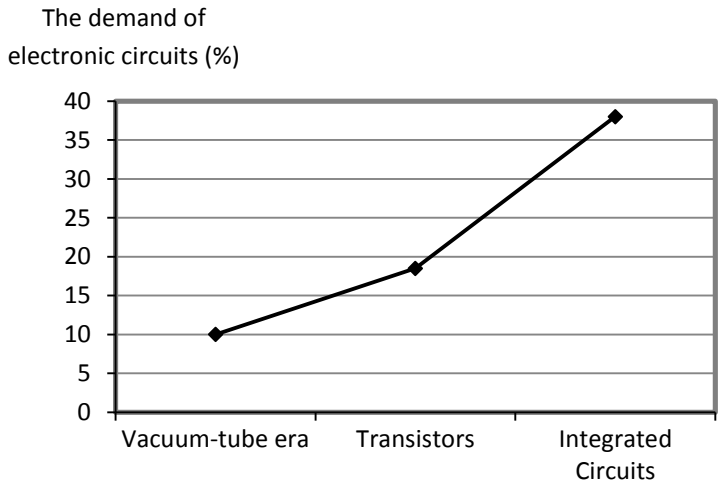

Figure 1.1 The demand for electronic circuits during vacuum-tube era and during the invention of transistor and ICs.

The inventions of transistors and ICs have given birth to microprocessors. Today, a microprocessor represents the most complex application of transistors [4]. The history of microprocessor starts in 1970, when Intel Corporation released their first microprocessor called Intel 4004 [5]. It was the first commercially available microprocessor. The designing of the chip started in April 1970 and was completed in January 1971.

The quest to increase the number of devices per chip had resulted in a rapid transition from Small-Scale Integration (SSI), Medium-Scale Integration (MSI), Large-Scale Integration (LSI) and Very Large-Scale Integration (VLSI) [6]. This advancement is as illustrated in Figure 1.2.

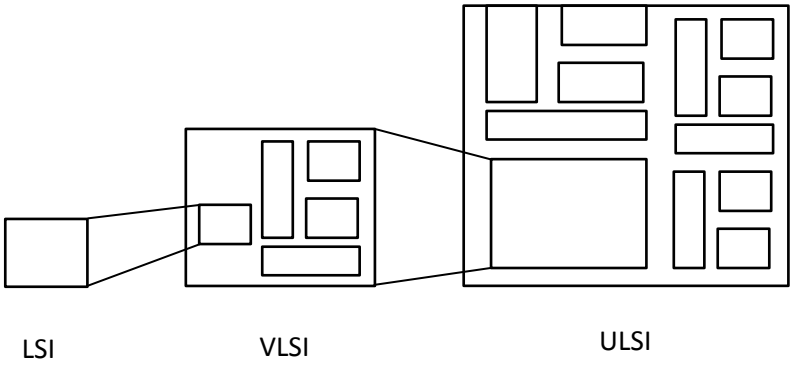

Figure 1.2 The chip scope and the sequence of technologies in circuit integration.

This integration has significantly reduces manufacturing cost and improves the design in several ways:

i. **Compactness**: Physically small.
ii. **Speed**: Higher speed with lower parasitic element (reduced interconnection length)
iii. **Power Consumption**: Lower.
iv. **Reliability**: High reliability which improves on-chip interconnection.

A VLSI chip constitutes 10 to 100 million devices compared to SSI that contains transistors numbering in the tens back then [7-8]. The relationship between numbers of transistors per chip versus years has become Moore's first law. According to this law, the transistor count doubles every 18 months [9]. To reflect further growth of complexity, the term Ultra Large Scale Integration (ULSI) has been used for chip with more than 1 million of transistors [10].

On-chip communication also undergoes several stages of evolution as illustrated in Figure 1.3. A shared bus on-chip communication architecture is an upgraded version of custom bus and is the most common way to send data and

commonly found in many commercial System-on-Chips (SoCs) [11]. However, several drawbacks of shared bus such as longer data transmission lead the researchers to focus on hierarchical buses. This type of buses consists of several shared buses interconnected by a bridge to improve the performance. This new topology offers large throughput improvements compared to shared buses such as decreased load per bus. Bus matrix, or also called crossbar switch as discussed in ([12], [13]), is getting increasingly popular for on-chip communication. It consists of several buses in parallel, which connect every master to every slave. This results in wire congestion and makes it impractical to achieve timing closure of the design [14].

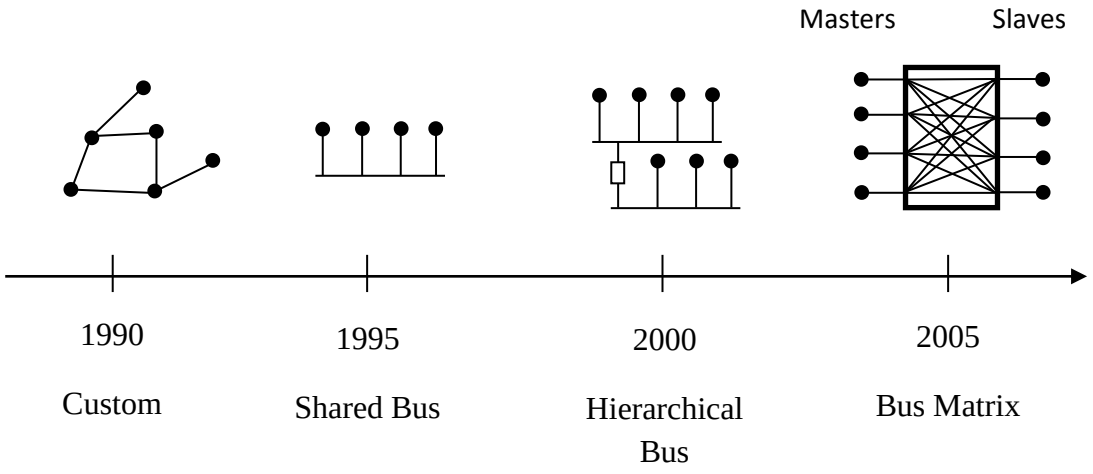

Figure 1.3 Evolution on bus on-chip communications.

Network-on-Chip (NoC) is the latest development in the field of VLSI design [15-16]. It is the communication backbone of virtually all large-scale System-on-Chips (SoC) designs. The main feature of NoC is the use of networking technology to establish connection within the chip instead of using buses. Since an integrated system contains billions of transistors composing tens to hundreds of IP cores, the main challenge in NoC is to design on-chip interconnection networks that efficiently connect the IP cores [17]. NoC architecture as proposed in [18] deploys mesh interconnection topology due to its simplest feature in terms of layout perspective. This topology is as shown in Figure 1.4.

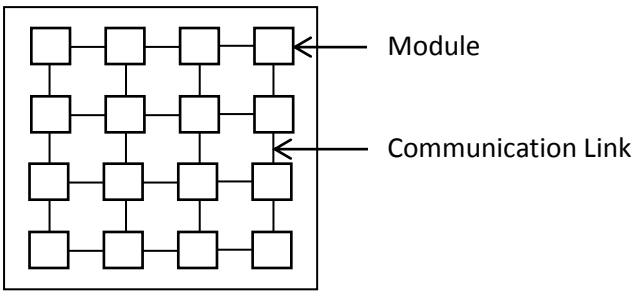

Figure 1.4 A 4×4 mesh NoC topology.

However, since mesh network has large network diameter and small bisection width, a lot of new topologies for NoC architecture have been proposed in the literature. This includes the introduction of additional links, some long links, and providing wrap-around links for each pair boundary module. NoC is becoming a more and more popular solution to accommodate a large number of IP cores in a network [17]. Due to its significance and importance for the technology nowadays, the research and development in this field has become really necessary.

In this research, we are concerned in providing a significant contribution in this field in terms of routing process between each pair of the components place onto a routing board. Routing process will result in a set of geometric path for each pair of components and when etched onto a PCB as routing tracks, electrical connectivity between these components is established. Therefore, an automatic routing technique that improves board routability and reduces number of layers required for complete routing process is needed. Three intelligent routing networks have been developed to perform connections between any two-terminal nets in the routing space, namely three-dimensional single-row routing conceptual model, mesh network to minimize number of layers for complete routing and fully gridded mesh network topology with the placement of obstacles, as well as semi-diagonal torus routing network for general purpose networking applications.

1.2 Motivation

There are several reasons that motivate us to conduct research on this topic. These includes

i. To the best of our knowledge, there is no literature available on the transformation of two-dimensional single-row routing into a dynamic three-dimensional problem and modeled single-row networks in a cylindrical shape.
ii. Most of the routing method for global routing is an extension of Lee's algorithm. Therefore, another method, such as the shortest path-based algorithm is proposed to solve this routing problem.
iii. Simulated annealing is a non-greedy probabilistic method but somehow, it always produces acceptable results and works well with combinatorial optimization problem compared to greedy method.

1.3 Problem Statement

The problem in this study consists of the development of intractable engineering routing problems. Routing in a modern chip is a notoriously difficult problem, and even the simplest routing problem that consists of a set of two-pin nets is known to be NP-complete [19]. After the placement phase, a routing method will determine the precise path in the layout for source node S to interconnect with its target node T. These paths must satisfy the design rules and several constraints added to the respective problem.

The main objective is to achieve 100% connections for each pair of nodes in the layout (henceforth regard as net), so that the chip will function correctly. As the advancement in technologies growth, the complexity of the routing process also increases since a single chip may contain billions of transistors, and this number will still grow in the near future [19]. This increasing complexity has made the research

on VLSI routing received much attention in the literature. Basically, the inputs for a routing problem are as follows:

i. A placed layout with fixed locations of nodes.
ii. A netlist which is a set of nets routing requirement.
iii. A set of design rules for manufacturing process.
iv. A timing budget for each critical net.

From these inputs, at the end of the routing process, we are expected to generate the connections for each net that meets the design rules and optimize the respective objective function.

1.4 Research Problems

Several problems that have been studied in this research include:

i. How to transform the two-dimensional single-row routing problem into a three-dimensional dynamic model?
ii. Given a network topology, how to route given a set of two-pin nets in such a way that the paths do not overlap?
iii. For a general mesh network topology, how to route the nets when the routing platform is utilized with the placement of obstacles?
iv. What is the extension to the original mesh topology to make it suitable for Network-on-Chip interconnection network?
v. How is the performance of semi-diagonal torus network when using our proposed routing algorithm?

1.5 Research Objectives

The objectives of this research are:

i. to model an ordinary single-row routing problem into a dynamic cylindrical model.
ii. to develop a routing method that uses shortest path-based algorithm and simulated annealing technique.
iii. to utilize grid routing graph with the placement of obstacles.
iv. to compare the performance of mesh and torus network with a more scalable and regular network, which is a semi-diagonal torus network (SD-Torus).
v. to compare the propose routing technique with greedy method.

1.6 Scope of the Study

This research is bounded by the followings:

i. The proposed solution space is three-dimensional in terms of design.
ii. The proposed solution is based on approximated methods.
iii. The parameters that are investigated in this study are initial temperature, temperature reduction rules, temperature setting schemes and stopping criteria.

1.7 Significance of Findings

This study has contributed some new ideas in the field of optimization problem in VLSI design. Through this study, three models have been proposed to perform routing in various branches of VLSI designs, namely single-row routing, global routing and interconnection networks. The first model is a conceptual model

called SA-CM (Simulated Annealing for Cylindrical Model), which is the transformation of an ordinary single-row routing problem into a dynamic cylindrical model, which no one has done this before. For routing problem in mesh, a network topology called SA-RM (Simulated Annealing for Rectangular Mesh) is proposed. Through this topology, two cases have been considered. The first case is a layer minimization network without placement of obstacles and the second one is a full gridded routing model utilized with blocks of obstacles. A significant routing method has been developed for both cases. From the result, it can be observed that there is a specific scheme of net ordering to encounter these two cases. The performance comparison of mesh and torus networks with a more scalable and regular network, which is a semi-diagonal torus network (SD-Torus), has also been studied and SA-SDT (Simulated Annealing for Semi-Diagonal Torus) routing network is proposed in this routing problem. Last but not least, the contribution is in terms of copyrights from papers and possible innovation and development of a tangible product from the work. Most of our research papers have been published in indexed local/international journals. Research papers have also been presented in international conferences (see Appendix).

1.8 Research Workflow

Our research work begins with the transformation of a two-dimensional single-row routing (SRR) into a three-dimensional conceptual model. Firstly, possible shapes to model this transformation have been studied. Then, a cylindrical design has been chosen due to its symmetrical properties along with an infinite number of planes due to the fact that its cross-sectional area is that of a circle. This differs with other shapes that have limited lines of symmetry such as hexagon, octagon and others. This property is very important in order to allow the configuration of the nets to change according to pin connection requirements, thus making it a dynamic model. Several properties of this cylindrical model also are studied.

Then, the maximum possible net ordering for general n number of nodes and produced an inductive relationship has been determined. An optimal result for a single-layer network has been achieved through Enhanced Simulated Annealing technique presented in [20]. Therefore, we are motivated to broad the SRR concept by proposing this transformation. The method in [20] has been studied and implemented to produce optimal configurations for each SRR network producing SA-CM model.

In the second part of our research work, another type of routing technique in the chip design has been studied, which is global routing. In this problem, our routing platform is assumed to be divided uniformly into $N_x \times N_y$ and the resulted routing graph is considered as an array of mesh-connected processors. This network is called as SA-RM and is further split into two cases. In the first case, we consider SA-RM network topology to minimize the number of layers to achieve a complete routing. For the second case, the network is further utilized with the placement of obstacles. The problem is mainly about performing connections for each pair of nodes in the graph, and the path taken must follow the communication links. This will allow for a simpler representation even though it reduces freedom during routing. The main objective of this problem is to seek the maximum number of connections while minimizing the level of congestion throughout the region. Then, the objective function for this problem has been developed.

In this study, it is important to have all pins connected in the shortest way to reduce the energy level in the routing region. Therefore, several possible methods have been studied for this purpose. Most of the routing algorithm reported in the literature is an extension to Lee's algorithm [21]. Even though it guarantees to find the minimum cost possible path if it exists, its searching nature based on wave propagation is slow. Therefore, we are motivated to use Dijkstra's algorithm, which is based on a Breadth-first Search method. Then, to further refine the sequences, simulated annealing method, a metaheuristic method, is applied.

When solving the routing problem in mesh network, several drawbacks of this topology have been noticed. It is a powerful candidate for general-purpose routing due to its simplicity and easy to implement. However, when designing a network topology for Network-on-Chip (NoC), it is the worst in this class. Its limited number of communication links degrades the performance as the network size increases. Several outstanding topologies in the literature have been studied and it has been noticed that regular and symmetrical interconnection networks lead to a better implementation in terms of their routing algorithm and routers as well [22-23]. Therefore, a routing network called SA-SDT which is based on a semi-diagonal torus network, a symmetric and more scalable network as proposed in [24] is discussed. It is a mixture of mesh and torus networks in topology. With the same objective function as in mesh routing problem, the proposed routing algorithm has been re-applied and the results have been compared with mesh and torus networks. All of the research work is summarized in Figure 1.5.

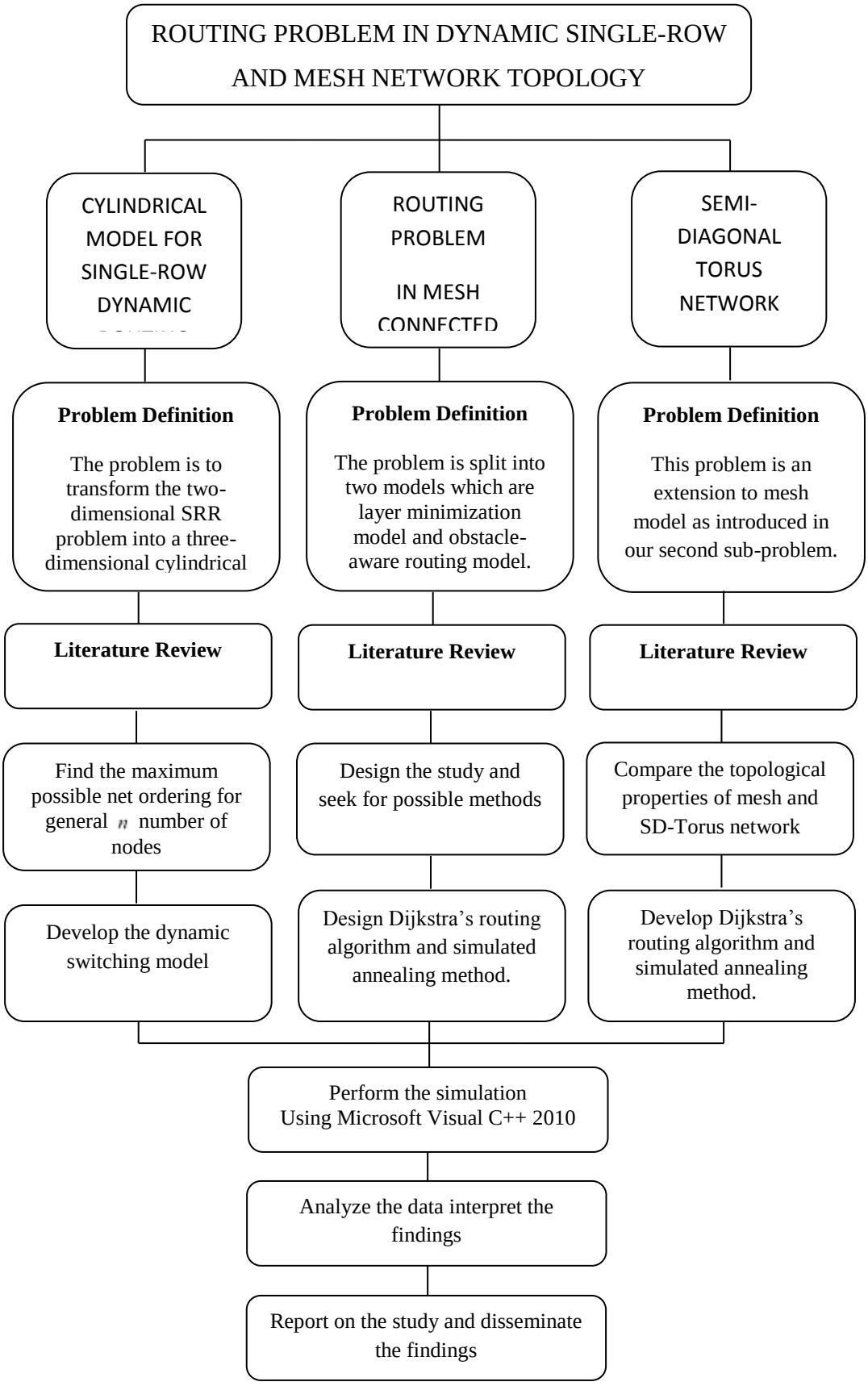

Figure 1.5 Research workflow.

1.9 Thesis Outline

This thesis is divided into six chapters, which include the introduction, literature review, a three-dimensional cylindrical model for a single-row dynamic routing, sequential global routing problem in VLSI, a semi-diagonal torus network for general purpose networking applications, as well as concluding remarks and further works.

In the first chapter, the introduction to the whole thesis is given, including the research background, problem statement, research objectives, scope of the study, significance of the findings and research workflow.

Chapter 2 presents the literature review of this research. In this chapter, an overview of the single-row routing technique, global routing problems, as well as its routing method and network topologies are described. Various works by different researchers regarding this topic is presented and an overview of our proposed method is also discussed.

Chapter 3 focuses on the SA-CM conceptual model, a transformation of a single-row routing technique, which has its main application in the printed circuit board design where the nets between the pins are drawn statically, that is, in a fixed manner. A new dynamic single-row routing model for the switching of pins based on the cylindrical design also is discussed. The single-row routings in each network are produced optimally using the earlier model called ESSR (Enhanced Simulated Annealing for Single-row Routing).

Next, in Chapter 4, another type of routing technique for the process of automatic design in printed circuit boards (PCBs) is discussed, which is called global routing. In this chapter, a routing method is proposed based on Dijkstra's shortest path algorithm and simulated annealing technique onto a mesh network model called SA-RM. This problem is further split into two cases. In the first case, a fully gridded model is considered to minimize the number of layers, whereas in the second

case, the earlier network topology is utilized with the location for all blocks with pins on the boundaries representing obstacles.

In Chapter 5, a semi-diagonal torus (SD-Torus) network is discussed and SA-SDT model is proposed. This network is both symmetrical and regular, which made it very advantageous in the implementation process. Its small network diameter also leads to lower network latency. The comparison part is divided into two. First, the performance of SD-Torus is being compared with mesh and torus networks. Secondly, the performance of our proposed algorithm on SD-Torus is compared with greedy method.

Finally, the last chapter presents the concluding remarks and further works of this research. Some recommendations for future research on the routing method, network topologies and few restrictions on the network are also suggested in this chapter.

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