SPEED ENHANCEMENT ON A MATRIX INVERSION HARDWARE ARCHITECTURE BASED ON GAUSS-JORDAN ELIMINATION

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Specially dedicated to my beloved family, lecturers and friends
For the guidance, encouragement and inspiration
Throughout my journey of education

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ABSTRACT

Matrix inversion is a mathematical algorithm that is widely used and applied in many real time engineering applications. It is one of the most computational intensive and time consuming operations especially when it is performed in software. Gauss-Jordan Elimination is one of the many matrix inversion algorithms which has the advantage of using simpler mathematical operations to get the result. This work presents the architecture of a matrix inversion hardware using Gauss-Jordan Elimination algorithm with single precision floating point representation. The proposed design is an enhancement of a previous work which implemented Gauss-Jordan Elimination to perform matrix inversion for complex matrix suitable for MIMO applications. The proposed design was bench-marked with other implementations such as hardware architecture of similar matrix inversion algorithm, hardware architecture of other matrix inversion algorithms and software implementation such as C++. The execution timing performance of the proposed design is improved in comparison with the previous architecture design by a factor of 0.14 for a matrix size of 36x36. Overall, the proposed design is capable of preforming matrix inversion for a matrix of size 36x36 in 1.9 milliseconds and consumes hardware resources of about 18128 logic elements.

ABSTRAK

Penyongsangan matrik merupakan algoritma matematik yang lazim digunakan dalam pelbagai aplikasi kejuruteraan. Ia merupakan salah satu operasi yang memerlukan pengiraan intensif dan memakan masa terutamanya apabila dilaksanakan dalam perisian. *Gauss-Jordan Elimination* merupakan salah satu daripada pelbagai algoritma matrik penyongsangan yang menggunakan matematik operasi yang lebih ringkas untuk mendapatkan hasil keputusan. Projek ini membentangkan seni bina perkakasan matrix penyongsangan dengan menggunakan *Gauss-Jordan Elimination* algoritma bersama dengan format ketepatan tunggal titik terapung. Perkakasan reka bentuk yang dicadangkan merupakan peningkatan kepada reka bentuk yang terlebih dahulu, di mana dengan tujuan untuk melaksanakan penyongsangan matrik untuk penyesuaian kepada aplikasi *MIMO* dengan menggunakan algoritma *Gauss-Jordan Elimination*. Perbandingan juga dibuat dengan reka bentuk perkakasan lain yang menggunakan algoritma matrik penyongsangan yang sama, reka bentuk perkakasan yang menggunakan algoritma matrik penyongsangan yang lain, serta pelaksanaan perisian seperti C++. Perkakasan reka bentuk yang dicadangkan mencatatkan masa yang lebih laju berbanding dengan reka bentuk yang terlebih dahulu dengan factor 0.14 bagi matrik saiz 36x36. Keseluruhannya, reka bentuk yang dicadangkan mampu untuk melaksanakan penyongsangan matrik bagi matrik saiz 36x36 dalam masa 1.9 milisaat dan mengambil sumber perkakasan sebanyak 18128 unsur-unsur logic perkakasan.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

QRD	-	QR decomposition
LUD	-	LU Decomposition
SVD	-	Singular Value Decomposition
GE	-	Gaussian Elimination
FSM	-	Finite State Machine
DU	-	Data-path Unit
CU	-	Control Unit
mif	-	memory initialization file
MIMO	-	Multiple Input Multiple Output
LTE	-	Long-Term Evolution

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Project Background

Matrix inversion is a widely used mechanism in many real time engineering applications. In telecommunication system, matrix inversion is used in MIMO-ODFM [5] (multiple input multiple output orthogonal frequency division multiplexing) and Long-Term Evolution (LTE) MIMO receivers to remove the effect of the channel on the received signal. In cryptography, matrix inversion is the key operations in decryption process. Matrix inversion is also applied in image processing for image reconstruction using neural networks. In VLSI circuit simulation, it is used to solve large systems of equations where matrix representation is used for the internal variables of a subcircuit, and the interconnect among subcircuits. In robotic applications, matrix inversion is used for computing velocities of the robot joints by inverting the Jacobian matrix.

There are numerous matrix inversion algorithms such as Newton's method, Cayley-Hamilton method, Eigendecomposition, QR decomposition, Cholesky decomposition, Blockwise inversion, other than Gauss Elimination and its extended version namely Gauss-Jordan Elimination method.

Gauss-Jordan Elimination requires simple arithmetic operations i.e. Addition/Subtraction, Multiplication, and Division. In contrast, other numerical matrix inversion methods require more complicated operations, such as square root operation as in QR decomposition by Gram-Schmidt Orthogonalization, and sine and cosine operations as in QR decomposition by Rotation [10]. Gauss-Jordan Elimination is characterized as a simple, efficient, direct, parallelizable, and universal algorithm to find the inverse of any kind of square matrices [9].

1.2 Problem Statement

Matrix inversion is one of the most costly and compute-intensive operations to be performed in software. It involves a series of mathematic operations in order to obtain the inversion of one matrix. As the matrix size increases, the number of operations needed will increase significantly. In the current hardware implementation, achieving high execution speed while maintaining the complexity and resource utilization is a huge challenge for hardware designer.

1.3 Objective

The objective of this project is to implement the hardware accelerator on a scalable and low area cost hardware architecture that performs matrix inversion using the Gauss-Jordan Elimination method. The performance of the proposed design is analyzed in terms of its execution speed, resource utilization, maximum frequency, and compared to the previous hardware design architecture [7].

1.4 Scope

The proposed system is implemented using hardware description languages, such as Verilog and SystemVerilog.

The following software are used in this project:

- Quartus II Version 13.1.0 Web Edition is used for modelling the system in Verilog and SystemVerilog.
- ModelSIM Altera is used for simulating the design and for acquiring performance statistics.
- C++ program is used for benchmarking and for results verification.

Single precision floating point (IEEE 745 standard) format is used to compute the matrix. Matrix size from 3x3 up to 36x36 is evaluated.

1.5 Thesis Structure

This thesis consists of five chapters. Chapter one has described the background, problem statement, objectives, and scope of the project. Chapter two describes the theory and background of Gauss-Jordan Elimination method as well as previous works that have been done in this field. Chapter three explains the research methodology used in this thesis including the system architecture. Chapter four shows the hardware results with analysis and discussion, followed by comparison with previous hardware design in terms of execution speed, maximum frequency, clock counts and resource utilization. Chapter five states the conclusion and the possible future works that can be implemented to improve the performance of the hardware architecture. References and appendixes are attached at the end of the thesis.

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