FAULT MODELING OF CHIRALITY VARIATION FOR CARBON NANOTUBE FIELD EFFECT TRANSISTOR AND ITS EFFECT ON CIRCUITS PERFORMANCE

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ABSTRACT

Carbon Nanotube (CNT) is one of the promising materials to be discovered that can replace silicon as the material for nano scale electrical switch. CNTFET have been shown to have better performance, able to operate on shorter channel length and drive a lower power envelop as it MOSFET counterpart. The conductivity of CNT is determined by the chirality of the tube, which determines the diameter of the CNT. However, the chirality cannot be fully controlled directly during manufacturing of the material. Much efforts have been concentrated to have tight manufacturing control to have constant chirality. The effect of chirality variation is in the diameter of the CNT tube which is responsible for the current carrying capacity of the CNT. Non-uniform chirality will cause degradation in performance of logic circuits. The variation in chirality can be viewed as faults. For that reason, there is a crucial need to model defects introduced during manufacturing process. Current defect models are purely based on simple resistors to mimic stuck at 0 and stuck at 1 which does not answer the basic question which is: "what is the optimum process control should be that so that even with variations in chirality, the circuit could still function? ". The objective of this project is first, to model the defect of CNT based on current manufacturing issues, so that designers and manufacturer could simply predict the behavior of logic circuit. Second, is to analyze logic circuit function with variations in chirality. Based on this result, a simple model is produced. The research methodology adopted in this project is analyzing the effect of changes in chirality and model it as a simple resistor in series with the fault free circuit. The work is based on simulation using HSPICE and the CNT is from Stanford CNT model. The result indicates that circuits could still function despite some changes in chirality which means manufacture still has some acceptable margin of errors.

ABSTRAK

Karbon Tube Nano (CNT) adalah salah satu bahan baharu yang ditemui yang diharapkan boleh menggantikan silikon sebagai suis elektrikal nano. CNTFET telah menunjukkan prestasi yang lebih baik, kebolehan berfungsi pada saluran (channel) yang lebih pendek, dan memacu pada sampulan kuasa yang lebih rendah daripada teknolgi MOSFET sekarang. Kekonduksian CNT adalah ditentukan oleh 'chirality'nya, 'chirality' itu kemudian menentukan diameter CNT. Berbagai usaha ditumpukan dengan kawalan penghasilan yang ketat supaya menghasilkan chiral yang seragam. Ketidak seragaman chiraliti akan menyebabkan penurunan prestasi litar logic. Variasi chiraliti boleh dilihat sebagai kecacatan. Oleh kerana itu, memodelkan kecacatan daripada proses peghasilan adalah penting. Model kecacatan yang biasa diguna hanyalah berdasarkan penyelesaian ringkas sebuah perintang yang hanya mengambarkan 'stuck at 0' atau 'stuck at 1'. Model ini tidak menjawab persoalan "Apakah kawalan proses yang optimum supaya walaupun dengan variasi chiraliti, litar masih boleh berfungsi? ". Objektif project ini adalah pertama, untuk memodelkan isu penghasilan CNTFET, supaya pereka dan pembuat dapat meramalkan keberkesanan litar yang telah direka. Kedua, adalah untuk menganalisa fungsi litar logic yang telah terdedah dengan variasi 'chirality'. Berdasar hasil analisa projek ini, satu kecacatan telah dihasilkan. Kaedah penyelidikan yang digunakan adalah dengan menganalisa kesan-kesan perbezaan chiraliti dan memodelkan suatu perintang yang memberi makluman yang lebih luas tentang keberkesanan litar logic berbanding dengan litar yang tiada kerosakan. Hasil projek ini adalah berdasarkan simulasi yang dijalan meggunakan HSPICE dan meggunakan model CNTFET daripada Stanford. Hasil simulasi telah menunjukkan walaupun terdapat variasi 'chirality' didalam litar, ia masih boleh berfungsi. Ini bermakna, terdapat julat ralat yang masih boleh diterima didalam proses pembuatan.

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CHAPTER 1

INTRODUCTION

1.1 Overview

This chapter describes some of the background information pertaining to this project. Also described in this is the objective and scope covered in this project.

1.2 Background

Carbon Nanotube Field Effect Transistor (CNTFET or CNFET) is one of the most promising components to replace MOSFET transistor. Figure 1.1 shows the summary of how carbon nanotube is explained by its basics structure from graphene taken from [1]. Research has shown that carbon nanotube can be used as the semiconducting channel between source and gate. This novel material is predicted could overcome the serious scaling limits related to fabrication technology and device performances faced by current MOSFET technology.

This limits include quantum mechanical tunneling of carriers through the thin gate oxides, quantum mechanical tunneling of carriers from source to drain and from drain to body, control of the density and location of dopant atoms in the MOSFET

channel and source drain region to provide high on off current ratio, the finite sub-threshold slope. [2]

The theory of CNT transistors is still in its infancy and the technology is still emerging [3]. Computerized calculation of such high-performance transistors in digital circuits is absolutely essential to drive the device design and address the limitation in multi-gigahertz processor design [4]. However, from a circuit designer's point of view, fast and simplified model is essential for circuit simulation and evaluation.

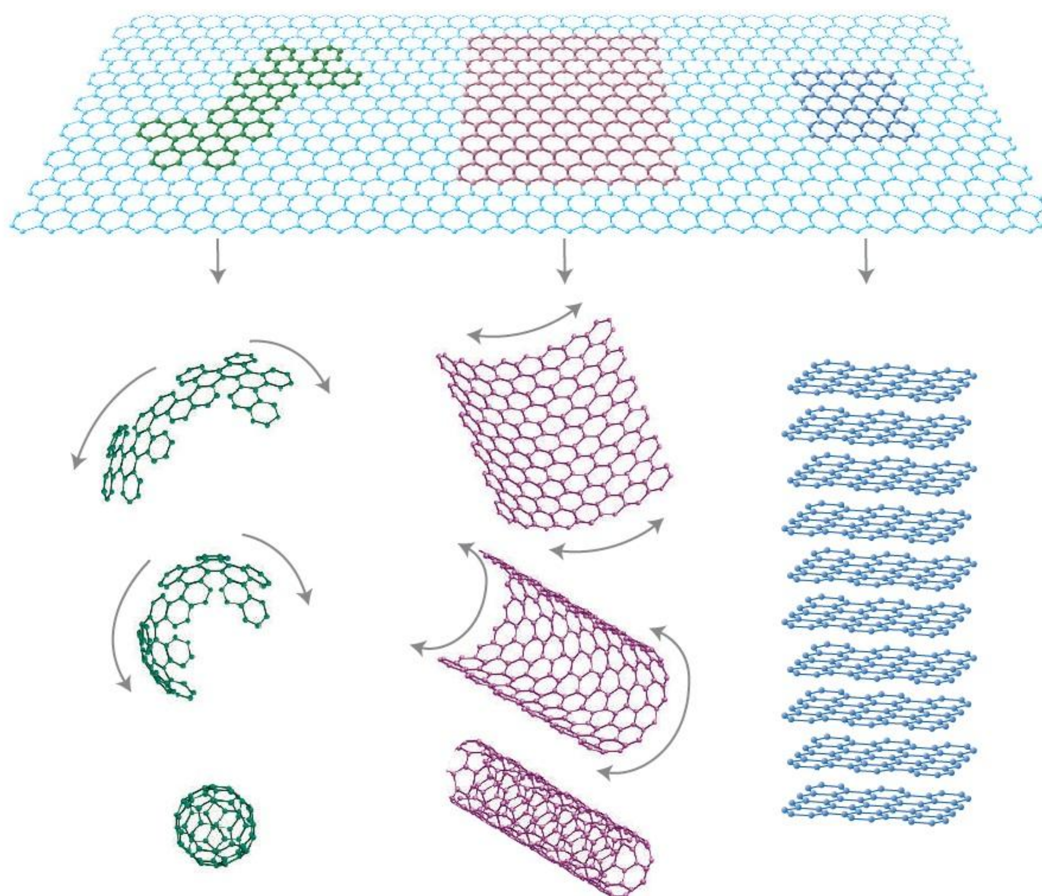

Figure 1.1. Graphene (top) is 2D building material for other carbon materials. It can be wrapped up into 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite [1].

1.3 The Need for Fault Modelling

Although CNTFET model have been established by wide variety of research group [3, 4, 5, 6]. Currently there is very little research on CNTFET fault model.

While CNFET circuits are expected to offer an order of magnitude benefit in energy-delay-product (EDP) over silicon CMOS circuits, in reality, CNTFET is very difficult to fabricate. CNTFET is very prone to failure due physical limitation of current process technology. Significant imperfections inherent to CNTs pose substantial hurdles to realizing practical CNFET circuits.

It is nearly impossible to precisely align and position all CNTs at VLSI scale. This limitation can cause stray conducting paths that result in incorrect logic functionality. Moreover, the CNT density distribution cannot be accurately controlled. CNT density variations can result in CNFET circuit performance variations and functional failures [7].

Metallic CNTs (m-CNTs) have zero or near-zero bandgap, and therefore cause source-to-drain shorts in CNFETs. CNFETs that contain m-CNTs result in excessive circuit leakage power or even incorrect circuit functionality. [7]

There is a continuous research effort to address fabrication issues in CNFET technology. Various techniques have been proposed to model and simulate CNFETs, and to evaluate their potential performance at the device-level in the presence of metallic tubes. Not much study, however, has been performed to analyze CNFET-based real logic circuits when faults are present.

Fault occurrences in new nanotechnologies are predicted to be significantly more as compare to conventional technology due to their size and speed characterizations [8, 9]. It is natural to expect that the future process technology will no longer be perfect at least when it is infancy stage. Ongoing research is being done to enable the design of robust systems that are resilient to hardware imperfections

However in order to achieve device robustness, failure analysis engineers require reliable fault models in order to analyze its effect on circuit performance. This is the aim of this project.

1.4 Problem Statement

CNTFET development is still bogged down by fabrication challenges. Even with the most advance manufacturing technology, CNFET fabrication is still produces high failure rate of the device. The most important challenge in the CNT growth process are the diameter control system and the presence metallic CNTs [10].

Metallic CNTs (m-CNTs) is not desirable as it resulted in high conductivity making its current can no longer be controlled by the gate, causing source-drain shorts in the transistor. At the same time, variations in diameter changes the electrical properties of CNFET altering the tolerance to temperature, currents leakage, drive current and the threshold voltage [10]. Current synthesis process produces 1/3 of m-CNTs and 2/3 of semiconducting CNTs (semi-CNTs) in random manner. The most advance CNTs growth techniques currently can produce up to 90% of semi-CNTs and even maximum of 96% [10] there is still no process that can grow to 100% semi-CNTs. This issue give rise to the need for different m-CNTs removal techniques post-growth processing, namely electrical burning and selective chemical etching.

Currently there is no process that grows nanotubes of only a specific diameter. Depending on the manufacturing method of the CNTs, diameter varies randomly, with every process yielded different mean diameters and diameter distributions [10].

An ”ideal” CNFET (Doped-S/D CNFET) which imitate the MOSFET devices is consist of one or more carbon nanotubes that aligned perfectly in which the section below the gate is intrinsic and the source/drain diameter extension regions are n/p doped. As is always the case, there are some challenges in CNFET manufacturing process.

These challenges have not been address in current fault model for CNTFET. There is a need in CNFET fault modeling so that it can be incorporated to extend the current CNFET design methodology in order to produce a more robust circuit for failure analysis purposes.

In addition, current defect models are purely based on simple resistors to mimic stuck at 0 and stuck at 1 which does not provide the optimum process control information on functionality with variations in chirality.

Fabricated circuits could only function if the manufacturing process produces products according to the design plan. However as discussed previously, the

manufacturing of CNT is plague with issue of uncontrollable chirality among all other issue.

Circuit designers always use a constant chirality for all designs. Constant chirality may not actually occur in practical fabrication. The cost to have a tightly controlled chirality could be too high and it may not necessary to have only one chirality. Minor changes in chirality might still produce acceptable circuit performance.

Totally malfunction circuit such as stuck 0 and stuck 1 could be due to too large change in chirality and this could be easily controlled in fabrication.

Research on slight changes in circuit performance due to small changes in chirality which leads to respective defect model has not been conducted.

Thus there is a need to translate changes in chirality issue to respective fault model.

1.5 Objective

This project focuses on fault model of CNFET due to small changes of chirality.

The objectives are to:

1. Analyze circuit performance with mixture of chirality.

2. Identify how much deviation of chirality will cause certain failure or degradation in performance of logic circuit.
3. Translate the degradations of circuit performance from part 1) and 2) above to a fault model.

1.6 Scope

This project uses Stanford University CNFET Model. All simulations have been carried out using HSPICE.

This project also only cover on digital logic circuit application with preliminary result dealing with basic inverter circuit and to other logic gate circuit.

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