ADAPTIVE ONLINE FAULT DETECTION ON NETWORK-ON-CHIP BASED ON PACKET LOGGING MECHANISM

LOO LING KIM

UNIVERSITI TEKNOLOGI MALAYSIA

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Dedicated to my beloved parents, family, supervisor, seniors, labmates and friends

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Life is a ceaseless learning process. We have to identify the things that we want to achieve at the moment. There is no right or wrong. It is about choices and determination to pass through endurance. The process of getting through endurance may be hard, but surely leave a meaningful memory throughout life.

ABSTRACT

The shrinking size of transistors and on-chip interconnects contribute to increasing probability of on-chip faults. Fault tolerance is one of the key features in Network-on-Chip (NoC) architecture. Current NoCs use Error Detection and Correction (EDC) and acknowledgement mechanisms for fault and error controls. In order to maintain system functionality in presence of the faults, adapting error detection and correction based on changing error probability is required. Adapting fault detection techniques based on error probability helps NoC to achieve improved fault tolerance. End-to-end (E2E) EDC works better at low error probability whereas switch-to-switch (S2S) works better at high error probability condition. This thesis proposes an adaptive fault detection and fault diagnosis based on Negative acknowledgement (NACK) logging mechanism. In the first part, this thesis proposes a PL-Adaptive method where NoC routers are able to switch between E2E and S2S EDC depending on changing error probability. Each router tracks transmitted packets and NACK packets to continuously monitor its fault level. In the second part, this thesis proposes fault type classification of router and link faults. Based on experimental results by using constant uniform traffic pattern, our proposed PL-Adaptive method gives better average latency than using only E2E or S2S. By evaluating the transmission latency with single error in a single path, our proposed PL-Adaptive method is able to achieve latency reduction in the range of $[13\% - 50\%]$ compared to only S2S or E2E mechanism. Moreover, based on smaller decay rate and error probability in the range of $[5 \times 10^{-5} - 10^{-1}]$, smaller threshold increases the higher probability to detect fault and error. PL-Adaptive method is able to detect faults and error up to 96%. Besides, our proposed PL-Adaptive method allows NoC routers to adapt with dynamic packet error probability and can identify router and link faults.

ABSTRAK

Pengecutan saiz transistor serta sambungan atas-cip menyumbangkan kebarangkalian tinggi terhadap kesesaran atas-cip. Toleransi sesar merupakan salah satu ciri utama dalam seni bina Rangkaian-atas-Cip (NoC). NoC terkini menggunakan Pengesan dan Pembetulan Ralat (EDC) serta mekanisme pengakuan untuk pengawalan kesesaran dan ralat. Dalam usaha mengekalkan fungsi sistem dengan kewujudan kesesaran, penyesuaian pengesanan dan pembetulan ralat berdasarkan perubahan kebarangkalian ralat diperlukan. Penyesuaian teknik pengesanan kesesaran berdasarkan kebarangkalian ralat membantu NoC mencapai toleransi kesesaran yang lebih baik. EDC hujung-ke-hujung (E2E) berfungsi lebih baik pada kebarangkalian ralat yang rendah manakala suis-ke-suis (S2S) pula berfungsi lebih baik pada kebarangkalian ralat yang tinggi. Tesis ini mencadangkan satu pengesanan kesesaran mudah suai dan diagnosis kesesaran berdasarkan mekanisme pengelogan pengakuan negatif (NACK). Dalam bahagian pertama, tesis ini mencadangkan *PL-Adaptive* di mana penghala NoC berupaya untuk bertukar di antara E2E atau S2S EDC bergantung kepada perubahan kebarangkalian ralat. Setiap penghala menjejaki paket yang dihantar dan paket NACK untuk memantau tahap kesesaran penghala sendiri secara berterusan. Berdasarkan keputusan eksperimen, kaedah yang dicadangkan memberi purata kependaman yang lebih baik daripada menggunakan hanya E2E atau S2S. Menilai kependaman penghantaran untuk satu ralat dalam penghantaran tunggal, kaedah *PL-Adaptive* yang dicadangkan mampu mencapai pengurangan kependaman dalam lingkungan $[13\% - 50\%]$ berbanding dengan hanya menggunakan kaedah E2E atau S2S. Di samping itu, berdasarkan kadar pereputan yang lebih kecil dan kebarangkalian ralat dalam lingkungan $[5 \times 10^{-5} - 10^{-1}]$, nilai ambang yang kecil menambah kebarangkalian yang tinggi untuk mengesan kesesaran dan ralat. Kaedah *PL-Adaptive* mampu mengesan ralat sehingga 96%. Selain itu, kaedah *PL-Adaptive* membolehkan penghala NoC menyesuaikan diri dengan kebarangkalian ralat paket yang dinamik dan boleh mengenal pasti ralat pada penghala dan penghubung.

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LIST OF ABBREVIATIONS

ACK	–	Acknowledgement
ARQ	–	Automatic-Repeat-Request
BIST	–	Built In Self Test
CBR	–	Constant Bit Rate
CDD	–	Code-Disjoint Detection
CRC	–	Cyclic Redundancy Check
CPD	–	Critical Path Delay
DOR	–	Dimension Order Routing
DSP	–	Digital Signal Processing
EC+ED	–	Single-Erro-Correcting, Multiple-Error-Detecting
ECC	–	Error Control Codings
EDC	–	Error Detection and Correction
epr	–	Equal Priority Recovery
E2E	–	End-to-End
FEC	–	Eorward Error Correction
FPGA	–	Field-Programmable Gate Array
FIFO	–	First-In First-Out
FT	–	Fault Tolerance
HBH	–	Hop-By-Hop
IP	–	Intellectual Property
I/O	–	Input/Output
MinFT	–	Minimal-path Fault Tolerant
NACK	–	Negative Acknowledgement
NI	–	Network Interface
NoC	–	Network-on-Chip
pbr	–	Priority-Based Recovery
PE	–	Processing Element
PL-Adaptive	–	Packet Logging-Adaptive

QoS	–	Quality-of-Service
SoC	–	System-on-Chip
S2S	–	Switch-to-Switch
VBR	–	Variable Bit Rate

LIST OF SYMBOLS

θ	–	Predefined Thresold
$\phi_{k,r_{i,j}}$	–	Value when the k-th packet is transmitted through router $r_{i,j}$
$\phi_{k,r_{i,j,m}}$	–	Value when the k-th packet is transmitted through port m of router $r_{i,j}$
$\varepsilon_{k,r_{i,j}}$	–	Value that indicates whether k-th packet is erroneous or error-free
$\varepsilon_{k,r_{i,j,m}}$	–	Value that indicates whether k-th packet transmitted through port m of router $r_{i,j}$ is erroneous or error-free
$C_{r_{i,j}}$	–	Packet Count on router $r_{i,j}$
$C_{r_{i,j,m}}$	–	Packet Count on port m of router $r_{i,j}$
$l_{i,j}$	–	Link of i-th row and j-th column
$N_{r_{i,j}}$	–	NACK Count on router $r_{i,j}$
$N_{r_{i,j,m}}$	–	NACK Count on port m of router $r_{i,j}$
$Q_{r_{i,j}}$	–	Error Ratio on router $r_{i,j}$
$Q_{r_{i,j,m}}$	–	Error Ratio on port m of router $r_{i,j}$
$r_{i,j}$	–	Router of i-th row and j-th column

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CHAPTER 1

INTRODUCTION

1.1 Background

Complex bus-based System-on-Chip (SoC) architectures can benefit from network-on-chip (NoC) interconnect architecture. NoC is a potential solution for on-chip interconnection by homogenizing connection between processing elements (PEs) with routers and shared links. NoC allows better predictability and scalability of topology [1]. As Very Large Scale Integration (VLSI) fabrication technology advances, component size and interconnects gaps become smaller, resulting in increasing fault and crosstalk occurrences.

NoC design methodology can be divided into application modeling, NoC communication, and NoC design validation [1]. Application modeling is concerned with application mapping with optimized topology, traffic and interconnection. NoC communication is concerned with the flow control scheme and routing algorithm for efficient NoC traffic transmission. On the other hand, NoC design validation is concerned with validating and testing an NoC design. The focus of this thesis is on fault tolerance towards effective NoC communication, which belongs to the last category.

Faults can be categorized in different perspectives such as temporal (transient, intermittent and permanent faults) and spatial (data faults or control faults). These faults result in packet errors or control errors which are detrimental to the NoC functionality for message transfer. Effective detection mechanism and diagnosis information allow fault recovery and even the fault characterization to be performed. Upon the detection of errors, fault diagnosis can only be performed with the information collected from fault detection. Therefore, recovery approaches can be applied, such as [2–5].

In order to handle bit errors in packets, error detection and correction (EDC) have been proposed on mesh-based NoC [2, 6–8]. These basic error detection mechanisms are either the end-to-end (E2E) or switch-to-switch (S2S) EDC [2]. E2E checks packets for error at destinations only, whereas S2S performs error detection at intermediate routers [6]. Several researchers [2–5] analyzed the cost and performance for both mechanisms. Several researchers proposed extensions to existing E2E and S2S EDCs to allow hybrid error detection and correcting mechanisms [2], hop-by-hop retransmission with 3-flit-deep retransmission buffer [3], fault diagnosis method on individual router and adjacent links [5], as well as code-disjoint detection method [4].

1.2 Problem Statement

Several researchers [2–5] have optimized both E2E and S2S EDCs in term of Quality of Service (QoS) performances. The NoC router architecture requires modification to fit in specific fault tolerance feature. Methods were proposed to improve those QoS, but require complex router architecture modification. From analysis in [2–4], it is clearly shown that with low error probability, both EDCs incur similar latency. However, E2E induces lower overhead and S2S requires more overhead at each router [2]. When error probability increases, E2E results in higher packet transmission latency than S2S. This is because each router is penalized for retransmission latency through the source to destination path when retransmission is activated. Due to the different performance of E2E and S2S at different error probabilities, making decision to adaptively choose either E2E or S2S to detect online fault can improve QoS of NoC fault tolerance.

Fault locating is also essential in fault tolerance in order to pinpoint faults on router or link [5]. Knowing the possible location of fault on NoC and the fault type allow the implementation of suitable recovery approach such as packet rerouting due to faulty paths [4]. Existing E2E EDCs is ineffective in locating error on router or link [4, 6]. Due to large numbers of PEs and interconnects, packet retransmission results in low throughput. Hence, a technique to locate faults is required to identify faults either as router or link faults.

1.3 Research Objectives of Research

The goal of this research is to propose an adaptive mechanism for online fault detection on NoC by utilizing existing NACK flow control mechanism. Specifically the objectives of this thesis are:

1. To propose the PL-Adaptive mechanism for adaptive online fault detection on NoC. The packet transmitted through each router as well as NACK will be tracked and used in the decision making to allow routers to switch between E2E and S2S EDC depending on near real-time error probability estimation.
2. To propose a fault-locating and fault type prediction technique. Either router or link faults can be predicted so that NoC priority recovery mechanism can be applied.

1.4 Scope of Research

The work presented in this thesis is scoped as follow. Firstly, the topology which is implemented throughout the thesis is mesh topology. 4×4 mesh topology is used to verify the mechanism because of its simple implementation. Next, YX routing mechanism is implemented for the packet routing. YX routing is used in this thesis for better simulation and analysis because of its simplicity of implementation. This thesis focuses on fault detection where fault recovery mechanism is excluded. The NACK feedback channel is assumed to be error-free. Queuing effect for packet buffering is excluded from the scope of research. A synthetic traffic is implemented to verify all possible paths in all experiments.

1.5 Statement of Contribution

The implementation of PL-Adaptive mechanism enables packet information to be logged by individual router for decision making that improves the overall transmission latency. The contributions of this thesis are as follow.

For fault detection, PL-Adaptive mechanism utilizes NACK logging to switch between E2E and S2S based on different local error ratio on NoC routers. This

results in the reduction of packet retransmission. Since existing NACK flow control is utilized as part of the algorithm, existing NACK information is used instead of sending additional packet information that may require additional processing.

From perspective of fault diagnosis, extracting the online packet fault information from routers enable almost real time fault diagnosis to be performed to detect router and link faults. Therefore, it helps in isolating potential fault locations before suitable fault recovery method can be applied, e.g. path rerouting. High general error ratio on router and certain ports indicate the link fault whereas the high router error ratio on all ports indicate router fault.

1.6 Thesis Organization

This thesis is organized in six chapters. Each chapter is described next.

Chapter 2 deliberates about theoretical background of NoC, fault and packet errors, fault tolerance and packet logging mechanism. Meanwhile, the literature review of current fault tolerance of E2E and S2S trends are discussed. Chapter 3 describes the methodology to carry out the works. The research framework, tool, mechanism and experiment setup are included.

Chapter 4 discusses the idea of PL-Adaptive mechanism on adaptive fault tolerance and the approach of fault tolerance implementation. The algorithm of proposed PL-Adaptive mechanism is also illustrated. Furthermore, experiments and result for simulation are analyzed to discuss the effectiveness of switching between E2E and S2S for different error probabilities.

Chapter 5 discusses about the extended idea of utilizing integrated PL-Adaptive mechanism to adapt for fault type prediction. This is to distinguish fault encountered on router or link. The approach as well as experiments are observed and discussed to analyze the effectiveness of integrated PL-Adaptive to detect router and link fault. Chapter 6 summarizes the thesis idea and objective while reinstates the contribution of the project.

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