MODELING THE EFFECTS OF PHONON SCATTERING IN CARBON NANOTUBE AND SILICON NANOWIRE FIELD-EFFECT TRANSISTORS

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Dedicated to my family.

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ABSTRACT

Carbon nanotubes (CNT) and silicon nanowires (Si NW) are nominated as the channel material for the next generation of transistors. Although previous works have shown that both CNT- and Si NW- based Field-Effect-Transistors (FET) are able to deliver better performance than conventional devices, phonon scattering occurs. The goal of this research is to examine the phonon scattering effects on the performance of CNTFET and Si NWFET. The influence of phonon scattering is incorporated into the models by adding the transmission probability into the Landauer-Buttiker ballistic current equation. Results show that the phonon scattering effects have deteriorated the current and become significant with the increase of bias voltages. At $V_D = 0.1V$, the current of a CNTFET (Si NWFET) has 0.44% (15.2%) of reduction while at $V_D = 0.8V$, the current of a CNTFET (Si NWFET) has degraded by 6.5% (40%). There are two types of phonons, acoustic phonons and optical phonons, with different Mean Free Paths (MFP). The acoustic phonon is the primary cause of current reduction at a low gate bias ($V_G \leq 0.6V$), while the optical phonon is dominant in reducing the current at a high gate bias. Besides, transistors with a short channel length operate close to the ballistic region, which is expected, as they approach the phonon MFP. In addition, the potential of CNTFET and Si NWFET to construct as logic gates is confirmed through Voltage Transfer Characteristic (VTC) by showing correct outputs for a given input. Moreover, the accuracy of the simulation results is assessed by comparing them with published models and experimental data, exhibiting good agreement with both. It is revealed that the use of a high-k dielectric and a thinner oxide are able to suppress the Short Channel Effects (SCE). Finally, it is experimentally proven that the device performance is improved by using a local bottom gate structure for CNTFET and a feedback FET for Si NWFET.

ABSTRAK

Carbon nanotubes (CNT) dan *silicon nanowires* (Si NW) dicadangkan sebagai bahan saluran untuk transistor generasi seterusnya. Penyerakan fonon berlaku dalam Transistor Kesan Medan (FET) berasaskan CNT- dan Si NW- walaupun kajian sebelum ini menunjukkan bahawa ia mempunyai prestasi lebih baik berbanding dengan peranti lazim. Tujuan kajian ini adalah untuk mengkaji kesan penyerakan fonon terhadap prestasi CNTFET dan Si NWFET. Kebarangkalian penghantaran ditambahkan ke persamaan arus balistik Landauer-Buttiker untuk menyepadukan pengaruh penyerakan fonon dalam model. Keputusan menunjukkan bahawa arus merosot akibat kesan penyerakan fonon dan menjadi penting dengan penambahan voltan pincang. Pada $V_D = 0.1V$, arus dalam CNTFET (Si NWFET) berkurang sebanyak 0.44% (15.2%) manakala pada $V_D = 0.8V$, arus dalam CNTFET (Si NWFET) merosot sebanyak 6.5% (40%). Dua jenis fonon, iaitu fonon akustik dan fonon optik, dengan lintasan bebas min fonon (MFP) yang berbeza, di mana fonon akustik merupakan sebab utama pengurangan arus pada get pincang rendah ($V_G \leq 0.6V$) manakala fonon optik dominan dalam pengurangan arus pada get pincang tinggi. Selain itu, seperti yang dijangka, transistor bersaluran pendek mengendali hampir di kawasan balistik kerana ia menuju ke MFP fonon. Tambahan pula, output betul yang ditunjukkan dengan pemberian input melalui Ciri Perpindahan Voltan (VTC) mengesahkan potensi CNTFET dan Si NWFET dibina sebagai get logik. Di samping itu, kejituan keputusan simulasi ditaksir dengan menunjukkan perbandingan yang baik dengan model dan data eksperimen yang terbit. Ia menunjukkan Kesan Saluran Pendek (SCE) dapat dikurangkan dengan menggunakan dielektrik *high-k* dan oksida yang lebih nipis. Akhirnya, eksperimen menunjukkan bahawa penggunaan *local bottom gate structure* untuk CNTFET dan *feedback FET* untuk Si NWFET dapat meningkatkan prestasi peranti.

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LIST OF ABBREVIATIONS

ACNT	-	Armchair CNT
BTBT	-	Band-to-band tunnelling
CNT	-	Carbon nanotube
CNTFET	-	Carbon nanotube field-effect transistor
C-C	-	Carbon to carbon
CVD	-	Chemical vapour deposition
CCNT	-	Chiral CNT
I-V	-	Current-voltage
DOS	-	Density of states
DIBL	-	Drain-induced barrier lowering
GAA	-	Gate all around
IC	-	Integrated circuit
ITRS	-	International Technology Roadmap for Semiconductors
LA	-	Laser ablation
MFP	-	Mean free path
MOSFET	-	Metal -oxide -semiconductor field-effect transistor
MWNT	-	Multi-wall CNT
1D	-	One-dimensional
PECVD	-	Plasma-enhanced CVD
QCL	-	Quantum capacitance limit
SB	-	Schottky-barrier
SCE	-	Short channel effect
Si NW	-	Silicon nanowire
Si NWFET	-	Silicon nanowire field-effect transistor
SWNT	-	Single-wall CNT

3D	-	Three-dimensional
2D	-	Two-dimensional
UTB	-	Ultra-thin-body
VTC	-	Voltage transfer characteristic
0D	-	Zero-dimensional
ZCNT	-	Zigzag CNT

LIST OF SYMBOLS

C_{QC_D}, C_{QS_D}	-	C_Q for a CNT and a Si NW at degenerate limits
C_{QC_ND}, C_{QS_ND}	-	C_Q for a CNT and a Si NW at non-degenerate limits
$L_{ac,300}$	-	L_{ac} at room temperature for a CNT with a specific diameter
$L_{op,300}$	-	L_{op} of the CNT at room temperature
a_0	-	$a_0 = 0.529 \text{Å} m$, Bohr radius
a_{cc}	-	$a_{cc} = 1.42 \text{Å}$, Distance between two carbon atoms
k_B	-	$k_B = 1.381 \times 10^{-23} JK^{-1}$, Boltzmann's constant
m_l	-	$m_l = 0.98 m_0$, Longitudinal mass of an electron
m_t	-	$m_t = 0.19 m_0$,Transverse mass of an electron
ε_0	-	$\varepsilon_0 = 8.854 \times 10^{-12} Fm^{-1}$, Vacuum permittivity
$L_{op,abs}$, $L_{op,ems}$	-	Absorption or emission optical MFP
D_{ac}, D_{op}	-	Acoustic or optical phonon deformation potential
L_{ac}, L_{op}	-	Acoustic or optical phonon scattering MFP
w_{ac}, w_{op}	-	Acoustic or optical phonon scattering rate
τ_{ac}, τ_{op}	-	Acoustic or optical phonon scattering time
E_g	-	Bandgap
V_L	-	Barrier potential that is lowered down by V_G and V_D
V_G, V_D, V_S		Bias voltages of the gate, drain and source
ε	-	Bottom of the subband
C_G, C_D, C_S		Capacitance of the gate, drain and source
$\langle \tau \rangle$	-	Carriers' average scattering time
L	-	Channel length

θ_c	-	Chiral angle
$\vec{C}$	-	Chiral vector
$\left\|\vec{C}\right\|$	-	Circumference of a CNT
l_c	-	Confined length in the x-, y- or z direction
D_0	-	Constant density of states of a metallic nanotube
ρ	-	Crystal density
$D(E)$	-	Density of states of the channel
d	-	Diameter
K	-	Dirac points
λ_n	-	Discrete wavelength
$D_{0D}(E)$, $D_{1D}(E)$, $D_{2D}(E)$, $D_{3D}(E)$	-	DOS of 0D, 1D, 2D or 3D material
I_D	-	Drain current
m_d^*	-	Effective density of states mass
N_{3D}, N_{2D}, N_{1D}	-	Effective DOS for 3D, 2D and 1D
N_{CNT}, $N_{Si\,NW}$	-	Effective DOS for a CNT or a Si NW
m^*	-	Effective mass
L_{eff}	-	Effective MFP
v_e	-	Electron velocity
C_E	-	Electrostatic capacitance
E	-	Energy
E_{ACNT}, E_{ZCNT}	-	Energy dispersion of ACNT and ZCNT
$E(\vec{K})$	-	Energy dispersion of graphene
N_0, N_S, N_D	-	Equilibrium, source and drain carrier density
T_E	-	Eutectic temperature
E_F	-	Fermi energy
$f(E)$	-	Fermi function
$F_{1/2}$, F_0,	-	Fermi-Dirac integral of order $1/2$, 0 and $-1/2$

$F_{-1/2}$		
Γ	-	Gamma function
$\alpha_{\mathrm{G}}, \alpha_{\mathrm{D}}$	-	Gate and drain control parameters
D_R	-	Greatest common factor
$\hbar$	-	$\hbar = 1.055 \times 10^{-34} Js$, Reduced Planck constant
NM_H, NM_L	-	High and low noise margins
V_{In}, V_{Out}	-	Input and output voltage
ε_r	-	Insulator dielectric constant
L_x, L_y, L_z	-	Length in the x-, y- and z- directions
$\lvert\vec{T}\rvert$	-	Length of a CNT
λ_0	-	Mean free path
ΔQ	-	Mobile charge
μ	-	Mobility
J	-	Net flux
N_{state}	-	Number of available quantum states
N	-	Number of hexagons per unit cell
$N_{op}(T)$	-	Number of optical phonons
ω_0	-	Optical phonon angular frequency
E_{op}	-	Optical phonon energy
t	-	Oxide thickness
$+k, -k$	-	Positive and negative velocity states
J^+, J^-	-	Positive- and negative-going carrier flux
$\overrightarrow{a_1}, \overrightarrow{a_2}$	-	Primitive unit vectors
C_Q	-	Quantum capacitance
l, m, n	-	Quantum numbers of the energy levels
r	-	Radius of the tube
$\overrightarrow{b_1}, \overrightarrow{b_2}$	-	Reciprocal lattice vectors
V_{sc}	-	Self-consistent potential
V_p	-	Shift up potential by ΔQ
t_{Si} , w_{Si}	-	Si body thickness and width
V_{state}, A_{state},	-	Smallest nonzero volume, area or width

L_{state}		
v_s	-	Sound velocity
E_{F1}, E_{F2}	-	Source and drain Fermi levels
T_S, T_D	-	Source or drain transmission probability
V_m	-	Switching threshold
T	-	Temperature
dx	-	Thickness of a semiconductor
V_T	-	Threshold voltage
C_Σ	-	Total capacitance
$E_{3D}, E_{2D},$ E_{1D}, E_{0D}	-	Total energy for 3D, 2D, 1D and 0D
N_{tot}	-	Total number of available quantum states
N'_{tot}	-	Total number of available quantum states per unit volume, area or length
$\vec{T}$	-	Translational vector
T_r	-	Transmission probability
$V_k,\ A_k,\ L_k$	-	Volume, area or length at k-space
k	-	Wave vector
w_{Wire}	-	Wire width
e	-	$e = 1.602 \times 10^{-19} C$, Electron charge
α	-	$\alpha \sim 3.0 eV$, C-C bonding energy

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CHAPTER 1

INTRODUCTION

1.1 Background

The scaling law introduced by Robert Dennard in 1974, known as Dennard scaling, indicates that transistor density, switching speed and power dissipation should improve with a scaling trend. Dennard scaling is related to Moore's Law, which states that the number of transistors that can be placed on a single die doubles every two years. It is expected that the chip size is reduced by approximately 0.7 times by each new development of an integrated circuit (IC) [1].

Each generation of downscale transistors aims to enhance the overall performance by providing higher speed, lower power, and higher packing density. However, the physical limitations of the materials and tools have restricted the scaling trend. The International Technology Roadmap for Semiconductors (ITRS) has noted that the semiconductor industry is entering the Third Era of Scaling, or 3D Power Scaling, where the number of transistors can be increased by stacking multiple layers of transistors to prolong the scaling trend [2].

Table 1.1 : Challenges in scaling [2].

Near-term (2013-2020)	1. Fluctuation of threshold voltage. 2. Reduction of saturation current. 3. Mobility degradation. 4. Difficulties in controlling the leakage current.
Long-term (2021-2028)	1. Reliability of new materials. 2. Problems in scaling the supply power. 3. Complexity of circuit design. 4. Integration of multiple functions into a single chip. 5. Difficulties in using 3-D integration to increase the chip density.

The obstacles in scaling the physical dimensions of transistors can generally be divided into near-term and long-term challenges. First, the use of high-k materials will cause variations in the threshold voltage and a deterioration in mobility. The decreasing of the saturation current and the control of the leakage current on small-size transistors are also concerns that represent near-term problems. Meanwhile, the uncertainty of the characteristics of new materials and the difficulties in scaling the supply power are among the long-term challenges. Problems in increasing the functionality and chip density have also added to the complexity of circuit design. Table 1.1 lists the challenges mentioned above.

Novel materials such as carbon nanotubes (CNT) have been introduced to overcome the limitations faced by current technology. In late 1991, Iijima discovered multi-walled CNTs (MWNT), which contains at least two layers of graphite with an inner diameter of 4 nm, when he was studying fullerene synthesis by arc discharge. Since then, CNTs have started to attract more interest. Two years later, in 1993, Iijima *et al*. used the same method to synthesize single-wall CNTs (SWNT) [3].

Along with the intensive research on CNTs, silicon nanowires (Si NW) have also attracted the attention from researchers. In 1964, Wagner and Ellis successfully

synthesize silicon whiskers using a vapour-liquid-solid (VLS) mechanism that set the basis for the growth of Si NWs. In 1998, Morales and Lieber synthesized Si NWs with nanometres dimensions and introduced laser ablation (LA) as a new technique to synthesize Si NWs [4].

1.2 Problem Statements

One-dimensional (1D) materials such as Si NWs and CNTs have been proposed as potential candidates for future generations of semiconductors due to their superior electrostatic performance over the bulk complementary metal-oxide-semiconductor (CMOS) devices that suffer from short channel effect (SCE) as the physical dimensions of transistors continue to decrease. The common SCEs experienced by short channel devices include [5]:

1. Drain-induced barrier lowering (DIBL), in which the increased drain voltage lowers the potential barrier between the source and the channel, causing the reduction of the threshold voltage and contributing to a higher leakage current.
2. The switching speed between the ON and OFF states becomes slower, i.e., the subthreshold swing (SS) is increased.

Carbon-based transistors have been proposed to solve these problems and prolong the life of Moore's Law. Thus, the use of a new and reliable material, CNTs, is recommended due to its high carrier mobility and long mean free path (MFP), which can deliver excellent performance on electronic circuits. The cylindrical structure of Si NWs also exhibits excellent properties compared to a planar structure, providing another way to continue device scaling by reducing the SCE.

Table 1.2 : CNTs and Si NWs characteristics.

CNTs [6]	1. 1D structure enables a ballistic transportation of carriers. 2. Able to withstand under extreme condition due to the strong covalent bond between the atoms. 3. Exhibit metallic and semiconducting behavior which is useful as transistor and interconnect.
Si NWs	1. Good gate controllability to suppress leakage current and SCE [5]. 2. Gate capacitance is inversely proportional to the wire diameter [7]. 3. Compatible with recent Si-based technology.

The extraordinary properties of CNTs and Si NWs, as listed in Table 1.2, have driven researchers to investigate the potential for CNTs and Si NWs to be used in future technology. It has been shown that CNTFETs and Si NWFETs are able to work as logic gates [8] outperforming the traditional MOSFETs [9, 10]. Indeed, the carrier transport in CNTFETs and Si NWFETs are affected by phonons, as shown in previous research, which is listed in section 2.16. However, there is lack of discussion on the effect of phonons on device performance. Therefore, it is important to evaluate the impact of phonon scattering in CNTFETs and Si NWFETs, as they are potential devices for the next generation of transistors. In short, the questions that arise in the research are:

1. How to examine the phonon scattering effects in CNTFETs and Si NWFETs?
2. What is the role of acoustic and optical phonons on CNTFETs and Si NWFETs at different gate biases?
3. What is the device performance of CNTFET and Si NWFET models upon experiencing phonon scattering effects?

1.3 Objectives

The objectives of the research are:

1. To improve channel length-dependent models of CNTFETs and Si NWFETs to study the phonon scattering effects.
2. To examine the effect of acoustic and optical phonons based on the current-voltage (I-V) characteristic of CNTFETs and Si NWFETs at different gate biases.
3. To verify the potential of the channel length-dependent models of CNTFETs and Si NWFETs to work as logic gates and the accuracy by experiencing phonon scattering effects.

1.4 Scopes

MATLAB is used to perform the simulations. The ballistic FETToy model of CNTFETs and Si NWFETs is modified by transforming it into channel length-dependent models. The Landauer-Buttiker mechanism is used to express the ballistic current equation, and the phonon scattering effects are incorporated into the models by introducing the transmission probability at each contact into the ballistic current equation. The role of the acoustic and optical phonons at different gate biasing is also investigated. Next, the ballisticity of CNTFETs and Si NWFETs at different channel lengths is examined. Performance metrics such as DIBL, SS and on-off ratio are calculated. The potential of CNTFETs and Si NWFETs to work as logic gates is determined through the voltage transfer characteristic (VTC). Finally, the device performances are compared with published models and experimental data to assess the accuracy of the simulation results.

1.5 Contributions

This research has developed a channel length-dependent model of CNTFETs and Si NWFETs to investigate the phonon scattering effects in the devices. The impact of phonon scattering is incorporated into the models by introducing the transmission probability at the source and drain sides. The transmission probability is a simple equation, which is a function of the channel length and the effective mean free path (MFP). The role of acoustic and optical phonons at different gate biases towards the drive current is discussed. CNTFETs and Si NWFETs are able to construct as logic gates by showing correct outputs for a given inputs through VTC.

1.6 Thesis Organization

Chapter 1 introduces the background of the research by briefly discussing the challenges in downsizing conventional MOSFETs and the advantages of CNTs and Si NWs as potential candidates for use as channel materials. The motivation of this research is defined through the problem statements, objectives and scopes. The contributions of the research will also be described. Chapter 2 discusses the basic theory and the methods used to synthesize CNT and Si NW. Next, the MOSFET operation, basic physics of semiconductor, fundamental of ballistic transistor and phonon scattering are described, followed by the review on the modelling works. Chapter 3 presents the flow of this research and the simulation steps used in MATLAB to compute the results. Chapter 4 discusses. The performance difference between the ballistic and the phonon scattering effects on the devices will also be discussed. Next, the potential of CNTFETs and Si NWFETs to be used as logic gates are investigated. The accuracy of the results is assessed against published models and experimental data. Chapter 5 presents the conclusions and summarizes the research based on the results obtained. Future work and recommendations are included, as well.

REFERENCES

1. Bohr, M., *A 30 year retrospective on Dennard's MOSFET scaling paper.* Solid-State Circuits Society Newsletter, IEEE, 2007. **12**(1): p. 11-13.
2. *International Technology Roadmap for Semiconductors.* . 2013 Edition.
3. Iijima, S., *Helical microtubules of graphitic carbon.* Nature, 1991. **354**(6348): p. 56-58.
4. Morales, A.M. and C.M. Lieber, *A laser ablation method for the synthesis of crystalline semiconductor nanowires.* Science, 1998. **279**(5348): p. 208-211.
5. Fasoli, A. and W.I. Milne, *Overview and status of bottom-up silicon nanowire electronics.* Materials Science in Semiconductor Processing, 2012. **15**(6): p. 601-614.
6. Avouris, P., et al., *Carbon nanotube electronics.* Proceedings of the IEEE, 2003. **91**(11): p. 1772-1784.
7. Kwong, D.-L., et al., *Vertical silicon nanowire platform for low power electronics and clean energy applications.* Journal of Nanotechnology, 2011. **2012**.
8. Chin, H.C., et al., *Quasi-One-Dimensional Performance and Benchmarking of CMOS-Based Multichannel Carbon Nanotube versus Nanowire Field-Effect Transistor Models.* Science of Advanced Materials, 2015. **7**(1): p. 178-189.
9. Chin, H.C., N.H.B. Mohamad, and M.L.P. Tan, *Performance Benchmarking of 32 nm Predictive Technology Model CMOS with Silicon Nanowire Physic-Based Compact Model of Field-Effect Transistors for Digital Logic Applications.* Science of Advanced Materials, 2014. **6**(3): p. 596-602.
10. Tan, M.L.P. and G. Lentaris, *Device and circuit-level performance of carbon nanotube field-effect transistor with benchmarking against a nano-MOSFET.* Nanoscale research letters, 2012. **7**(1): p. 1-10.
11. Andrei, E.Y., G. Li, and X. Du, *Electronic properties of graphene: A perspective from scanning tunneling microscopy and magneto-transport.* arXiv preprint arXiv:1204.4532, 2012.
12. Park, J.-Y., *Band Structure and Electron Transport Physics of One-Dimensional SWNTs*, in *Carbon Nanotube Electronics*, J. Kong and A. Javey, Editors. 2009, Springer US. p. 1-42.
13. Lundstrom, M. and J. Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation*2006: Springer.
14. Lundstrom, M. and J. Guo, *Nanowire Field-Effect Transistors*, in *Nanoscale Transistors: Device Physics, Modeling and Simulation*2006, Springer US. p. 140-181.

15. Wong, H.-S.P. and D. Akinwande, *Carbon nanotubes*, in *Carbon Nanotube and Graphene Device Physics*2010, Cambridge University Press. p. 73-98.
16. Krueger, A., *Carbon Nanotubes*, in *Carbon Materials and Nanotechnology*2010, Wiley-VCH Verlag GmbH & Co. KGaA. p. 123-281.
17. Ismail, R., M.T. Ahmadi, and S. Anwar, *Advanced Nanoelectronics*2012: Taylor & Francis.
18. Deji, A., Wong, P.H.S., *Carbon Nanotube and Graphene Device Physics*2011, United States of America: Cambridge University Press, New York.
19. Nessim, G.D., *Properties, synthesis, and growth mechanisms of carbon nanotubes with special focus on thermal chemical vapor deposition.* Nanoscale, 2010. **2**(8): p. 1306-1323.
20. Meyyappan, M., *A review of plasma enhanced chemical vapour deposition of carbon nanotubes.* Journal of Physics D: Applied Physics, 2009. **42**(21): p. 213001.
21. Kumar, M. and Y. Ando, *Chemical vapor deposition of carbon nanotubes: a review on growth mechanism and mass production.* Journal of nanoscience and nanotechnology, 2010. **10**(6): p. 3739-3758.
22. Koziol, K., B.O. Boskovic, and N. Yahya, *Synthesis of Carbon Nanostructures by CVD Method*, in *Carbon and Oxide Nanostructures*2011, Springer. p. 23-49.
23. Rafique, M.M.A. and J. Iqbal, *Production of Carbon Nanotubes by Different Routes-A Review.* Journal of Encapsulation and Adsorption Sciences, 2011. **1**(02): p. 29.
24. Szabó, A., et al., *Synthesis methods of carbon nanotubes and related materials.* Materials, 2010. **3**(5): p. 3092-3140.
25. Singh, I., Rehni, A.K., Kumar, P., Kumar, M., and Hassan Y.A.E., *Carbon Nanotubes: Synthesis, Properties and Pharmaceutical Applications.* 2009. **17**(4): p. 361-377.
26. Hayden, O. and K. Nielsch, *Molecular- and Nano-Tubes*2011: Springer.
27. Zhihong, C., et al., *Externally Assembled Gate-All-Around Carbon Nanotube Field-Effect Transistor.* Electron Device Letters, IEEE, 2008. **29**(2): p. 183-185.
28. Chang, L., et al., *Moore's law lives on [CMOS transistors]*. Circuits and Devices Magazine, IEEE, 2003. **19**(1): p. 35-42.
29. Gupta, K., et al. *Non-classical scaling approaches for ultra deep sub micron technology*. in *Emerging Trends in Communication, Control, Signal Processing & Computing Applications (C2SPCA), 2013 International Conference on*. 2013.
30. Singh, N., et al., *High-performance fully depleted silicon nanowire (diameter $\leq$ 5 nm) gate-all-around CMOS devices.* Electron Device Letters, IEEE, 2006. **27**(5): p. 383-386.
31. Paul, B.C., et al., *An analytical compact circuit model for nanowire FET.* Electron Devices, IEEE Transactions on, 2007. **54**(7): p. 1637-1644.
32. Liang, G. *Structure Effects in the gate-all-around Silicon Nanowire MOSFETs*. in *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on*. 2007. IEEE.
33. Colinge, J.P. and S.H. Dhong. *Prospective for nanowire transistors*. in *Custom Integrated Circuits Conference (CICC), 2013 IEEE*. 2013.
34. Cui, Y., et al., *High performance silicon nanowire field effect transistors.* Nano letters, 2003. **3**(2): p. 149-152.

35. Wang, J., *Device physics and simulation of silicon nanowire transistors*, 2005, Citeseer.
36. Shao, M., D.D.D. Ma, and S.-T. Lee, *Silicon Nanowires – Synthesis, Properties, and Applications.* European Journal of Inorganic Chemistry, 2010. **2010**(27): p. 4264-4278.
37. Dresselhaus, M.S., et al., *Nanowires*, in *Springer Handbook of Nanotechnology*2010, Springer. p. 119-167.
38. Meng, C.-Y., B.-L. Shih, and S.-C. Lee, *Silicon nanowires synthesized by vapor–liquid–solid growth on excimer laser annealed thin gold film.* Journal of Nanoparticle Research, 2007. **9**(4): p. 657-660.
39. Natori, K., *Ballistic/quasi-ballistic transport in nanoscale transistor.* Applied surface science, 2008. **254**(19): p. 6194-6198.
40. Serway, R. and J. Jewett, *Physics for Scientists and Engineers*2012: Cengage Learning.
41. Mansfield, M. and C. O'Sullivan, *Understanding Physics*2010: John Wiley & Sons.
42. Kumar, C.S.S.R., *Semiconductor Nanomaterials*2010: Wiley.
43. Sattler, K.D., *Handbook of Nanophysics: Nanoparticles and Quantum Dots*2010: Taylor & Francis.
44. YU, P. and M. Cardona, *Fundamentals of Semiconductors: Physics and Materials Properties*2010: Springer.
45. Korkin, A., et al., *Nanotechnology for Electronic Materials and Devices*2010: Springer.
46. Kuno, M., *Introductory Nanoscience*2011: Garland Science.
47. Mino, L., et al., *Low-dimensional systems investigated by x-ray absorption spectroscopy: a selection of 2D, 1D and 0D cases.* Journal of Physics D: Applied Physics, 2013. **46**(42): p. 423001.
48. Ahmadi, M.T., et al., *Analytical Study of Carriers in Silicon Nanowires.* MASAUM Journal of Basic and Applied Sciences, 2009. **1**(2): p. 233-239.
49. Srivastava, A., et al., *Current transport modeling of carbon nanotube field effect transistors.* physica status solidi (a), 2009. **206**(7): p. 1569-1578.
50. Wunnicke, O., *Gate capacitance of back-gated nanowire field-effect transistors.* Applied Physics Letters, 2006. **89**(8): p. 083102.
51. Burke, P.J. *An RF circuit model for carbon nanotubes*. in *Nanotechnology, 2002. IEEE-NANO 2002. Proceedings of the 2002 2nd IEEE Conference on*. 2002. IEEE.
52. Knoch, J., et al. *One-dimensional nanoelectronic devices-towards the quantum capacitance limit*. in *Device Research Conference, 2008*. 2008. IEEE.
53. Ahmadi, M.T., et al. *Carbon Nanotube Capacitance Model in Degenerate and Nondegenerate Regimes*. in *Proceedings of the Fourth Global Conference on Power Control and Optimization*. 2011. AIP Publishing.
54. Wong, H.S.P. and D. Akinwande, *Carbon Nanotube and Graphene Device Physics*2011: Cambridge University Press.
55. Waser, R., *Nanoelectronics and Information Technology*2012: Wiley.
56. Rahman, A., et al., *Theory of ballistic nanotransistors.* Electron Devices, IEEE Transactions on, 2003. **50**(9): p. 1853-1864.
57. Hamaguchi, C., *Electron—Phonon Interaction and Electron Transport*, in *Basic Semiconductor Physics*2010, Springer Berlin Heidelberg. p. 207-286.

58. Singh, J., *LATTICE VIBRATIONS: PHONON SCATTERING*, in *Electronic and Optoelectronic Properties of Semiconductor Structures*2003, Cambridge University Press. p. 217-259.
59. Natori, K., *Compact modeling of quasi-ballistic silicon nanowire MOSFETs.* Electron Devices, IEEE Transactions on, 2012. **59**(1): p. 79-86.
60. Deng, J. and H.-S. Wong, *A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region.* Electron Devices, IEEE Transactions on, 2007. **54**(12): p. 3186-3194.
61. Pourfath, M., H. Kosina, and S. Selberherr. *The effect of inelastic phonon scattering on carbon nanotube-based transistor performance*. in *Journal of Physics: Conference Series*. 2008. IOP Publishing.
62. Grassi, R., et al., *Phonon-scattering effects in CNT-FETs with different dimensions and dielectric materials.* Solid-state electronics, 2008. **52**(9): p. 1329-1335.
63. Zhao, Y., A. Liao, and E. Pop, *Multiband mobility in semiconducting carbon nanotubes.* Electron Device Letters, IEEE, 2009. **30**(10): p. 1078-1080.
64. Xu, B., et al., *The effect of acoustic phonon scattering on the carrier mobility in the semiconducting zigzag single wall carbon nanotubes.* Applied Physics Letters, 2010. **96**(18): p. 183108.
65. Frégonese, S., et al., *Implementation of electron–phonon scattering in a CNTFET compact model.* Electron Devices, IEEE Transactions on, 2009. **56**(6): p. 1184-1190.
66. Kazmierski, T.J., et al., *Numerically efficient modeling of CNT transistors with ballistic and nonballistic effects for circuit simulation.* Nanotechnology, IEEE Transactions on, 2010. **9**(1): p. 99-107.
67. Bushmaker, A.W., M.R. Amer, and S.B. Cronin, *Electrical transport and channel length modulation in semiconducting carbon nanotube field effect transistors.* Nanotechnology, IEEE Transactions on, 2014. **13**(2): p. 176-181.
68. Buin, A., A. Verma, and M. Anantram, *Carrier-phonon interaction in small cross-sectional silicon nanowires.* Journal of applied physics, 2008. **104**(5): p. 053716.
69. Luisier, M. and G. Klimeck, *Atomistic full-band simulations of silicon nanowire transistors: Effects of electron-phonon scattering.* Physical Review B, 2009. **80**(15): p. 155430.
70. Bescond, M., et al., *Modeling of phonon scattering in n-type nanowire transistors using one-shot analytic continuation technique.* Journal of applied physics, 2013. **114**(15): p. 153712.
71. Akhavan, N.D., et al., *Effect of intravalley acoustic phonon scattering on quantum transport in multigate silicon nanowire metal-oxide-semiconductor field-effect transistors.* Journal of applied physics, 2010. **108**(3): p. 034510.
72. Aldegunde, M., A. Martinez, and A. Asenov, *Non-equilibrium Green's function analysis of cross section and channel length dependence of phonon scattering and its impact on the performance of Si nanowire field effect transistors.* Journal of applied physics, 2011. **110**(9): p. 094518.
73. Akhavan, N.D., et al., *Influence of elastic and inelastic electron–phonon interaction on quantum transport in multigate silicon nanowire MOSFETs.* Electron Devices, IEEE Transactions on, 2011. **58**(4): p. 1029-1037.

74. Akhavan, N.D., et al., *Emission and absorption of optical phonons in multigate silicon nanowire MOSFETs.* Journal of Computational Electronics, 2012. **11**(3): p. 249-265.
75. Koswatta, S.O., et al., *Ballisticity of nanotube field-effect transistors: Role of phonon energy and gate bias.* Applied Physics Letters, 2006. **89**(2): p. 023125.
76. Tsuchiya, H. and S.-i. Takagi, *Influence of elastic and inelastic phonon scattering on the drive current of quasi-ballistic MOSFETs.* Electron Devices, IEEE Transactions on, 2008. **55**(9): p. 2397-2402.
77. Ahmed, S. and K. Alam. *Effects of phonon scattering on the performance of silicon nanowire transistors*. in *Electrical and Computer Engineering (ICECE), 2010 International Conference on*. 2010. IEEE.
78. Guo, J. and M. Lundstrom, *Role of phonon scattering in carbon nanotube field-effect transistors.* Applied Physics Letters, 2005. **86**(19): p. 193103.
79. Aldegunde, M., A. Martinez, and J. Barker, *Study of individual phonon scattering mechanisms and the validity of Matthiessen's rule in a gate-all-around silicon nanowire transistor.* Journal of applied physics, 2013. **113**(1): p. 014501.
80. Chen, W.K., *The Electrical Engineering Handbook*2004: Elsevier Science.
81. Murali, R., *Graphene Nanoelectronics: From Materials to Circuits*2012: Springer.
82. Luo, J., et al., *Compact Model for Carbon Nanotube Field-Effect Transistors Including Nonidealities and Calibrated With Experimental Data Down to 9-nm Gate Length.* IEEE transactions on electron devices, 2013. **60**(6): p. 1834-1843.
83. Mehrotra, S.R., *A Simulation Study of Silicon Nanowire Field Effect Transistors (FETs)*, 2007, University of Cincinnati.
84. Hong, B., et al., *Subthreshold degradation of gate-all-around silicon nanowire field-effect transistors: Effect of interface trap charge.* Electron Device Letters, IEEE, 2011. **32**(9): p. 1179-1181.
85. Liang, S., et al., *High-performance carbon-nanotube-based complementary field-effect-transistors and integrated circuits with yttrium oxide.* Applied Physics Letters, 2014. **105**(6): p. 063101.
86. Van, N.H., et al., *High performance Si nanowire field-effect-transistors based on a CMOS inverter with tunable threshold voltage.* Nanoscale, 2014. **6**(10): p. 5479-5483.
87. Maehashi, K., et al. *Fabrication of high-performance voltage inverters based on carbon nanotube field-effect transistors*. in *Nanotechnology Materials and Devices Conference (NMDC), 2010 IEEE*. 2010. IEEE.
88. Rustagi, S., et al., *CMOS inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach.* Electron Device Letters, IEEE, 2007. **28**(11): p. 1021-1024.
89. Kazmierski, T.J., D. Zhou, and B.M. Al-Hashimi. *Efficient circuit-level modelling of ballistic CNT using piecewise non-linear approximation of mobile charge density*. in *Design, Automation and Test in Europe, 2008. DATE'08*. 2008. IEEE.
90. Alam, K. and R.K. Lake, *Dielectric scaling of a zero-Schottky-barrier, 5nm gate, carbon nanotube transistor with source/drain underlaps.* Journal of applied physics, 2006. **100**(2): p. 024317.

91. Nayak, K., et al., *CMOS logic device and circuit performance of Si gate all around nanowire MOSFET.* Electron Devices, IEEE Transactions on, 2014. **61**(9): p. 3066-3074.
92. Bhowmick, S. and K. Alam, *Dielectric scaling of a top gate silicon nanowire on insulator transistor.* Journal of applied physics, 2008. **104**(12): p. 124308-124308-6.
93. Chang-Ki, B., et al., *Characteristics of gate-all-around silicon nanowire field effect transistors with asymmetric channel width and source/drain doping concentration.* Journal of applied physics, 2012. **112**(3): p. 034513-034513-5.
94. Yang, M.-H., et al., *Advantages of top-gate, high-k dielectric carbon nanotube field-effect transistors.* Applied Physics Letters, 2006. **88**(11): p. 113507.
95. Lee, T.-C., et al., *A process for high yield and high performance carbon nanotube field effect transistors.* Microelectronics Reliability, 2010. **50**(5): p. 666-669.
96. Franklin, A.D. and Z. Chen, *Length scaling of carbon nanotube transistors.* Nature nanotechnology, 2010. **5**(12): p. 858-862.
97. Grobert, N., *Carbon nanotubes – becoming clean.* Materials Today, 2007. **10**(1–2): p. 28-35.
98. Franklin, A.D., N.A. Bojarczuk, and M. Copel, *Consistently low subthreshold swing in carbon nanotube transistors using lanthanum oxide.* Applied Physics Letters, 2013. **102**(1): p. 013108.
99. Li, M., et al. *Sub-10 nm gate-all-around CMOS nanowire transistors on bulk Si substrate*. in *VLSI Technology, 2009 Symposium on*. 2009. IEEE.
100. Moon, D.I., et al., *Silicon nanowire all-around gate MOSFETs built on a bulk substrate by all plasma-etching routes.* Electron Device Letters, IEEE, 2011. **32**(4): p. 452-454.
101. Jeon, Y., et al., *Switching Characteristics of Nanowire Feedback Field-Effect Transistors with Nanocrystal Charge Spacers on Plastic Substrates.* ACS nano, 2014. **8**(4): p. 3781-3787.