ENHANCING SRAM PERFORMANCE OF COMMON GATE FINFET BY USING CONTROLLABLE INDEPENDENT DOUBLE GATES

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Specially dedicated to my beloved family, lecturers and friends
For the guidance, encouragement and inspiration
Throughout my journey of education

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ABSTRACT

This project is focus on the research and evaluation on the characteristic of independent controllable gate FinFET structure in static random access memory (SRAM) circuitry. BSIM-CMG model for common gate FinFET is chosen in this research. The independent controllable gate FinFET is constructed using two parallel connection of common gate FinFET except the gate terminal, thus it has the independent controllable gate capability. SRAM 6T scheme is being chosen in this study and benchmarking with the conventional common gate FinFET SRAM. Netlist for device NMOS and PMOS, and the SRAM circuitry are being constructed and simulated with HSPICE tool. From the device perspective, through the dynamic gate voltage adjustment capability, the IV characteristic of this proposed structure has better drive currents with 1.1X for NMOS and 1.3X for PMOS compare to conventional common gate FinFET. Besides that, there is a significant reduction of leakage current in this proposed structure compare to the conventional common gate FinFET, the reduction leakage for NMOS and PMOS is up to 3 order magnitude. The results of the SRAM circuitry constructed by this proposed independent controllable gate FinFET structure has shown that the read and write margin are higher than the conventional common gate FinFET SRAM design. Besides that, the proposed structure in SRAM design is beneficial to low power application design as it has lower standby current. Furthermore, different back gate bias scheme for this structure is explored, and the optimum back gate scheme is proposed which having the reverse biased on Pull Down device and Pull Up device, with the dynamic gate voltage control on the Pass Gate device.

ABSTRAK

Projek ini bertujuan untuk memberi penyelidikan dan penilaian tentang ciri-ciri bebas kawalan get FinFET struktur dalam litar pegun rawak laluan ingatan (SRAM). Dalam kajian ini, pengunaan BSIM-CMG model untuk get samaan FinFET dipilih. Bebas kawalan get FinFET struktur dibina daripada dua sambungan selari get samaan FinFET, dua get dibiarkan untuk membentuk ciri bebas kawalan. SRAM 6T skema dipilih dalam kajian ini dan dibandingkan dengan get samaan FinFET SRAM. Semua peranti NMOS, PMOS dan litar SRAM disimulasikan oleh alat HSPICE, di mana ia merupakan industry piawai. Dari segi peranti, ciri IV untuk bebas kawalan jet FinFET memiliki lebih banyak arus pengaliran dengan 1.1X untuk NMOS dan 1.3X untuk PMOS dibandingkan the get samaan FinFET. Di samping itu, arus bocoran untuk bebas kawalan get FinFET struktur adalah kurang daripada tradisi get samaan FinFET sebanyak tiga magnitude apabila dibandingkan dengan tradisi get samaan FinFET. Keputusan untuk bebas kawalan get FinFET struktur dalam litar SRAM adalah lebih baik dari segi pembacaan dan penulisan margin apabila dibandingkan dengan rekabentuk dalam tradisi get samaan FinFET SRAM. Cadangan struktur ini dalam litar rekabentuk SRAM memberi kebaikan dalam bidang kegunaan kuasa rendah kerana ia mempunyai arus bocor yang rendah. Di samping itu, berbeza-beza skema belakang get voltan pincang juga disiasat dan optimum skema belakang get voltage pincang telah diperkenalkan, di mana ia mempunyai terbalik pincang kepada Tarik Ke-bawah dan Tarik Ke-atas peranti, dengan dinamik kawalan get voltan kepada Lalu Get peranti.

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LIST OF ABBREVIATIONS

SRAM	-	Static Random Access Memory
MOSFET	-	Metal–Oxide–Semiconductor Field-Effect Transistor
SCE	-	Short Channel Effects
LDE	-	Layout Dependent Effects
GIDL	-	Gate Induced Drain Leakage
RDF	-	Random Dopant Fluctuations
CMC	-	Compact Modeling Council
NMOS	-	N-channel Metal-Oxide-Semiconductor
PMOS	-	P-channel Metal-Oxide-Semiconductor
W	-	Width
L	-	Length
SNM	-	Static Noise Margin
RNM	-	Read Noise Margin
WNM	-	Write Noise Margin
V_{th}	-	Threshold Voltage
IG	-	Independent Gate
SG	-	Shorted Gate
DG	-	Double Gate
RSNM	-	Read Static Noise Margin
PG	-	Pass Gate
PU	-	Pull Up
PD	-	Pull Down
AR	-	Aspect Ratio
PGFB	-	Pass Gate Feedback
PUWG	-	Pull Up Write Gating
BSIM	-	Berkeley Short-channel IGFET Model
PTM	-	Predictive Technology Model

PSP	-	Penn State-Philips
HICUM	-	High Current Model
BSIM-CMG	-	BSIM Common Multi-Gate
CMC	-	Compact Modeling Council
SINM	-	Static Current Noise Margin
WTI	-	Write Trip Current
CG	-	Controllable Gate

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CHAPTER 1

INTRODUCTION

1.1 Background

Semiconductor memories can be categorized as volatile and non-volatile type. The main difference between volatile memory and non-volatile memory is that volatile type only retain the data when there is a power supply but non-volatile type can obtain the stored information even though it is not powered. Volatile type is widely use as primary storage in semiconductor design because it is faster, reliable and cost effective compare to non-volatile type of memory. Static Random Access Memory (SRAM) is classified as volatile memory.

In VLSI design especially multi core processor architectures, the demand of on-chip caches for data sharing and storage efficiency is high and important across parallel processing units [1]. The memory is designed in SRAM array thus it is occupying a large fraction of chip area in many design nowadays. In the recent deep submicron technology, both static and dynamic power dissipated is high. Static power dissipation has concern because most of the time SRAM stays in standby mode and compared to switching time. However dynamic power dissipation cannot be neglected, it can be minimized with the scaling of voltage supply due to the square law dependency of digital circuit active power. Thus it requires the scaling of threshold voltage to maintain the performance but low threshold voltage introduces high leakage currents such as sub threshold leakage current due to shorter channel length. In

addition, the scaling of supply voltage and threshold voltage will cause instability of the SRAM cell for nanometer technology nodes [2].

SRAM design in planar MOSFET is challenging in deep submicron technology due to short channel effect (SCE), layout dependent effect (LDE) and high leakage current. The thinning of gate oxides result in higher gate leakage and causing gate induced drain leakage (GIDL) [3]. FinFET device architecture is a promising candidate to replace MOSFET in SRAM design for improved scalability. FinFET offer lower gate leakage and sub-threshold leakage due to two electrically coupled gates and the thin silicon body which suppress the short channel effects [2]. Moreover it enhances gate controllability over the channel allowing thicker gate oxide which can reduce the gate leakage significantly [2]. Moreover, FinFET has a lower process variation compared to planar MOSFET as FinFET has minimum random dopant fluctuations (RDF) due to the lightly body doping [4].

1.2 Problem Statement

Planar MOSFET scaling could not continue forever with Moore's law, planar structure in nanometer range introduced a lot of degradation effects and deep submicron effect to the device such as short channel length effect. Aggressive scaling in MOSFET result in higher leakage current and sensitive to process variation. FinFET architecture is chosen as promising candidate due to its lower leakage current and better scalability and higher I_{on}/I_{off} ratio [5].

SRAM arrays greatly contribute to overall VLSI design thus power consumption is always a concern for SRAM especially standby power as it is having the behavior of short active periods but long idle periods [1]

In common gate FinFET, two gates are biased together to switch the FinFET on or off. Thus this gives no flexibility control over the gate bias. However, independent gate FinFET provides independent biasing on gate with one gate used to switch the FinFET on and off and the other gate used to determine the threshold voltage to minimize the leakage. The back gate operation mode offer the flexibility to tune the static and dynamic performance characteristic. The only drawback of independent gate finFET is having lower drive current strength compared to common gate FinFET.

It is clear that SRAM in planar bulk MOSFET is not a solution in future anymore and FinFET is a good candidate to address its weakness. In addition, the intention of this proposal is to combine both advantage of common gate and independent gate FinFET into one model for SRAM design. This model is consists of parallel common gate FinFET with source and drain connected but having two gates to enable independent gate biasing. Each of the common gate FinFET is having half dimension to compensate the area penalty imposed.

1.3 Objectives

The study of Static Random Access Memory (SRAM) circuitry by using independent gate controllable technique on common gate FinFET. The objectives are:

- To develop a simple subckt model in order to enable the behavior of independent gate control
- To explore the technique of independent gate controllable technique on SRAM
- To evaluate the performance and standby leakage on proposed technique benchmarking with conventional SRAM FinFET structure.

1.4 Research Scope

The scope of study includes the literature review of SRAM circuitry on FinFET device and fundamental of SRAM operation is studied. Common gate FinFET device has been commercialize widely and FinFET based SRAM design has becoming popular practice, thus comparison with conventional common gate FinFET SRAM is carried out.

In this research, independent controllable gate structure on common gate FinFET is proposed. The proposed approach is to minimize the leakage current and boost up the performance of SRAM. Performance of SRAM with this new technique is evaluated and compared with conventional common gate FinFET SRAM.

The research also includes the investigation on the behaviour, advantages and disadvantages on this technique. Various aspect like power, performance and area are discussed.

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