NETWORK-ON-CHIP FLOORPLANNING AND APPLICATION MAPPING USING CROSS-ENTROPY METHOD

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To my beloved father, mother and sister.

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ABSTRACT

The increase in number of on-chip components (IP core) integration on System on Chip (SoC) has caused the communication of on-chip components (IP core) to hit the bottleneck of communication due to bandwidth limitation of buses. Network-on-Chip (NoC) is introduced to solve the communication bandwidth problem and it is widely used in System-on-Chip (SoC) nowadays to enable the communication between on-chip components through routers and network channel within the chip so that the complexity of communication between on-chip components can be reduced by reducing number of wire used which can lead to huge saving in chip area and reducing dynamic power significantly. The performance of Network-on-Chip (NoC) is highly dependence on floorplanning methodology used which can improve performance (transfer rate) of Network-on-Chip (NoC) blocks while meeting communication requirements and achieving minimal area overhead. The Cross-Entropy (CE) method has been applied successfully by researcher in various optimization problems and able to produce promising results. Therefore, the Cross-Entropy (CE) Method is introduced to solve optimization problems for Network on Chip (NoC) floorplanning and application mapping. The Cross-Entropy (CE) method is used to generate optimal floorplan with optimal communication cost for various multimedia benchmark applications. Evaluation results show that the Cross-Entropy (CE) method is able to produce comparable results compared to other selected methods from published journal papers and has faster convergence in terms of iteration/generation when compared to GA with heuristic crossover and random initial mapping.

ABSTRAK

Peningkatan dalam bilangan atas cip komponen (teras IP) integrasi Sistem pada Chip (SoC) menyebabkan komunikasi komponen atas cip (teras IP) megalami kesesakan komunikasi kerana had jalur lebar bas. Rangkaian pada cip (NOC) yang diperkenalkan untuk menyelesaikan masalah lebar jalur komunikasi dan ia digunakan secara meluas dalam Sistem pada Chip (SoC) hari ini untuk membolehkan komunikasi antara komponen atas cip melalui router dan saluran rangkaian dalam cip supaya kerumitan komunikasi antara komponen atas cip boleh dikurangkan dengan mengurangkan beberapa wayar yang digunakan yang boleh membawa kepada penjimatan kos yang besar di kawasan cip dan mengurangkan kuasa dinamik dengan ketara. Prestasi Rangkaian pada cip (NOC) adalah sangat bergantung kepada metodologi floorplanning digunakan yang boleh meningkatkan prestasi (kelajuan pemindahan) blok rangkaian pada cip (NOC) di samping memenuhi keperluan komunikasi dan mencapai overhed kawasan yang minimum. Kaedah Cross-Entropy (CE) telah digunakan dengan berjayanya oleh penyelidik dalam pelbagai masalah pengoptimuman dan dapat menghasilkan kejayaan awal. Oleh itu, Kaedah Cross-Entropy (CE) diperkenalkan untuk menyelesaikan masalah pengoptimuman untuk rangkaian pada cip (NOC) floorplanning dan aplikasi pemetaan. Kaedah Cross-Entropy (CE) yang digunakan untuk menghasilkan Pelan Lantai optimum dengan kos komunikasi yang optimum untuk pelbagai aplikasi penanda aras multimedia. Keputusan penilaian menunjukkan bahawa kaedah Cross-Entropy (CE) mampu menghasilkan keputusan yang setanding berbanding dengan kaedah lain dipilih dari kertas jurnal yang diterbitkan dan mempunyai penumpuan yang lebih cepat dari segi lelaran / generasi berbanding Genetic Algorithm (GA) dengan crossover heuristik dan pemetaan awal rawak.

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LIST OF ABBREVIATIONS

SoC	-	System-on-Chip
NoC	-	Network-on-Chip
IC	-	Integrated Circuit
IP	-	Intellectual Property
VLSI	-	Very-large-scale integration
PE	-	Processing Element
TDG	-	Traffic Distribution Graph
TDM	-	Traffic Distribution Matrix
BSG	-	Bounded Slicing Grid Structure
NP-hard	-	Non-deterministic Polynomial-time hard
CBL	-	Corner Block List
GA	-	Genetic Algorithm
PSO	-	Particle Swarm Optimization
DPSO	-	Discrete Particle Swarm Optimization
ILP	-	Integer Linear Programming
ACO	-	Ant Colony Optimization
SA	-	Simulated Annealing
CE	-	Cross-Entropy
MWD	-	Multiwindow Display
VOPD	-	Video Object Plane Decoder
NP_GA	-	Genetic Algorithm with Network Partitioning
NMAP	-	Fast algorithm for mapping IP cores onto mesh floorplan
PSMAP	-	Meta-heuristic strategy using Particle Swarm Optimization technique

LIST OF SYMBOLS

α	-	Smoothing parameter
ρ	-	Rarity parameter

CHAPTER 1

INTRODUCTION

1.1 Motivation of Research

Performance, power and area are three areas of focus of System-on-Chips (SoCs) design nowadays. Network-on-Chip (NoC) plays an important role in balancing and achieving these aggressive three critical key targets. The performance of NoC is highly dependence on floorplanning methodology used as the placement of NoC core and routers may impact the data transfer rate and area overhead of the chip. Optimal NoC floorplan can help to improve performance (transfer rate) of NoC while meeting communication requirements and achieving minimal area overhead. Besides this, optimal NoC floorplan can help to achieve low power while meeting performance and area requirements.

1.2 Problem Statement

Heuristic optimization method has been used to solve application mapping and floorplanning problem due to large NoC mapping search space. Simulated Annealing (SA) and other heuristic optimization methods such as Genetic Algorithm (GA) and adaptive search techniques can be trapped in local minimum. Reference [1] shows that the Cross-Entropy (CE) method has fast convergence and is less susceptible trapped in a local minimum as Cross-Entropy (CE) method is a global search method.

1.3 Objectives

The main objectives of this project are:

1. To propose Network-on-Chip (NoC) floorplanning and application mapping based on Traffic Distribution Graph (TDG) using the Cross-Entropy (CE) method.
2. To find the optimal source-to-destination communication path through routers for each communication path in Traffic Distribution Graph (TDG) given.

1.4 Scope of Work

The main focus of this project is to develop MATLAB program based on the Cross-Entropy (CE) method that can:

1. Generate random NoC mapping sequences based on given Traffic Distribution Graph (TDG).
2. Find optimal NoC floorplan/mapping sequence with the lowest communication cost.

1.5 Report Organization

This report is divided into 5 chapters:

1. Chapter 1 discusses about the motivation of research, problem statement, objective, scope of work and report organization.
2. Chapter 2 summarizes literature reviews on the floorplan representation models, NoC architecture and NoC application mapping and floorplanning. Various NoC application mapping and floorplanning techniques/methods are discussed. A brief introduction of the Cross-Entropy (CE) method, smoothed probabilities updating equation, the main Cross-Entropy (CE) Algorithm for Optimization and Node Transition Algorithm (Fast Trajectories Generation Algorithm) are discussed at the end of this chapter.

3. Chapter 3 discusses about the NoC floorplanning and application mapping, communication cost, node transition matrix and how solution can be represented.

4. Chapter 4 shows CE generated floorplans for each of the multimedia benchmark applications. Optimal floorplans with optimal communication cost generated using the Cross-Entropy (CE) method are then compared with floorplans generated using selected methods in term of communication cost and convergence speed in terms of iteration/generation. Besides this, the relationship between parameter is also discussed at the end of this chapter.

5. Chapter 5 summarizes all the findings of this project and discusses briefly about future works recommendations for future researchers that plan to do research on NoC floorplanning and application mapping.

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