

FINFET BASED DESIGN OF XOR AND XNOR USING HSPICE

CHEAH HUI FUEN

UNIVERSITI TEKNOLOGI MALAYSIA

FINFET BASED DESIGN OF XOR AND XNOR USING HSPICE

CHEAH HUI FUEN

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical - Computer and Microelectronic System)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JUNE 2015

Specially dedicated to my beloved family, lecturers and friends
For the guidance, encouragement and inspiration
Throughout my journey of education

ACKNOWLEDGEMENT

First, I would like to take this opportunity to express my deepest gratitude to my project supervisor Ir. Dr. Michael Tan Loong Peng, for his kind teaching and guidance. He has been very helpful with the setup of software needed to simulate, and has been guiding me to the right path ever since. I sincerely thank him for his supports.

In addition, I wish to thank my postgraduate course-mates for their cooperation and information sharing in completing this project. Yet, not to forget my fellow friends for their care and moral support when it was most required.

Furthermore, I would like to thank my friends for their encouragement and support. They had gave me useful opinion and assistance. Last but not the least; I am very thankful for my family members for their spiritual and financial support.

ABSTRACT

XOR and XNOR are popular gates in microprocessors. They are fundamental unit circuits used in adder, multiplexer, comparator, parity checker and generator circuits. This project proposes a new five transistors XOR-XNOR design using FinFET. The use of conventional MOSFET as basic unit of XOR and XNOR design has reached its performance limit due to short channel effects (SCEs) at nanoscale region. International Technology Roadmap for Semiconductors (ITRS) had proposed FinFET to replace conventional MOSFET to overcome the limitations of MOSFET at nanoscale region. Impact of variation FinFET parameters such as gate length, fin height and fin thickness to performance of proposed design are analyzed. In this project, the proposed design is compared with other existing designs in terms of power, delay, power delay product (PDP) and energy delay product (EDP). Simulation results demonstrate the power, delay, PDP and EDP at different supply voltage range from 0.6V to 1.2V using HSPICE alongside with CosmosScope. The simulation results reveal that the proposed design has full output swing with all input combinations. It consumes least power compared to existing designs and has low PDP and EDP. This project also compare the performance between SG FinFET and IG FinFET based designs. IG FinFET based design consumes lesser power but bigger delay. Thus, higher PDP and EDP compared to SG FinFET based design.

ABSTRAK

XOR dan XNOR adalah get popular di mikropemproses. Mereka adalah unit asas yang digunakan dalam penambah, pemultipleks, comparator, penyemak pariti dan penjana litar. Projek ini mencadangkan lima transistor reka bentuk XOR-XNOR menggunakan FinFET. Penggunaan MOSFET konvensional sebagai unit asas XOR dan XNOR reka bentuk telah mencapai had prestasinya kerana kesan saluran pendek (SCE) di rantau skala nano. *International Technology Roadmap for Semiconductors* (ITRS) telah mencadangkan FinFET untuk menggantikan MOSFET konvensional untuk mengatasi batasan MOSFET di rantau skala nano. Kesan perubahan parameter FinFET kepada prestasi reka bentuk yang dicadangkan dianalisis. Dalam projek ini, reka bentuk yang dicadangkan itu berbanding dengan reka bentuk yang lain yang sedia ada dari segi kuasa, kelewatan, produk kelewatan kuasa (PDP) dan product kelewatan tenaga (EDP). Keputusan simulasi menunjukkan kuasa, kelewatan, PDP dan EDP pada jarak voltan bekalan yang berbeza daripada 0.6V hingga 1.2V menggunakan HSPICE bersama-sama dengan CosmosScope. Keputusan simulasi menunjukkan bahawa reka bentuk yang dicadangkan mempunyai swing output penuh dengan semua kombinasi input. Ia menggunakan kurangnya *power* berbanding dengan reka bentuk yang sedia ada dan mempunyai PDP dan EDP yang rendah. Projek ini juga membandingkan prestasi antara reka bentuk berasaskan *SG FinFET* dan reka bentuk berasaskan *IG FinFET*. Reka bentuk berasaskan *IG FinFET* menggunakan *power* yang lebih kurang tetapi *delay* yang lebih besar. Dengan itu lebih banyak PDP dan EDP berbanding dengan reka bentuk berasaskan *SG FinFET*.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	x
	LIST OF FIGURES	xi
	LIST OF ABBREVIATIONS	xv
	LIST OF APPENDICES	xvii
1	INTRODUCTION	1
	1.1 Introduction	1
	1.2 Background of Study	2
	1.3 Problem Statement	4
	1.4 Objectives	4
	1.5 Scope of Work	5
2	LITERATURE REVIEW	6
	2.1 FinFET Overview	6
	2.2 Shorted Gate FinFET and Independent Gate FinFET	9
	2.3 SOI vs Bulk FinFET	10
	2.4 XOR and XNOR Design	13
	2.4.1 CMOS XOR-XNOR	14
	2.4.2 Inverter Based XOR-XNOR	14

	2.4.3	DCVSL Based XOR-XNOR	15
	2.4.4	10T Transmission Gate Based XOR-XNOR	16
	2.4.5	6T XOR-XNOR	16
	2.4.6	10T XOR-XNOR	17
	2.4.7	8T XOR-XNOR	18
	2.4.8	10T XOR-XNOR with Single Feedback Network	18
	2.4.9	10T XOR-XNOR with Single Feedback Network	19
	2.4.10	Energy Recovery XOR-XNOR	20
	2.4.11	Concurrent Error Detection Based Fault Tolerant XOR-XNOR	20
	2.4.12	6T FinFET Based XOR-XNOR	21
3		RESERCH METHODOLOGY	22
	3.1	Introduction	22
	3.2	BSIM-CMG Model	24
	3.3	HSPICE	25
	3.4	CosmosScope	25
	3.5	Gantt Chart	26
	3.6	Technique to Obtain Optimizing Parameter	27
4		RESULTS AND DISCUSSION	29
	4.1	I-V Curve	29
	4.2	Proposed Design	31
	4.3	Impact of Variation FinFET Parameters to Circuit Performance	34
	4.3.1	Gate Length Variation	34
	4.3.2	Fin Height Variation	39
	4.3.3	Fin Thickness Variation	44
	4.4	Comparison with Existing Designs	49

4.5	Comparison between SG FinFET and IG FinFET Based Designs	53
5	CONCLUSION AND FUTURE WORK	58
5.1	Conclusion	58
5.2	Future Work	59
	REFERENCES	60
	Appendices A-C	63

LIST OF TABLES

TABLE NO.	TITLE	PAGE
1.1	Truth table of XOR and XNOR [2]	2
2.1	Fabrication steps for bulk and SOI FinFETs [17]	13
2.2	Variability of fin height and fin width for bulk and SOI FinFETs [17]	13
3.1	Gantt chart for first semester	26
3.2	Gantt chart for second semester	26
4.1	Summary of device characteristic	30
4.2	Summarized operation of circuit	32
4.3	Summary of FinFET parameters of the circuit	32
4.4	Summary of circuit performance at different supply voltage	33
4.5	Summary of circuit performance at different L_g	34
4.6	Summary of circuit performance at different H	39
4.7	Summary of circuit performance at different H	44
4.8	Summary of circuit performance	54

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
1.1	Symbol and logic operation of XOR and XNOR [2]	1
1.2	Moore's law [3]	2
1.3	ITRS showing MuG-FET is at current trend [5]	3
2.1	Basic structure of FinFET [6]	6
2.2	Intel's Tri-Gate transistors shows similarity to FinFET [8]	7
2.3	Sub-threshold leakage current and gate delay of planar and Tri-Gate transistors [8]	8
2.4	FinFET with multiple fins per finger structure [8]	8
2.5	FinFET with key parameters labelled [13]	9
2.6	SG FinFET and IG FinFET [13]	10
2.7	2-D cross-section along transistor gate of bulk and SOI FinFET [16]	10
2.8	DIBL vs gate length for bulk and SOI FinFETs [17]	11
2.9	Leakage current comparison between bulk and SOI FinFETs [17]	11
2.10	Delay vs fin height of bulk and SOI FinFETs [17]	12
2.11	CMOS XOR-XNOR [18]	14

2.12	Inverter based XOR-XNOR [19]	15
2.13	DCVSL based XOR-XNOR [20]	15
2.14	10T transmission gate based XOR-XNOR [21]	16
2.15	6T XOR-XNOR [21]	17
2.16	10-T XOR-XNOR [22]	17
2.17	8-T XOR-XNOR [23]	18
2.18	10-T XOR-XNOR with single feedback network [24]	19
2.19	10-T XOR-XNOR with dual feedback network [24]	19
2.20	Energy recovery XOR-XNOR [25]	20
2.21	CED based XOR-XNOR [26]	21
2.22	6T FinFET based XOR-XNOR [27]	21
3.1	Research methodology flowchart	23
3.2	Varieties of BSIM-CMG model [28]	24
3.3	Optimizing flow to obtain optimized parameters	28
4.1	NMOS I-V curve	29
4.2	PMOS I-V curve	30
4.3	Schematic of proposed XOR-XNOR design	31
4.4	Transient analysis of 5T XOR-XNOR at V _{dd} =1.0V	33
4.5	Power at different L _g	35

4.6	XOR delay at different Lg	36
4.7	XNOR delay at different Lg	36
4.8	XOR PDP at different Lg	37
4.9	XNOR PDP at different Lg	37
4.10	XOR EDP at different Lg	38
4.11	XNOR EDP at different Lg	38
4.12	Power at different H	40
4.13	XOR delay at different H	41
4.14	XNOR delay at different H	41
4.15	XOR PDP at different H	42
4.16	XNOR PDP at different H	42
4.17	XOR EDP at different H	43
4.18	XNOR EDP at different H	43
4.19	Power at different T	45
4.20	XOR delay at different T	46
4.21	XNOR delay at different T	46
4.22	XOR PDP at different T	47
4.23	XNOR PDP at different T	47
4.24	XOR EDP at different T	48
4.25	XNOR EDP at different T	48

4.26	Power of different designs	49
4.27	XOR delay of different designs	50
4.28	XNOR delay of different designs	50
4.29	XOR PDP of different designs	51
4.30	XNOR PDP of different designs	51
4.31	XOR EDP of different designs	52
4.32	XNOR EDP of different designs	52
4.33	The proposed circuit using IG FinFET	53
4.34	Power of SG FinFET and IG FinFET based circuit	54
4.35	XOR delay of SG FinFET and IG FinFET based circuit	55
4.36	XNOR delay of SG FinFET and IG FinFET based circuit	55
4.37	XOR PDP of SG FinFET and IG FinFET based circuit	56
4.38	XNOR PDP of SG FinFET and IG FinFET based circuit	56
4.39	XOR EDP of SG FinFET and IG FinFET based circuit	57
4.40	XNOR EDP of SG FinFET and IG FinFET based circuit	57

LIST OF ABBREVIATIONS

VLSI	-	Very large-scale integrated
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect Transistor
GIDL	-	Gate-Induced Drain Leakage
SCE	-	Short Channel Effect
ITRS	-	International Technology Roadmap for Semiconductors
MuG-FET	-	Multigate FET
PDP	-	Power Delay Product
EDP	-	Energy Delay Product
T	-	Fin Thickness
H	-	Fin Height
W	-	Width
L	-	Gate Length
IG FinFET	-	Independent Gate Fin-shaped Field Effect Transistor
SG	-	Shorted Gate Fin-shaped Field Effect Transistor
FinFET		
SOI	-	Silicon-On-Insulator
DIBL	-	Drain-Induced Barrier Lowering
CMOS	-	Complementary MOS
PTL	-	Pass Transistor Logic
TG	-	Transmission Gate
PMOS	-	P-Channel MOSFET
NMOS	-	N-Channel MOSFET
V _{dd}	-	Supply Voltage
G _{nd}	-	Ground
DCVSL	-	Differential Cascade Voltage Switch Logic
CED	-	Concurrent Error Detect

BSIM-	-	Berkeley's Short-channel IGFET Model-Common Multi Gate
CMG		FETs
R_{out}	-	Output resistance
V_{DS}	-	Drain-source voltage

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	Proposed 5T XOR-XNOR HSPICE Netlist	64
B	PMOS IV Characteristic HSPICE Netlist	65
C	PMOS IV Characteristic HSPICE Netlist	66

CHAPTER 1

INTRODUCTION

1.1 Introduction

XOR stands for exclusive-OR, acts in the same way as the logical “either/or”. The output is “true” if either, but not both of the inputs are “true”. The output is “false” if both inputs are the same. XNOR stands for exclusive-NOR, is a combination of XOR gate followed by an inverter. The output is “true” if both of the inputs are the same and false if both of the inputs are different [1]. Figure 1.1 shows the XOR and XNOR symbols and logic operations. Table 1.1 shows the truth table of XOR and XNOR.

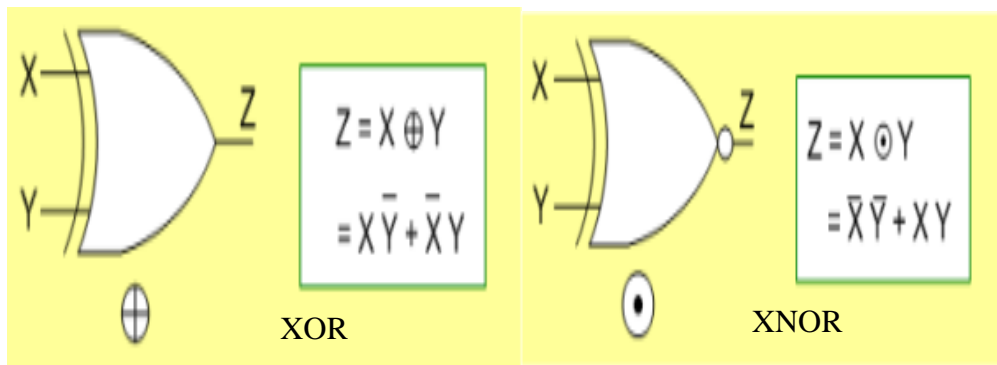


Figure 1.1 Symbol and logic operation of XOR and XNOR [2]

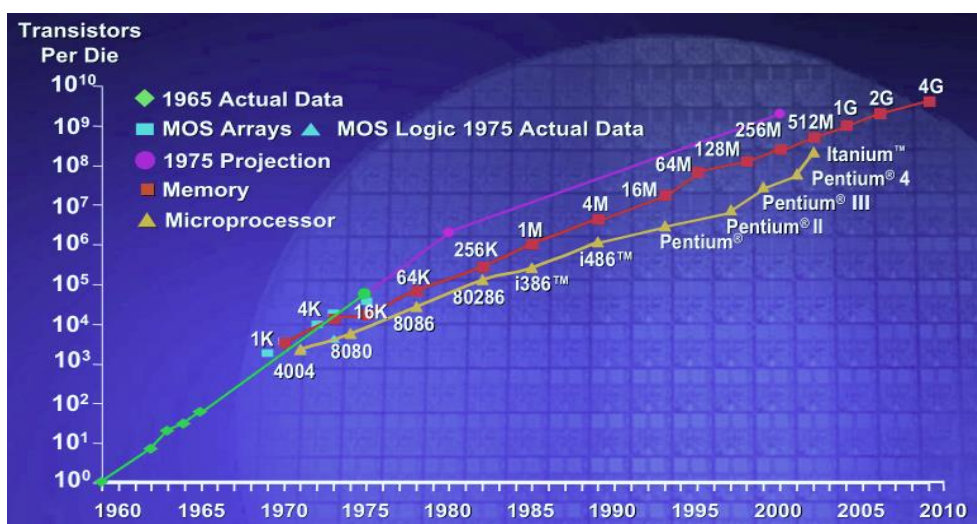
Table 1.1 : Truth table of XOR and XNOR [2]

X	Y	Z (XOR)	Z (XNOR)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

XOR and XNOR are the sub-circuits mostly used in arithmetic circuits, such as full adder and multiplexer. They also play important roles in designing parity checker and generator circuits. Optimized design of XOR and XNOR circuit can benefit the performance of larger number of circuits that they are part of.

1.2 Background of Study

According to Moore's law, the number of transistors that can be fabricated on a very large-scale integrated (VLSI) chip doubles every two years [3]. Moore's law shown in Figure 1.2.

**Figure 1.2** Moore's law [3]

The scaling of transistor aim at increasing operation speed, reduction in space usage and better control on the channel by gate configuration. The downscaling of MOSFET is based on Moore’s Law finally reaches nanoscale which faces severe challenges such as gate-leakage current, Gate-Induced Drain Leakage (GIDL), off-state leakage current, power dissipation and short channel effects (SCEs) are prevalent. These challenges are unavoidable as the size of transistor is the most important parameter to be considered by design engineers in the scaling process [4].

Figure 1.3 shows the International Technology Roadmap for Semiconductors (ITRS). It’s observed that Multigate FET (MuG-FET), which is FinFET family, is at current trend [5]. FinFET is an alternative of conventional MOSFET to overcome limitation of MOSFET at nanoscale region.

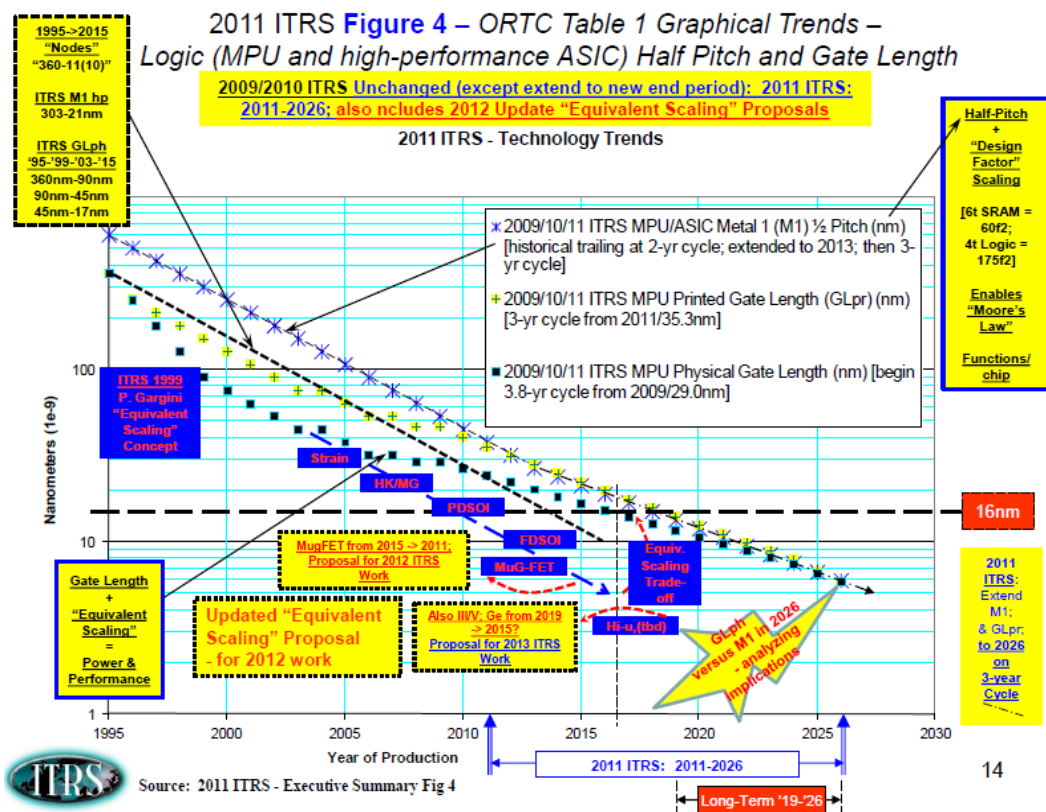


Figure 1.3 ITRS showing MuG-FET is at current trend [5]

1.3 Problem Statement

XOR and XNOR are popular gates in microprocessors. They are fundamental unit circuits used in adder, multiplexer, comparator, parity checker and generator circuits. Optimized design of XOR and XNOR circuit enhances the circuit performance. Hence, a XOR-XNOR that has low power consumption, low delay in critical path and energy efficient is in demand.

The downscaling of conventional MOSFET faces severe challenges such as gate-leakage current, Gate-Induced Drain Leakage (GIDL) and off-state leakage current beyond 32nm node due to short channel effect control and suppression of device performance variability. Thus, the use of conventional MOSFET as basic unit of XOR and XNOR design has reached its performance limit. The International Technology Roadmap of Semiconductor (ITRS) had proposed FinFET to replace conventional MOSFET to overcome the problem in 2006. Therefore, FinFET is used as the basic unit of XOR and XNOR design in this project. The performance of FinFET based XOR-XNOR design are explored.

1.4 Objective

The focus of this study is on the development of FinFET device and implementation of various XOR-XNOR designs where the performance are analyzed. The following are the objectives of this study:

1. To propose a low power FinFET based XOR and XNOR design.
2. To investigate impact of variation of FinFET parameters such as fin height, gate length and fin thickness on XOR and XNOR performance.
3. To analyze the performance of proposed circuit in terms and of power, delay, power delay product (PDP) and energy delay product (EDP) and compare with existing circuits.

1.5 Scope of Work

The scope of study is to clearly define the specific field of the research and ensure that entire content of this project is confined within the scope. The project scope are as below:

1. Literature review of XOR and XNOR designs and FinFET device is carried out.
2. FinFET modelling using BSIM-CMG model.
3. HSPICE is used alongside CosmosScope to perform circuit simulation. The circuit simulator will be used to investigate power, delay, delay product (PDP) and energy delay product (EDP) of the designs.
4. Performance impact with variation of FinFET parameters.
5. Analysis and comparison between performance of proposed design and existing designs in terms of power, delay, delay product (PDP) and energy delay product (EDP).
6. Analysis and comparison between performance of using SG FinFET and IG FinFET.

REFERENCES

1. What is logic gate (AND, OR, XOR, NOT, NAND, NOR, and XNOR). Available: <http://whatis.techtarget.com/definition/logic-gate-AND-OR-XOR-NOT-NAND-NOR-and-XNOR>, 2014.
2. XOR-XNOR Gates. Available: http://www.ccse.kfupm.edu.sa/~amin/eCOE200/Lesson2_7.pdf, 2014.
3. Computer Measurement Group, (May 2007). "Moore's Law: More or Less?" Available: http://www.cmg.org/measureit/issues/mit41/m_41_2.html, 2014.
4. International Technology Roadmap for Semiconductor (ITRS). Available: www.itrs.net/Links/2006update/2006updatefinal.htm, 2014.
5. International Technology Roadmap for Semiconductors. Available: <http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf>, 2014.
6. BSIM-CMG. Available: <http://www-device.eecs.berkeley.edu/bsim/?page=BSIMCMG>, 2014.
7. Hisamoto, D., et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm", IEEE Trans. Electron Devices, pp. 2320- 2325, Dec 2000.
8. David Kanter, "Intel's 22nm Tri-Gate Transistors". Available: <http://www.realworldtech.com/intel-22nm-finfet/>, 2011.
9. Mahender Veshala, Ramchander Jatooth, Kota Rajesh Reddy, "Reduction of Short-Channel Effects in FinFET", Issn: 2277-3754, vol. 2, issue 9, 9 March 2013.
10. Jamil Kawa, Andy Biddle, "FinFETs Herald A Seismic Shift in Semiconductor Technology". Available: <http://electronicdesign.com/digital-ics/finfets-herald-seismic-shift-semiconductor-technology>, Jan 2013
11. Haiying Zhao, "Introduction to FinFET". Available: http://newport.eecs.uci.edu/~rnelson/files-2008/Student_Presentations/Intro_to_FinFet.ppt, 2013
12. Debajit Bhattacharya and Niraj K. Jha, "FinFETs: From Devices to Architectures", Advances In Electronics, VOL. 2014.

13. Prateek Mishra, Anish Muttreja, and Niraj K. Jha, “FinFET Circuit Design”, Nanoelectronic Circuit Design, 2011.
14. Michael C. Wang, “Independent-Gate FinFET Circuit Design Methodology”, IJCS, 2010.
15. Terence Hook, “FinFET Isolation: Bulk vs. SOI”. Available: <http://semimd.com/hars/2013/05/15/guest-blog-by-ibm-finfet-isolation-%E2%80%93-bulk-vs-soi/>, 2014.
16. Mirko Poljak, Vladimir Jovanović and Tomislav Suligo, “SOI vs. Bulk FinFET: Body Doping and Current Effects Influence on Device Characteristic”, Electrotechnical Conference, 2008. MELECON 2008.
17. David Fried, Thomas Hoffmann, Bich-Yen Nguyen, and Horacio Mendez, “Comparison Study of FinFETs: SOI vs. Bulk”, SOI Industry Consortium, 2009.
18. Sung-Mo Kang, Y. Leblibici, “CMOS Digital Integrated Circuits: Analysis and Design”, Addition-Tata McGraw Hill, (2003).
19. H. Lee and G. E. Sobelman, “New Low-voltage Circuits for XOR and XNOR”, in Proc. IEEE Southeastcon, Apr. 12-14, pp. 225-229(1997).
20. J.Rabaey, “Digital Integrated Circuits (A Design Prospective)”, Prentice-Hall, Englewood Cliffs, NJ, (1996).
21. D. Radhakrishnan, “Low-voltage Low-power CMOS Full Adder,” IEE Proceedings of Circuits Devices Systems, VOL. 148, NO. 1, FEB, 2001.
22. S. W. Shiv Shankar Mishra, R.K. Nagaria, and S. Tiwari, “ New Design Methodologies for High Speed Low Power XOR-XNOR Circuits”, World Academy of Science, Engineering and Technology, 2009.
23. S. Goel, M. A. Elgamel, and M. A. Bayoumi, “Design Methodologies for High-Performance NoiseTolerant XOR-XNOR circuits”, IEEE Trans. Circuits Syst. –I, Reg. Papers, VOL. 53, NO. 4, pp. 867 – 878, APRIL, 2006.
24. S. Goel, M. A. Elgamel, and M. A. Bayoumi, “Novel Design Methodology for High-Performance XOR-XNOR Circuit Design”, in Proc. Symp. Integr. Circuits Syst. Design (SBCCI 2003), Sep. 2003, pp. 71-76.
25. Y. Xu and A. Srivastava, “New Energy Recovery CMOS XNOR/XOR Gates”, IEEE, 2007.
26. Mouna Karmani, Chiraz Khedhiri, Belgacem Hamdi, Ka Lok Man, Eng Gee Lim, and Chi-Un Lei, “A Concurrent Error Detection Based Fault-Tolerant 32nm XOR-XNOR Circuit Implementation”, IMECS, 2012.

27. Neha Yadav, Saurabh Khandelwal, and Shyam Akashe, "Analysis of Conventional CMOS and FinFET based 6-T XOR- XNOR circuit at 45nm Technology", International Journal of Computer Applications, VOL. 84, NO. 4, DECEMBER 2013.
28. Navid P. and et.al. *BSIM-SPICE Models Enable FinFET and UTB IC Designs*. 2013 Access, IEEE. Pages: 201-215