FINFET BASED DESIGN OF XOR AND XNOR USING HSPICE

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Specially dedicated to my beloved family, lecturers and friends

For the guidance, encouragement and inspiration

Throughout my journey of education

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ABSTRACT

XOR and XNOR are popular gates in microprocessors. They are fundamental unit circuits used in adder, multiplexer, comparator, parity checker and generator circuits. This project proposes a new five transistors XOR-XNOR design using FinFET. The use of conventional MOSFET as basic unit of XOR and XNOR design has reached its performance limit due to short channel effects (SCEs) at nanoscale region. International Technology Roadmap for Semiconductors (ITRS) had proposed FinFET to replace conventional MOSFET to overcome the limitations of MOSFET at nanoscale region. Impact of variation FinFET parameters such as gate length, fin height and fin thickness to performance of proposed design are analyzed. In this project, the proposed design is compared with other existing designs in terms of power, delay, power delay product (PDP) and energy delay product (EDP). Simulation results demonstrate the power, delay, PDP and EDP at different supply voltage range from 0.6V to 1.2V using HSPICE alongside with CosmosScope. The simulation results reveal that the proposed design has full output swing with all input combinations. It consumes least power compared to existing designs and has low PDP and EDP. This project also compare the performance between SG FinFET and IG FinFET based designs. IG FinFET based design consumes lesser power but bigger delay. Thus, higher PDP and EDP compared to SG FinFET based design.

ABSTRAK

XOR dan XNOR adalah get popular di mikropemproses. Mereka adalah unit asas yang digunakan dalam penambah, pemultipleks, comparator, penyemak pariti dan penjana litar. Projek ini mencadangkan lima transistor reka bentuk XOR-XNOR menggunakan FinFET. Penggunaan MOSFET konvensional sebagai unit asas XOR dan XNOR reka bentuk telah mencapai had prestasinya kerana kesan saluran pendek (SCE) di rantau skala nano. *International Technology Roadmap for Semiconductors* (ITRS) telah mencadangkan FinFET untuk menggantikan MOSFET konvensional untuk mengatasi batasan MOSFET di rantau skala nano. Kesan perubahan parameter FinFET kepada prestasi reka bentuk yang dicadangkan dianalisis. Dalam projek ini, reka bentuk yang dicadangkan itu berbanding dengan reka bentuk yang lain yang sedia ada dari segi kuasa, kelewatan, produk kelewatan kuasa (PDP) dan produck kelewatan tenaga (EDP). Keputusan simulasi menunjukkan kuasa, kelewatan, PDP dan EDP pada jarak voltan bekalan yang berbeza daripada 0.6V hingga 1.2V menggunakan HSPICE bersama-sama dengan CosmosScope. Keputusan simulasi menunjukkan bahawa reka bentuk yang dicadangkan mempunyai swing output penuh dengan semua kombinasi input. Ia menggunakan kurangnya *power* berbanding dengan reka bentuk yang sedia ada dan mempunyai PDP dan EDP yang rendah. Projek ini juga membandingkan prestasi antara reka bentuk berasaskan *SG FinFET* dan reka bentuk berasaskan *IG FinFET*. Reka bentuk berasaskan *IG FinFET* menggunakan *power* yang lebih kurang tetapi *delay* yang lebih besar. Dengan itu lebih banyak PDP dan EDP berbanding dengan reka bentuk berasaskan *SG FinFET*.

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LIST OF ABBREVIATIONS

VLSI	-	Very large-scale integrated
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect Transistor
GIDL	-	Gate-Induced Drain Leakage
SCE	-	Short Channel Effect
ITRS	-	International Technology Roadmap for Semiconductors
MuG-FET	-	Multigate FET
PDP	-	Power Delay Product
EDP	-	Energy Delay Product
T	-	Fin Thickness
H	-	Fin Height
W	-	Width
L	-	Gate Length
IG FinFET	-	Independent Gate Fin-shaped Field Effect Transistor
SG FinFET	-	Shorted Gate Fin-shaped Field Effect Transistor
SOI	-	Silicon-On-Insulator
DIBL	-	Drain-Induced Barrier Lowering
CMOS	-	Complementary MOS
PTL	-	Pass Transistor Logic
TG	-	Transmission Gate
PMOS	-	P-Channel MOSFET
NMOS	-	N-Channel MOSFET
Vdd	-	Supply Voltage
Gnd	-	Ground
DCVSL	-	Differential Cascade Voltage Switch Logic
CED	-	Concurrent Error Detect

BSIM-CMG	-	Berkeley’s Short-channel IGFET Model-Common Multi Gate FETs
R_{out}	-	Output resistance
V_{DS}	-	Drain-source voltage

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CHAPTER 1

INTRODUCTION

1.1 Introduction

XOR stands for exclusive-OR, acts in the same way as the logical “either/or”. The output is “true” if either, but not both of the inputs are “true”. The output is “false” if both inputs are the same. XNOR stands for exclusive-NOR, is a combination of XOR gate followed by an inverter. The output is “true” if both of the inputs are the same and false if both of the inputs are different [1]. Figure 1.1 shows the XOR and XNOR symbols and logic operations. Table 1.1 shows the truth table of XOR and XNOR.

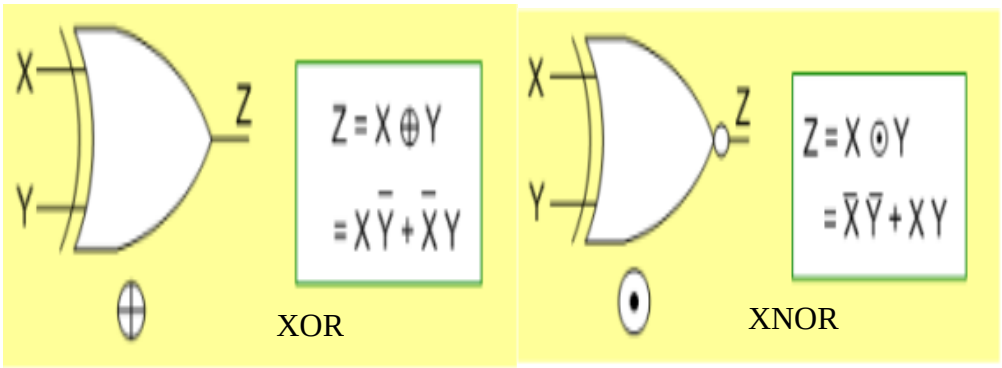

Figure 1.1 Symbol and logic operation of XOR and XNOR [2]

Table 1.1 : Truth table of XOR and XNOR [2]

X	Y	Z (XOR)	Z (XNOR)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

XOR and XNOR are the sub-circuits mostly used in arithmetic circuits, such as full adder and multiplexer. They also play important roles in designing parity checker and generator circuits. Optimized design of XOR and XNOR circuit can benefit the performance of larger number of circuits that they are part of.

1.2 Background of Study

According to Moore's law, the number of transistors that can be fabricated on a very large-scale integrated (VLSI) chip doubles every two years [3]. Moore's law shown in Figure 1.2.

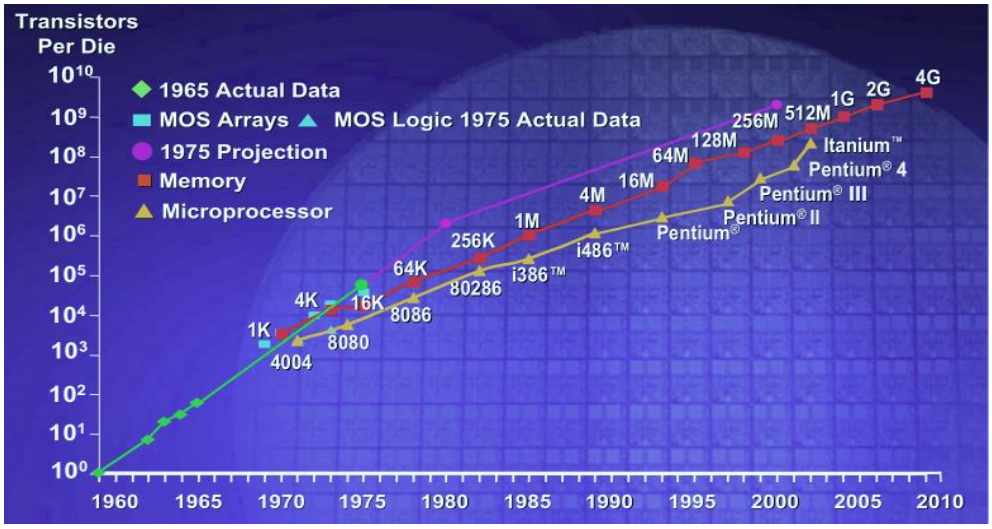

Figure 1.2 Moore's law [3]

The scaling of transistor aim at increasing operation speed, reduction in space usage and better control on the channel by gate configuration. The downscaling of MOSFET is based on Moore's Law finally reaches nanoscale which faces severe challenges such as gate-leakage current, Gate-Induced Drain Leakage (GIDL), off-state leakage current, power dissipation and short channel effects (SCEs) are prevalent. These challenges are unavoidable as the size of transistor is the most important parameter to be considered by design engineers in the scaling process [4].

Figure 1.3 shows the International Technology Roadmap for Semiconductors (ITRS). It's observed that Multigate FET (MuG-FET), which is FinFET family, is at current trend [5]. FinFET is an alternative of conventional MOSFET to overcome limitation of MOSFET at nanoscale region.

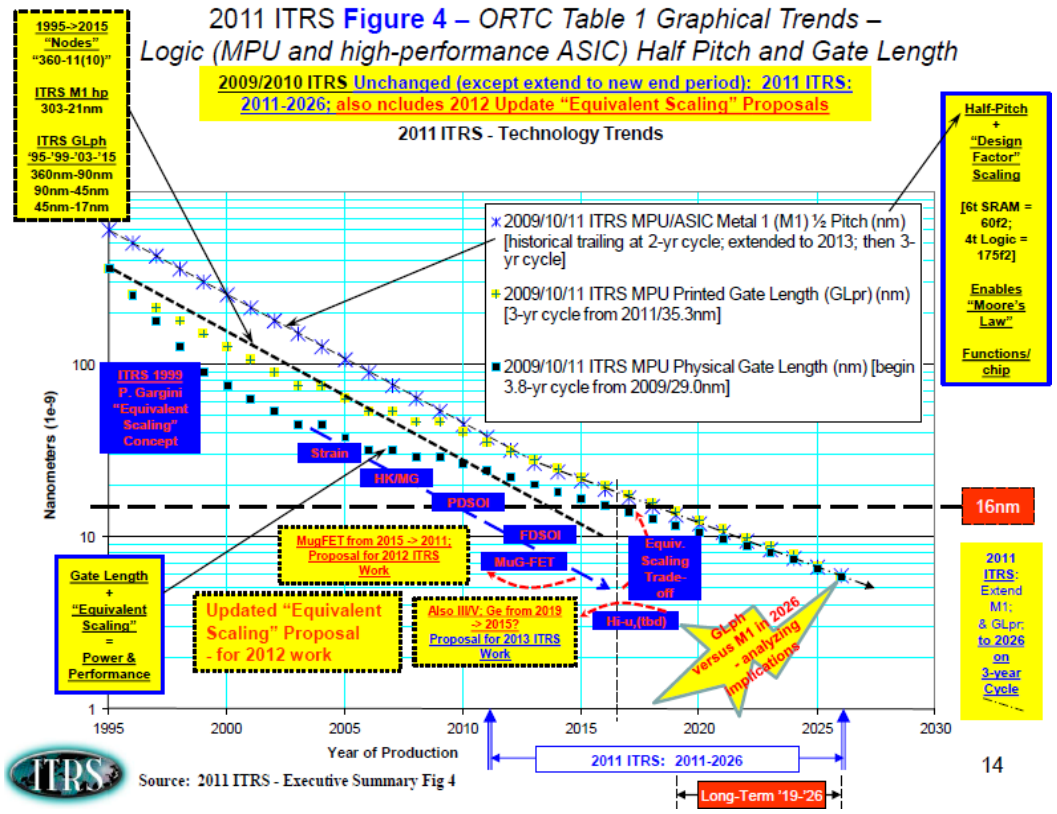

Figure 1.3 ITRS showing MuG-FET is at current trend [5]

1.3 Problem Statement

XOR and XNOR are popular gates in microprocessors. They are fundamental unit circuits used in adder, multiplexer, comparator, parity checker and generator circuits. Optimized design of XOR and XNOR circuit enhances the circuit performance. Hence, a XOR-XNOR that has low power consumption, low delay in critical path and energy efficient is in demand.

The downscaling of conventional MOSFET faces severe challenges such as gate-leakage current, Gate-Induced Drain Leakage (GIDL) and off-state leakage current beyond 32nm node due to short channel effect control and suppression of device performance variability. Thus, the use of conventional MOSFET as basic unit of XOR and XNOR design has reached its performance limit. The International Technology Roadmap of Semiconductor (ITRS) had proposed FinFET to replace conventional MOSFET to overcome the problem in 2006. Therefore, FinFET is used as the basic unit of XOR and XNOR design in this project. The performance of FinFET based XOR-XNOR design are explored.

1.4 Objective

The focus of this study is on the development of FinFET device and implementation of various XOR-XNOR designs where the performance are analyzed. The following are the objectives of this study:

1. To propose a low power FinFET based XOR and XNOR design.
2. To investigate impact of variation of FinFET parameters such as fin height, gate length and fin thickness on XOR and XNOR performance.
3. To analyze the performance of proposed circuit in terms and of power, delay, power delay product (PDP) and energy delay product (EDP) and compare with existing circuits.

1.5 Scope of Work

The scope of study is to clearly define the specific field of the research and ensure that entire content of this project is confined within the scope. The project scope are as below:

1. Literature review of XOR and XNOR designs and FinFET device is carried out.
2. FinFET modelling using BSIM-CMG model.
3. HSPICE is used alongside CosmosScope to perform circuit simulation. The circuit simulator will be used to investigate power, delay, delay product (PDP) and energy delay product (EDP) of the designs.
4. Performance impact with variation of FinFET parameters.
5. Analysis and comparison between performance of proposed design and existing designs in terms of power, delay, delay product (PDP) and energy delay product (EDP).
6. Analysis and comparison between performance of using SG FinFET and IG FinFET.

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