MODELING AND SIMULATION OF GRAPHENE THREE BRANCH JUNCTION USING VERILOG-A

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To my beloved parents,
sister and brother,
for their love and support

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ABSTRACT

Graphene three-branch junction device (G-TBJ) is a non-conventional device that offers promising potential in various application in digital (e.g. logic gates) and analog (frequency mixer, etc) circuit. Operation of G-TBJ can be explained by a capacitor-based equivalent circuit. However, the proposed equivalent circuit neglects other device parameter and properties which can affect the characteristics of G-TBJ. The main objective of this project is to investigate other device model consist of graphene field effect transistor (G-FET). The feasibility of implementing of embedded Verilog-A models to simulate TBJ was assessed. The device simulation is performed using Quite Universal Circuit Simulator (QUCS). First, simulation results of single G-FET is verified against with result measured from fabricated GFET in experiment. Next, simulation is done at TBJ circuit level where two G-FET devices are connected at two terminals. Simulation result shows that model which is proposed and implemented in verilog-A has produced a close result with experiment and simpler device physics formula to describe the operation principle of GFET. Thirdly, TBJ is simulated as inverter. The inverter shows voltage gain of 0.0065 at voltage supply of 0.1V.

ABSTRAK

Graphene tiga cawangan peranti persimpangan (GTBJ) adalah peranti bukan konvensional yang menawarkan potensi yang cerah dalam pelbagai aplikasi dalam digital (contohnya litar logik) dan analog (frekuensi mixer) litar. Operasi GTBJ dapat dijelaskan oleh litar setara berasaskan kapasitor. Walau bagaimanapun, litar setara yang dicadangkan mengabaikan parameter peranti dan parameter lain yang boleh memberi kesan kepada ciri-ciri GTBJ. Objektif utama projek ini adalah untuk menyiasat model peranti lain terdiri daripada graphene kesan medan transistor (GFET). Kemungkinan melaksanakan model Verilog-A untuk mensimulasikan TBJ yang dinilai. Simulasi peranti dilakukan dengan menggunakan Quite universal circuit simulator (QUCS). Pertama, keputusan simulasi tunggal GFET disahkan dengan keputusan diukur mengukur peranti GFET dalam eksperimen. Seterusnya, simulasi dilakukan di peringkat litar TBJ mana dua peranti G-FET disambungkan pada dua terminal. Keputusan simulasi menunjukkan bahawa model yang dicadangkan dan dilaksanakan dengan verilog-A adalah rapat dengan eksperimen dan lebih ringkas untuk formula fizik peranti untuk menggambarkan prinsip pengendalian GFET. Ketiga, TBJ disimulasi sebagai inverter. Inverter tersebut menunjukkan inverter gandaan voltan daripada 0.0065 pada bekalan volt 0.1V.

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LIST OF SYMBOLS

R	-	Resistor
L	-	Length
W	-	Width
V_{th}	-	Threshold Voltage
m	-	Mass
V	-	Voltage
I	-	Current
C	-	Capacitance
g	-	Gate terminal in field effect transistor
d	-	Drain terminal in field effect transistor
s	-	Source terminal in field effect transistor

LIST OF APPPENDICES

CHAPTER 1

INTRODUCTION

Three-branch junction device (TBJ) is a non-conventional device which operates in ballistic transport [1]. The advantages of the TBJ is simple structure, high frequency operation and low power consumption. Demonstration of TBJ has been done using high mobility-semiconductor such Gallium Arsenide, Indium Gallium arsenide, graphene. TBJ can be used in many applications in digital (e.g. logic gates) and analog (frequency mixer, etc) circuit [1].

In this study, possible application of graphene TBJ with well controlled gate voltage is studied in application as logic circuit. Three-branch junctions have been found featuring unique nonlinear electrical characteristics. Nonlinear voltage characteristics or "V" curve have been observed at graphene TBJ dirac point [2].

However, study on graphene-TBJ is quite new and not much on the application of graphene TBJ. MOSFET model equivalent circuit has been proposed for graphene TBJ simulation work. The proposed MOSFET current model is for zero bandgap graphene with backgate voltage controlled structure. In order to control the nonlinear electrical characteristics, critical parameters such as graphene FETs device size, oxide thickness and other key parameters are discussed in this study. The circuit simulation result was presented.

1.1 Objectives

The objective of this research study is to assess the proposed device model for TBJ device. The second objective is to simulate a logic circuit using the proposed circuit model.

1.2 Scope of Work

In this project, MOSFET device model was proposed for graphene three branch junction simulations. Verilog-A modeling language which absorb analog capability was carried out for device modeling activity in this project. Circuit was modeled with QUCS open software.

The non linear electrical characteristics of three branch junctions are looked into. The scope of study mainly focuses on the characterization of transfer characteristics and drain current model at TBJ at dirac point, from the aspects of oxide thickness and device size with different backgate voltage applied. Furthermore, feasibility and performance of the proposed application was investigated.

1.3 Sructure of Project

This project comprises five chapters. The first chapter is the introduction of research. A statement of the objectives and scope of this project is also presented.

The second chapter consists of three parts of literature review. Part one is the basic of graphene including its crystal structure of graphene and electronic characteristics. The next two parts include graphene field effect transistor review and graphene based three branch junction device.

The third chapter deals with methodology and simulation process flow. In chapter four, results and discussion are carried out. The modeling methods and the simulation results as well as drain current versus gate voltage will be presented and analyzed. Lastly, in chapter five, a set of conclusions is presented.

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