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Design of Low Power Integrated CMOS Potentiometric Biosensor for Direct Electronic Detection of DNA Hybridization

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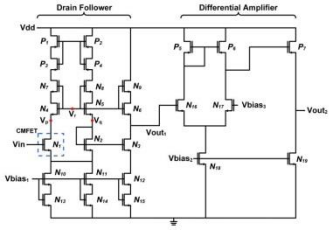
Graphical abstract



Abstract

The purpose of this research is to design a low power integrated complementary metal oxide semiconductor (CMOS) detection circuit for charge-modulated field-effect transistor (CMFET) and it is used for the detection of deoxyribonucleic acid (DNA) hybridization. With the available CMOS technology, it allows the realization of complete systems which integrate the sensing units and transducing elements in the same device. Point-of-care (POC) testing device is a device that allows anyone to operate anywhere and obtain immediate results. One of the important features of POC device is low power consumption because it is normally battery-operated. The power consumption of the proposed integrated CMOS detection circuit requires only 14.87 mW. The detection circuit will amplify the electrical signal that comes from the CMFET to a specified level in order to improve the recording characteristics of the biosensor. Self-cascode topology was used in the drain follower circuit in order to reduce the channel length modulation effect. The proposed detection circuit was designed with 0.18µm Silterra CMOS fabrication process and simulated under Cadence Simulation Tool.

Keywords: Potentiometric; CMFET; DNA; CMOS; low-power

Abstrak

Tujuan penyelidikan ini adalah untuk mereka satu litar pengesan CMOS yang berkuasa rendah untuk CMFET dan digunakan untuk pengesanan penghibridan DNA. Dengan adanya teknologi CMOS, satu sistem lengkap yang terbentuk daripada elemen pengesan dan elemen transduser dapat direalisasikan. Peranti ujian (POC) adalah peranti yang membenarkan pengguna menggunakannya di mana-mana tempat dan mendapat keputusan serta-merta. Salah satu ciri penting yang terdapat pada peranti POC ialah penggunaan kuasa yang rendah kerana biasanya peranti tersebut beroperasi dengan kuasa bateri. Kuasa yang digunakan dalam litar pengesan dalam penyelidikan ini ialah 14.87 mW. Litar pengesan akan menguatkan isyarat elektrik yang dihantar daripada CMFET kepada satu tahap yang tertentu supaya ciri-ciri rakaman biosensor dapat diperbaiki. Topologi *self-cascode* digunakan dalam litar *drain follower* untuk menggurangkan kesan *channel length modulation*. Litar pengesan tersebut direka dengan proses fabrikasi Silterra CMOS 0.18µm dan disimulasi dengan Cadence.

Kata kunci: Potentiometrik; CMFET; DNA; CMOS; kuasa rendah

1.0 INTRODUCTION

Diagnosis of deoxyribonucleic acid (DNA) is significant as it can serve as an early indicator of gene-based diseases like cancers and greatly improves the chances of a cure. There is an increasing number in the demand for gene-based disease testing and paternity testing. Furthermore, the conventional method of DNA detection has relied on labeling of DNA samples and followed by optical readout, a process that can be time-consuming, labor-intensive and expensive. Therefore, the development of a portable gene-based point-of-care testing system has become an important task.

In this research, one of the label-free DNA detection methods is used, which is called potentiometric sensing. The ion-senstive field-effect transistor (ISFET) is the first well-known potentiometric sensor for biological sensing due to its simple and direct detection method.[1] Several novel potentiometric sensors have been proposed in the last decade.[2-5] M. Barbaro[5] proposed a charge-modulated field-effect transistor (CMFET) for DNA detection. CMFET has the advantage of not requiring reference electrode for potentiometric sensing and it is compatible with the standard CMOS process.

Most of the potentiometric sensing of biomolecules researches are focused on the structure of the biosensor but not

the detection circuit.[1-5] Therefore, this research focuses on how to improve the recording characteristic of the potentiometric biosensor by designing the appropriate and efficient detection circuit. Well-designed detection circuit allows the biosensor to be operated with lower noise and power consumption.

2.0 SENSING PRINCIPLE

The DNA biosensor used in this research is based on the potentiometric sensing of DNA molecules. Every double-stranded DNA (ds-DNA) molecule carries $2e^-$ per base pair.[6] The splitting of a ds-DNA will produce two complementary single-stranded DNA (ss-DNA) molecules. If two of the ss-DNAs are complementary to each other, DNA hybridization will occur. Therefore, the DNA hybridization can be detected by measuring the difference in the total charge carried by the DNA molecules.

The potentiometric sensor used in this paper is named as CMFET.[5] The sensor is inspired by the concept of the floating gate MOSFET (FGMOS). FGMOS is usually used as the digital storage in EPROM, EEPROM and flash memories. The main advantage of this type of potentiometric sensor is the avoidance of using any external reference electrode. The cross-sectional view of the CMFET is shown in Figure 1. It consists of a floating gate MOSFET, a control capacitor as the reference electrode and a sensing site to detect the existence of electrical charges. From the modeling and simulation of CMFET[7], it is proved that the floating gate voltage will change linearly with the control gate voltage and the charge density on the sensing site.

The relationship between the floating gate voltage, V_F and net electric charge (total charge of DNA molecules, Q_{DNA} and the electric charge initially trapped in the floating gate, Q_0) on the sensing site is shown in Equation 1. C_C and C_F are the control capacitor and parasitic capacitor in the sensor, respectively. According to Equation 1 and Equation 2, the floating gate voltage will decrease and effective threshold voltage (V_{THF}) will increase when the net charge on the sensing site increases. In this paper, the DNA hybridization event was detected by observing the floating gate voltage of CMFET. A drop in the floating gate voltage indicates DNA hybridization event has occurred.

$$V_F \approx V_C + \frac{Q_{DNA} + Q_0}{C_C + C_F} \quad (1)$$

$$V_{THF} = V_{TH0} - \frac{Q_{DNA} + Q_0}{C_C + C_F} \quad (2)$$

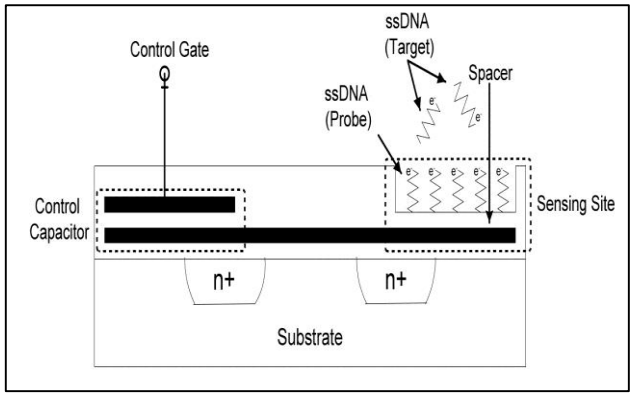


Figure 1 The cross-sectional view of the CMFET

The parameters of the CMFET used in this detection circuit is shown in Table 1. The size of the sensing site is 20 µm x 20 µm. M. Barbaro[7] stated that a CMFET with 40 µm x 40 µm of sensing site has the sensitivity of 54.4 mV/pC. The sensitivity of the CMFET will increase 0.6 mV/pC with every shrinking of 20 µm x 20 µm for the size of the sensing site. Thus, the sensitivity of the sensor is estimated to be around 55 mV/pC. The minimum detectable amount of DNA molecules is on the order of 10^7.[8-10] This estimation is based on the DNA detection with the fluorescent approach. The voltage shift of the sensor with such amount of DNA molecules is estimated to be in the order of hundreds of milivolts.

Table 1 The parameters of the CMFET used in designing the detection circuit

Parameters	Values
Size of sensing site [µm]	20 x 20
Sensitivity [mV/pC]	55

3.0 CIRCUIT IMPLEMENTATION

The schematic of the proposed detection circuit is shown in Figure 2. The drain follower achieved low power consumption due to the subthreshold (weak inversion) operation of the transisors. N_1 is the CMFET sensor that is used to detect the DNA hybridization, where V_{in} controls its gate. When V_{in} increases, the floating gate voltage increases linearly and then CMFET will be turned on. The drain follower is able to keep the CMFET to be operated under fixed gate-source and gate-drain voltages.[11] Under fixed operating point condition, long term stability and reduced signal-to-noise ratio are obtained.[12] The changes of the total charge on the sensing site can be detected by observing the changes in the floating gate voltage, while the drain current and control gate voltage of the CMFET are kept constant.

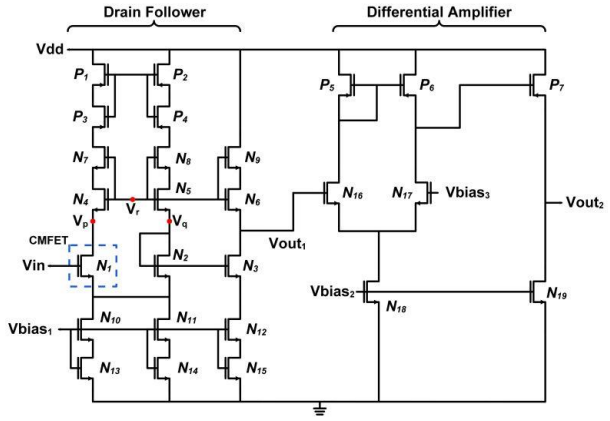


Figure 2 The proposed detection circuit schematic

The change in the floating gate voltage can be observed at the output of drain follower as $V_{out} = V_{in}$. P_1 - P_4 act as the PMOS current mirrors that make the drain current of N_7 and N_8 equal in magnitude. V_p and V_q are equal since they are given by $V_r - V_{TH} - V_{ON}$, where V_{TH} is the threshold voltage and V_{ON} is the overdrive voltage of N_4 and N_5. N_1 (CMFET) and N_2 are biased with the same drain current and drain-source voltage, thus the gate voltage of N_1 is equal to the gate voltage of N_2. N_6 works as the source follower, thus V_{out} is equal to V_{in}.

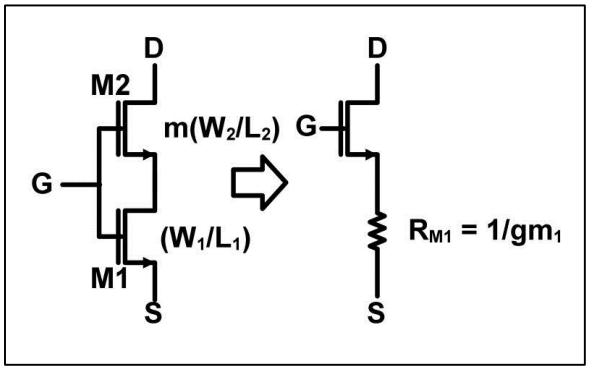


Figure 3 Self-cascode NMOS transistor and equivalent simple transistor

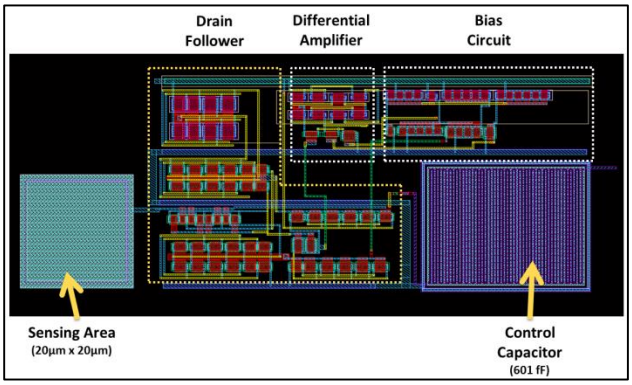


Figure 4 The layout of the complete detection circuit

K. Nakazato[13] reported that the channel length modulation effect in the drain follower can be reduced by using cascode topology. We proposed to use the self-cascode topology in the drain follower circuit in order to reduce this effect. The self-cascode transistor has bigger transconductance, bigger output impedance and no additional supply voltage is needed compared to the simple transistor.[14] Therefore, it is suitable to be used in low voltage applications. Less number of transistor is used for self-cascode topology compared to the cascode topology.

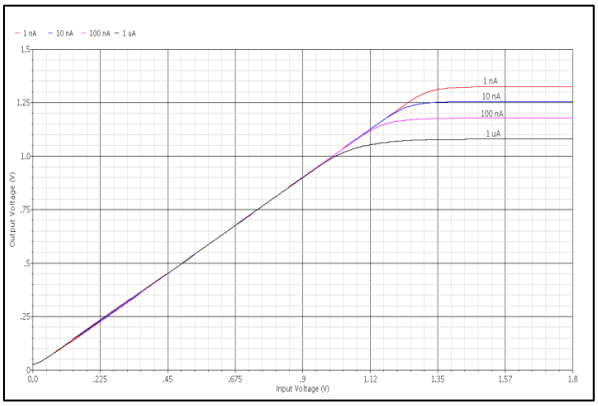
A self-cascode transistor consists of two simple transistors with different width is shown in Figure 3. It can be treated as a single composite transistor. M1 is equivalent to a resistor and the resistance is input dependent. For better result, the W/L ratio of M2 should be larger than W/L ratio of M1, where $W_1/L_1=mW_2/L_2$ and $m > 1$.[15]

The CMOS differential amplifier was used to amplify the output voltage of the drain follower. In designing the differential amplifier, many electrical characteristics such as differential gain, frequency range, input common mode range (ICMR), output swing and offset have to be taken into consideration. The multistage topology was chosen because its performances are more suitable for biosensing application such as high gain, high output swing and low power dissipation.[16] $Vbias_1$, $Vbias_2$ and $Vbias_3$ are biased by a CMOS bias circuit, therefore no external voltage source is needed for biasing purpose other than suppy voltage (Vdd).

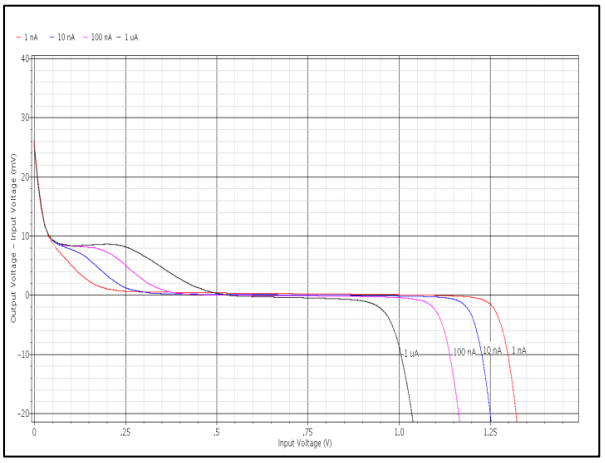
4.0 RESULTS AND DISCUSSION

The simulations of the layout design as shown in Figure 4 were performed by using the 0.18µm Silterra CMOS fabrication process with different process corners and Analog Design Environment from Virtuoso Cadence. The corner analysis of the drain follower is shown in the Figure 6 and all the process corners met with all the required specifications. The chip area for the the detection circuit is 107 µm x 45 µm.

The drain follower can be operated under different bias currents. The total bias current of the drain follower (I_D) was controlled by the voltage of $Vbias_1$. As the I_D increased, the range of input for linear relationship to output decreased, as shown in Figure 5. Lower current means lower power consumption. Therefore, the goal of the design is to design a low power and high accuracy drain follower. The input range of the drain follower was from 0.106 V to 1.28 V within ±5 mV accuracy for I_D = 1 nA.



(a)



(b)

Figure 5 The output waveform of the drain follower with different bias current. (a) The graph of Vout vs. Vin; (b) The graph of Vout -Vin

Figure 7 shows the temperature dependance of the output voltage with input voltage = 0.9 V and I_D = 1nA. The temperature was varied from 20 to 100 °C and the output voltage dropped with temperature. The cut-off frequency of the proposed drain follower was 3.48 MHz for I_D = 1 µA and 5 kHz for I_D = 1 nA. The overall performance of the drain follower is summarized in Table 2

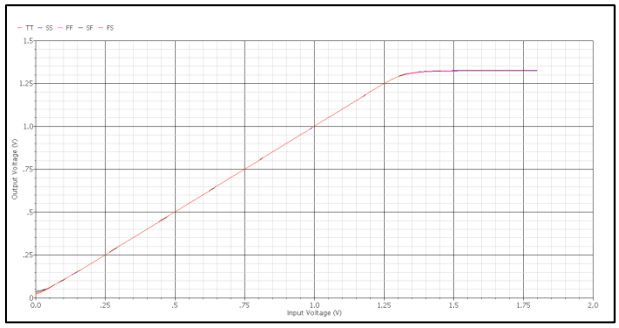


Figure 6 The corner analysis of the drain follower

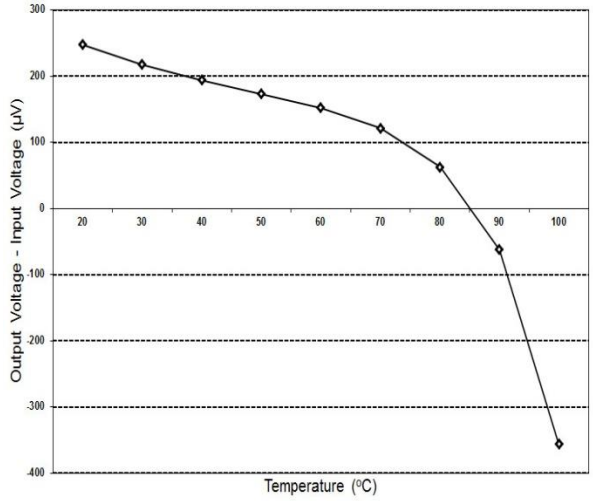


Figure 7 Temperature dependence of the output voltage of drain follower

Table 2 The overall performance of the drain follower.

Specifications	Values
Gain [V/V]	0.998
-3 db Frequency [kHz]	5.0
Input Range [V]	0.106 – 1.28
I_D [nA]	1

The second stage of the detection circuit is the CMOS differential amplifier. Amplification of the output voltage of drain follower is important in improving the recording characteristic of the biosensor. As seen in Figure 8, the designed differential amplifier can amplify the input signal up to 273.5 times and the frequency range was 8.23 kHz with the phase margin of 80°

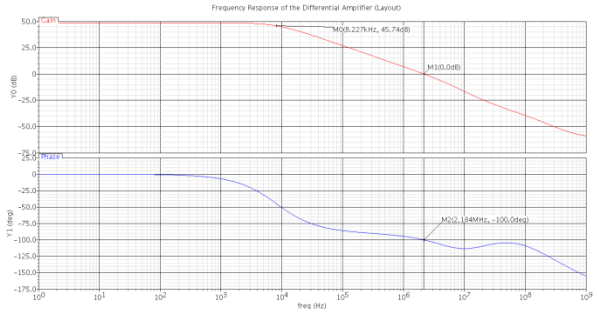


Figure 8 The frequency response of the differential amplifier

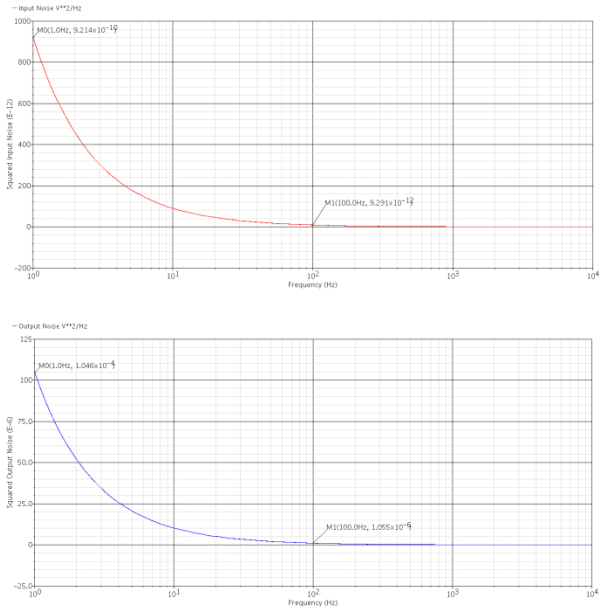


Figure 9 The noise analysis of the detection circuit. (a) Input noise; (b) Output noise

Table 3 The overall performance of the differential amplifier

Specifications	Values
Gain [dB]	48.74
Phase Margin	80°
-3db Frequency [kHz]	8.23
Unity Gain Bandwidth [MHz]	2.16
Input Common Mode Range [V]	0.83 – 1.45
Output Swing [V]	6.33×10^{-6} – 1.79
Common Mode Rejection Ratio [dB]	75.43
Power Supply Rejection Ratio [dB]	41

The noise analysis of detection circuit is shown in Figure 9. The 1/*f* contribution of the input noise was in the range of 0.92 nV^2/Hz to 9.3 pV^2/Hz, while the higher frequency noise was around 1.2 pV^2/Hz. The resulting noise level was considered as small and suitable for DNA sensing purpose. The power consumption was calculated by summing the total current running through each supply path and multiply with the supply voltage. The total power consumption was found to be about 14.87 mW under normal operating conditions. The overall performance of the CMFET based on the detection circuit is summarized in the Table 4.

Table 4 The overall performance of the proposed CMFET based detection circuit

Specifications	Values
Gain [dB]	50.55
-3db Frequency [kHz]	5.72
Unity Gain Bandwidth [kHz]	144.8
Power dissipation [mW]	14.87
Max. Input Noise [nV^2/Hz]	0.92
Max. Output Noise [μV^2/Hz]	104.6
Technology	0.18 µm Silterra
Power supply [V]	1.8

5.0 CONCLUSION

The proposed detection circuit was able to achieve a voltage gain of 50.55 dB in the frequency range up to 5.72 kHz using 0.18 µm technology. The power dissipation of the detection circuit was quite low, which is 14.87.mW. The detection circuit with low input noise is essential especially in biological sensing applications and our detection circuit was able to achieve about 0.92 nV^2/Hz.

The input voltage range of the designed drain amplifier was 0.106 V until 1.28 V within ±5mV accuracy. Self-cascode topology reduces the channel modulation effect and thus improves the performance of the drain follower.

Acknowledgement

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