A UNIFIED CONSTITUTIVE MODEL FOR SOLDER MATERIALS

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Dedicated to Jesus Christ,

The Almighty God and Creator of the Universe

My personal Lord and Savior,

And

To my beloved parents and family.

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ABSTRACT

Solder joint reliability has been the main concern in electronic packaging since the advent of surface mount technology. In this study, a unified constitutive model was developed for finite element analysis of solder joint reliability. The model is based on the Anand model and Runge-Kutta time integration scheme. The constitutive behavior of tin-lead eutectic solder was examined based on published experimental data to establish the material database for the analyses. Procedures to determine the nine model parameters were developed. These parameters were determined using monotonic constant strain rate tensile test data. Two sets of parameters were extracted from representative groups of experimental data. The predictive capability of the Anand model under monotonic loading was assessed by comparing the predictions of the model under tension, strain rate jump, creep and stress relaxation tests with the experimental data. The capability of the model to capture the cyclic behavior of the alloy was also evaluated. Ratcheting effects, low cycle fatigue and load-history dependence of the solder behavior were simulated and compared with the experiments. The model is capable of predicting the behavior of solder materials under both monotonic and cyclic loading conditions for identical batch of specimens. However, the model is not able to simulate fracture of the material, tertiary creep, Bauschinger effects and variations in reported experimental data. A few recommendations were suggested to further improve the model by considering kinematic internal variables, damage and grain size parameters to better represent the behavior of solder materials.

ABSTRAK

Kebolehpercayaan penghubung solder telah menjadi perhatian utama dalam teknologi pembungkusan elektronik sejak penggunaan teknologi pajangan permukaan, untuk kaedah unsur terhingga dalam pemodelan kebolehpercayaan penghubung solder. Dalam kajian ini, satu model penyatuan telah dibangunkan. Model ini adalah berdasarkan Model Anand dan skim integrasi masa Runge-Kutta. Kelakuan solder timah-plumbum eutektik telah dikaji berdasarkan data eksperimen yang diterbitkan bagi membangunkan kumpulan maklumat untuk analisis. Tatacara untuk menentukan sembilan parameter model telah dibangunkan. Parameter ini telah ditentukan dengan menggunakan data eksperimen tegangan dengan kadar terikan malar. Dua set parameter telah diperoleh dari data eksperimen yang berkewakilan. Keupayaan Model Anand untuk meramal pembebanan monotonic telah ditaksir dengan pembandingan ramalan model dan data eksperimen bawah ujian tegangan, ujian lompatan kadara terikan, ujian rayapan dn ujian pengenduran terakan. Keupayaan model untuk meramal kelakuan aloi in bawah beban berulang-ulangan telah dikaji. Kesan "ratchet", kelesuan ulangan rendah dan kebergantungan solder kepada sejarah bebanan telah disimulasikan dan dibandingkan dengan eksperimen. Model ini berkeupayaan untuk meramal kelakuan solder bawah kedua-dua bebanan monotonik dan ulangan untuk kumpulan spesimen yang serupa. Model ini tidak dapat menyimulasi pematahan bahan, rayapan tahap ketiga, kesan "Bauschinger" dan variasi dalam data eksperimen yang dilaporkan. Beberapa cadangan telah dihujahkan untuk terus meperbaiki model ini dengan mempertimbangkan pembolehubah dalaman kinematik, parameter kerosakan dan parameter saiz grain, supaya dapat mewakili kelakuan solder dengan lebih baik.

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a	-	Crack length / strain rate sensitivity of hardening/softening
ABS	-	Absolute value
b	-	Burgers vector
BGA	-	Ball grid array
C4	-	Controlled-collapse chip connection
CBGA	-	Ceramic ball grid array
CSP	-	Chip scale package
CTE	-	Coefficient of thermal expansion
d	-	Grain size
D_{eff}	-	Effective diffusion coefficient
DC	-	Dislocation climb
DCA	-	Direct chip attach
E	-	Young's modulus
ERR	-	Error
ERRMAX	-	Maximum value of error
F_{def}	-	Internal variable
FCOB	-	Flip chip on board
FE	-	Finite element
FEM	-	Finite element method
FPC	-	Flexible printed circuit
G	-	Shear modulus
GBS	-	Grain boundary sliding
h_0	-	Hardening/softening constant
H	-	Work-hardening coefficient
IC	-	Integrated circuit
IGBT	-	Insulated gate bipolar transistor

I/O	-	Input/output
K	-	Bulk modulus
k	-	Boltzmann constant
KGD	-	Known Good Die
LCCC	-	Leadless ceramic chip carrier
LCF	-	Low cycle fatigue
LFBGA	-	Low-profile fine-pitch ball grid array
LOC	-	Lead-on-chip
LOC-TSOP	-	Lead-on-Chip Thin-Small-Outline Package
M	-	Strain rate sensitivity
MLBGA	-	Multilayer laminate ball grid array
n	-	Stress exponent
n_{eff}	-	Effective stress exponent
N_f	-	Number of cycles to failure
N_0	-	Number of cycles for crack initiation
OLGA	-	Organic land grid array
p	-	Grain size exponent
PBGA	-	Plastic ball grid array
PCB	-	Printed circuit board
PTH	-	Plated through hole
Q	-	Activation energy
q	-	Von Mises equivalent stress
R	-	Gas constant
RH	-	Relative humility
s	-	Deformation resistance
s^*	-	Saturation value of s
SMT	-	Surface mount technology
SS_{Res}	-	Residual Sum of Squares
T_m	-	Melting temperature
T_s	-	Mean cyclic temperature
T, Temp	-	Temperature
$TOLR$	-	Tolerance
TSOP	-	Thin single outline package

UCP	-	Unified creep-plasticity
WLCSP	-	Wafer level chip scale package
W^{in}	-	Plastic strain energy
α, ξ	-	Multiplier of stress
ε	-	Total strain
ε_p	-	Inelastic strain
$\Delta\varepsilon_p$	-	Plastic strain range
$\Delta\gamma_t$	-	Total shear strain
λ	-	Conditioning factor
σ	-	Stress
σ_0	-	Intrinsic stress resisting dislocation motion
σ_{flow}	-	Flow stress
τ	-	Shear stress
υ	-	Poisson's ratio
γ	-	Shear strain
*	-	Saturation value
acc	-	Accumulated
ave	-	Average
cr	-	Creep
def	-	Deformation
eff	-	Effective
in	-	Inelastic
j	-	Initial guess
new	-	Next time step value
old	-	Current time step value
pl	-	Plastic

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Overview of Surface Mount Technology (SMT)

Surface mount technology (SMT) offers a lot of advantages over the conventional plated through hole (PTH) technology (Enke *et al.*, 1989; Ren, 2000; Kanchanomai *et al.*, 2002). In a SMT process, a series of devices are simultaneously soldered directly to a printed circuit on a board instead of soldering each device individually. SMT is known to have lower production costs, higher package density and easier automation. Over the past decade, various SMT compatible packaging technologies have been developed to facilitate a wide variety of different cost, pin-count and performance requirements of IC devices. These technologies include direct chip attach (DCA), chip scale package (CSP), wafer level chip scale package (WLCSP), ball grid array (BGA) and area-array solder-bumped flip chip technology, to name only a few (Lau, 1996; Lau and Pao, 1997; Lau and Lee, 1999; Lau, 2000). Figure 1.1 shows some examples of these packaging technologies, used in four of the major IC devices (e.g. ASIC, cache, microprocessor, and system memory) for

various clock frequencies and pin counts (Lau, 2000). Figure 1.2 shows some schematic layouts of the examples of these packaging technologies on a printed circuit board (PCB) (Lau, 2000).

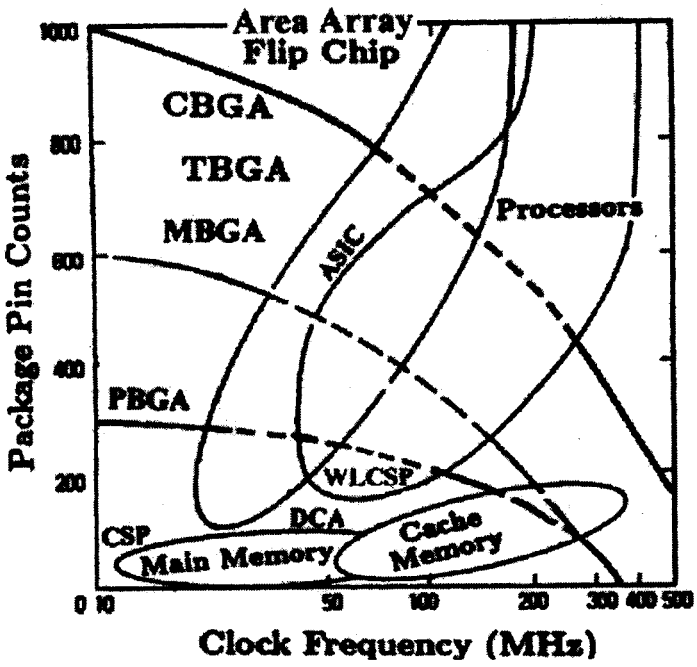

Figure 1.1: Variation of pin counts with clock frequencies for various applications in packaging technologies.

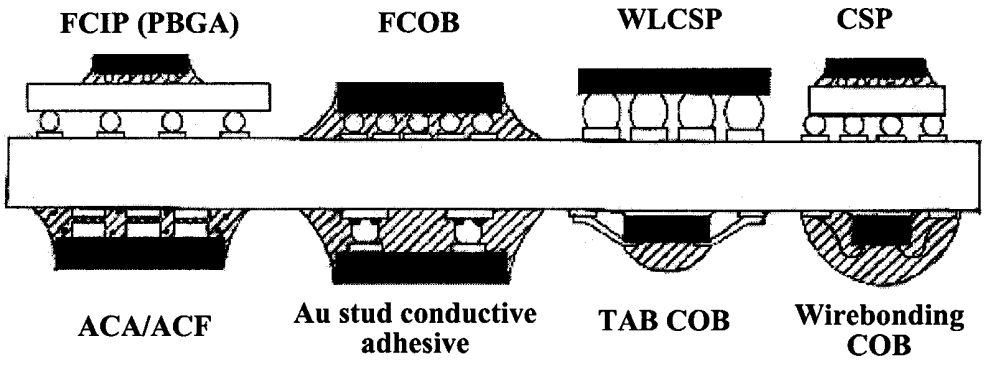

Figure 1.2: Examples of several applications in packaging technologies on a PCB.

One of the most cost-effective SMT compatible packaging technologies is direct chip attach (DCA), also called solder-bumped flip chip on board (FCOB) (Lau and Pao, 1997; Lau, 2000). For the DCA technology, chips are directly attached to the PCB or the flexible printed circuit (FPC) without a package or substrate. Even though the technology has been introduced by the early 1960s, research and development efforts on the FCOB grow significantly only after IBM at Yasu, Japan, assembled solder-bumped flip chip on low-cost organic PCB since 1990 and the publications by Tsukada *et al* (1992) in 1992. Underfill encapsulant is usually required for FCOB assemblies. Figure 1.3 shows a typical FCOB on a low-cost organic PCB with underfill encapsulant (Lau, 2000).

Another new class of SMT compatible technology, called chip scale package (CSP), has also emerged during the past decade (Lau and Lee, 1999). The unique feature of the CSP is that a small substrate (less than 1.5 times the chip size) is used to redistribute the very fine pitch (as small as 0.075mm) peripheral array pads on the

chip to much larger pitch (0.5mm – 1.0mm) area array pads on the PCB. The advantages of CSP over the DCA are that with the substrate, CSP is much convenient for test-at-speed and burn-in for Known Good Die (KGD), for handling, assembling and rework, for die protection, shrinkage and expansion, besides advantages of less infrastructure constraint. Figure 1.4 shows the top view of a substrate of a low-cost chip scale package, NuCSP for memory chips and low-pin-count ASIC, delineating the redistribution of peripheral pads on the chip to the area-array pads on the PCB (Lau and Lee, 1999).

Being SMT compatible as well, Ball Grid Array (BGA) is another technology that has overwhelmed the whole IC packaging industry for the past decade (Huang *et al.*, 2001). BGA has become the choice of the first-level and second-level interconnection as the trend toward higher input/output, performance and yield continues (Liu *et al.*, 2001). Among the advantages of BGA are larger number of I/Os, self-alignment capability, more robust assembly process, better thermal and electrical performance, besides high throughput and low cost assemblies for mass production (Lau, 1996; Lau and Pao, 1997; Lau, 2000; Lee and Huang, 2002). Recently, plastic ball grid array (PBGA) with solder-bumped flip chip has been used to house the microprocessors on organic substrates, instead of the conventional high-cost ceramic substrates. Intel, for instance, employs its organic land grid array (OLGA) package technology to house its top-of-the-line area-array solder-bumped flip chip microprocessors. Figure 1.5 illustrates the schematic overview of an OLGA package (Lau, 2000).

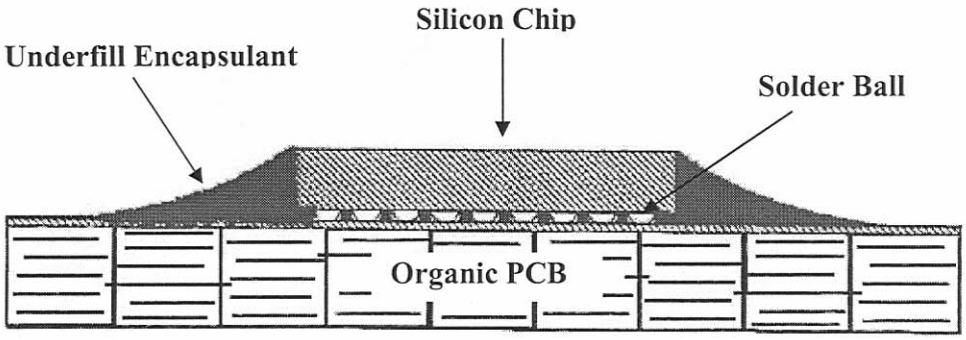

Figure 1.3: A schematic view of low cost flip chip on board (FCOB).

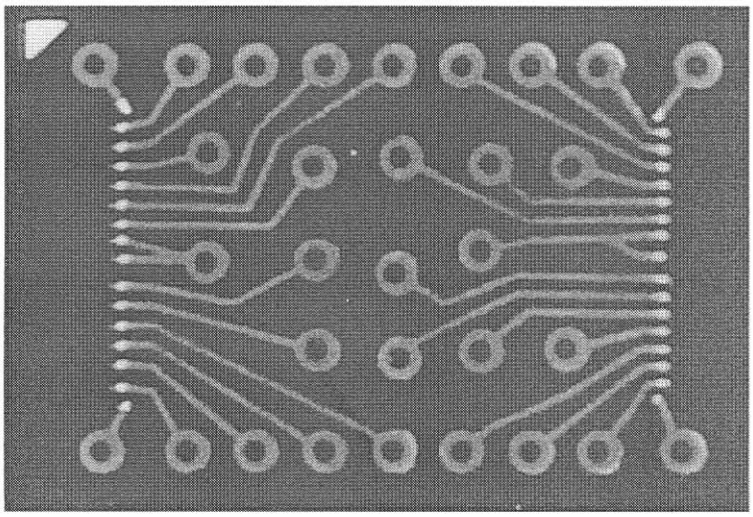

Figure 1.4: NuCSP substrate (top side) for the 32-pin SRAM.

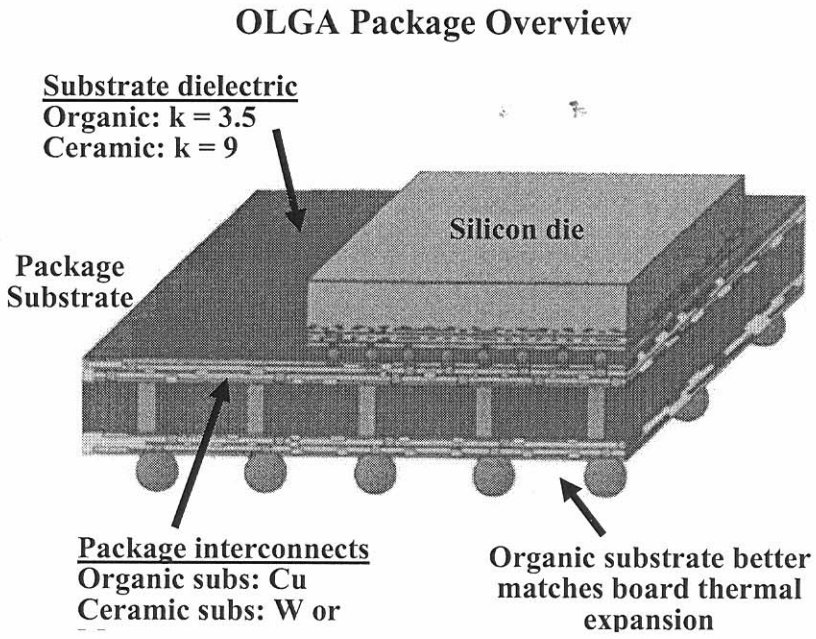

Figure 1.5: OLGA package overview.

1.2 Reliability Concerns of Solder Joints

Solder joints play a crucial role for all these SMT compatible technologies. Solder joints provide both the mechanical support to hold the module in position on the PCB and the electrical connection for the passage of electrical signals, power and ground, at both chip level and printed circuit board (PCB) level assembly (Enke *et al.*, 1989; Logsdon *et al.*, 1990; Lau, 1992; Plumbridge, 1996; Lau, 2000; Lee and Huang, 2002). The electronic package hierarchy consists of basically four levels of packages, namely zero level package (chip level connections), first level package (single chip or multi-chip modules), second level package (PCB) and third level

package (motherboards) (Lau, 2000; Su, 2001). Figure 1.6 shows a schematic representation of these four levels of packages (Lau, 2000). Solder joints, as a very versatile connection method, has been utilized in both the first and the second level of electronic packages, including direct chip attach (second level), chip scale package (first level), and ball grid array (second level).

As solders are very soft alloys, there are new concerns arising, particularly regarding the long term reliability of the solder joints connecting an SMT package to the printed circuit board (PCB) and a silicon chip to the package (Enke *et al.*, 1989). In many electronic systems, reliability losses have been found to result mainly from mechanical failures of the solder joints rather than device malfunctions (Chandaroy, 1998; Stephen and Frear, 1999). Various sources of these mechanical failures are reported and studied in the literature, including cyclic bending (Wu *et al.*, 2002) and drop impact (Mishiro *et al.*, 2002). However, apart from catastrophic failures such as die or substrate cracking, the primary failures induced in electronic packages are attributed to thermomechanical fatigue, in the forms of solder cracking, crack propagation and interface delamination (Zhuang *et al.*, 2001; Kuang *et al.*, 2001; Ciappa, 2002).

As there is a mismatch of the coefficient of thermal expansion (CTE) between two soldered components, solder joints will inevitably suffer from cyclic strains during power on/off and temperature fluctuations, due to both device internal dissipation and ambient temperature changes. Progressive damage as a result of thermomechanical fatigue is experienced in the solder joints, leading to ultimate failure eventually. For instance, in the low cost flip chip technology, the CTE mismatch between the silicon (CTE = 2.5 ppm/K) and a cost effective commonly

used substrate material like FR4 (CTE = 18.5 ppm/K) is as high as 16 ppm/K, which ineluctably raises concerns over the thermomechanical fatigue reliability of the tiny solder joints (Wiese *et al.*, 1999). Figure 1.7 (Amagai, 1999) shows an example of solder cracking as a result of thermomechanical fatigue. The crack appeared at the interface between solder and the chip/substrate, one of the most common places where solder joint failures occur (Lee *et al.*, 1998; Zhang *et al.*, 2000; Su, 2001).

Recent developments in the semiconductor industry only further aggravate the situation. First, dramatic increase in the number of devices and functionality of the latest ultra large, giga, and other yet-to-come scale integration designs has resulted in increased chip sizes (Amagai, 1999; Zhuang *et al.*, 2001; Lau, 2000). According to the Semiconductor Industry Association (SIA)'s technology tends, the chip sizes of some IC devices are forecast to be as large as 10 cm^2 by the year 2006 (Lau, 2000). These gigantic chips will impose severe strain on the solder joints at the corners of the devices, where the maximum deformation of the substrate and maximum stress in the solder joints occurred.

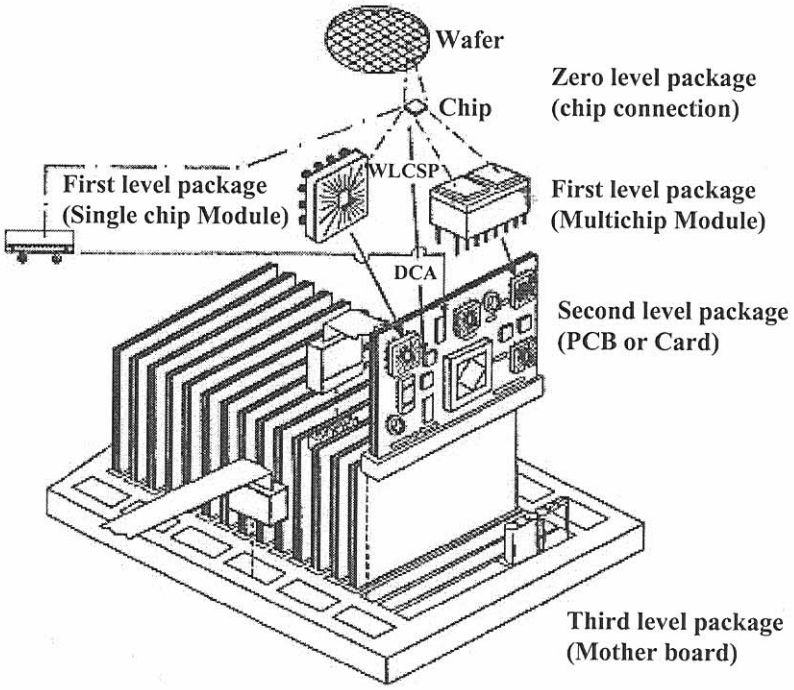

Figure 1.6: Hierarchy of electronic packages.

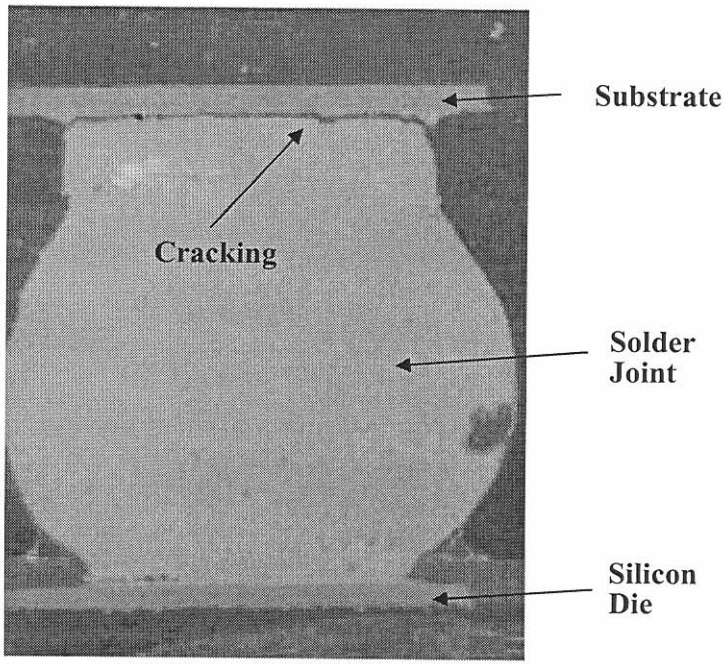

Figure 1.7: An example of failure of a solder joint by cracking between solder and substrate interface.

Higher circuit board component densities are achieved by having smaller package dimensions, leading to very fine feature sizes that are often more sensitive to package induced stresses (Amagai, 1999). Higher densities and smaller feature sizes stipulate the development of advanced packages containing a higher number of interconnections (Wen *et al.*, 2002). A logical consequence of such development is the reduction in the volume of the solder joints. Smaller solder joints, however, pose numerous mechanical considerations, for they are mechanically and electrically more vulnerable than the larger ones. Hence, the continual miniaturization of package dimensions imposes continuing challenges on the thermomechanical reliability aspects of solder joints.

Meanwhile, modern electronic devices are frequently subjected to severe operating conditions and environment, including higher temperature levels, and fluctuating stresses and temperatures (Wade *et al.*, 1999; Nowottnick *et al.*, 2000). Typical operating conditions include a high temperature environment (up to 150°C) with frequent temperature oscillations and mechanical vibrations from 20 to 2000Hz (McDougall, 1998; Wiese *et al.*, 1999). In automotive applications, for example, the electronic modules are subject to extreme operating conditions, such as cyclic temperature variations, vibration, and humidity (Shangguan, 1999; Wilde, 2001). Table 1.1 illustrates the severe specifications for service environments of automotive electronic units (Wilde, 2001). These loading conditions and environments induce higher temperatures in the creep range, high amplitude vibration and mechanical shock. These trends in IC devices are leading to rigorous requirements on the thermal, electrical and mechanical characteristics of the packaging devices. Consequently, the reliability of the solder joints remains one of the greatest challenges to the package designers and engineers.

Table 1.1: Severe specifications for the automotive electronics.

	Environmental Conditions		
Unit	ECU	ECU	Sensors
Environment Classification	Under the Hood	On the Engine	On the Engine
Temperature Range	-40°C to 125°C	-40°C to 150°C	-40°C to 175°C
Vibration	Up to 3g	Up to 10g	Up to 40g
Shock	Up to 20g	Up to 30g	Up to 50g

1.3 Finite Element Method and Lifetime Prediction of Solder Joints

The development of estimation methods to predict the reliability and the lifetime of a particular packaging design has become of paramount importance to the packaging industry. Many methods of estimation of the fatigue life of solder alloys have been proposed (Solomon, 1989; Satoh *et al.*, 1991; Pao *et al.*, 1993; Vaynman and Mckeown, 1993; Solomon and Tolksdorf, 1995; Subbarayan, 1996; Guo and Conrad, 1996; Ishikawa *et al.*, 1996; Zhang *et al.*, 2000b). Of all these methods, finite element (FE) method has been utilized extensively to estimate the strain range, work density and other damage parameters of the packages. The thermomechanical modeling has proven to permit significant cost reduction in both the design of high reliability and the failure analysis of solder joints in the electronic packaging and surface mount technology.

Numerous applications of FE analyses to assess the reliability of the solders are available in the literature. Tee *et al.* (2000) built a FE model to predict the fatigue life of solder joints in their low profile fine-pitch BGA (LFBGA) during thermal cycling tests. The effects of key package parameters, such as die size, substrate size and solder ball size were studied. Bailey *et al.* (2001) employed FE in their computational models to assess solder joints reliability. Suhling *et al.* (1994) employed FE analysis to evaluate the fatigue life and reliability of solder joints used to attach leadless ceramic chip resistors and chip capacitors to insulated metal substrates. Lau (1998) estimated the thermal fatigue life of the solder joints of a NuCSP assembly using the FE modeling. Solder deformations are considered to be either temperature-dependent elasto-plastic or time-dependent elasto-plastic-creep. Lau *et al.* (2000) investigated a novel and reliable wafer level chip scale package (WLCSP) by performing nonlinear time-temperature-dependent FE analyses. The thermal-fatigue life of the corner solder joint was predicted by the averaged creep strain energy density range per cycle and a linear fatigue crack growth rate theory.

The usage of FE analyses is not confined to the reliability estimation only, but also in various physical analyses, parametric studies and processing of experimental data. In order to compare the solder joints reliability of the novel LOC-TSOP (Lead-on-Chip Thin-Small-Outline Package) to the conventional LOC-TSOP, Lin and Chiang (2000) used a nonlinear FE analysis to analyze the physical behavior of packages under a thermal loading condition. It is found that the maximum plastic strain occurred at the leadframe/solder interface inside the solder joints, where crack initiation occurs. Moore and Jarvis (2001) employed FE analyses to find the root cause of the observed failure modes of their BGA packages in the design of improved reliability BGA assembly. Lee and Huang (2002) used FE analysis to

investigate the effect of shear ram speed on the solder ball shear strength of PBGA packages. Jonnalagadda (2002) developed a FE model to qualitatively identify the high risk regions within the via-in-pad structure under mechanical bending. Mishiro *et al.* (2002) used the numerical analysis to find the correlation between solder joint stresses and motherboard strains in their study on the effect of the drop impact on BGA and CSP package reliability. Wiese *el at.* (1999) applied FE simulation to evaluate the experimental raw data to extract material parameters for their model. Other examples of the applications of the finite elements analyses include the warpage analyses (Lee, 2000; Miyake *et al.*, 2001), the properties of substrates (Moore and Jarvis, 2002), the effects and deformation of the underfill (Su *et al.*, 1999; Cheng *et al.*, 2000), cracks (Wu *et al.*, 1998), material selections (Khan and Molligan, 2001), testing designs (Hui and Ralph, 1997; Xie, 2000), parametric studies (Popelar, 1997; Lee and Lau, 2000; Okura *et al.*, 2000) and interfacial fracture toughness (Wang *et al.*, 1999; Gu *et al.*, 2001).

1.4 Constitutive Models for Material Modeling

The accuracy of FE prediction depends on the precise modeling of the behavior of the solder materials (Frost *et al.*, 1988). This is a significant task as the behavior of the solder alloys throughout their service lives is complicated (Basaran and Chandaroy, 1998; Palmer *et al.*, 2000). As solders usually operate at high homologous temperatures, both time-dependent creep and time-independent plasticity are significant parts of solder deformation. Solder materials are also highly viscoplastic, with high degree of dependence on both the temperature and strain rate.

At elevated temperatures (room temperature with homologous temperature of 0.65 is considered high for solders), the alloy is significantly weaker as creep and stress relaxation occur rapidly. At lower temperatures, the alloy is stronger and creep phenomenon is less severe. The thermomechanical properties and behavior of solder joints depend on the microstructure as well (Basaran and Chandaroy, 1998). In general, solder materials are significantly weaker with smaller grain sizes.

For accurate estimation of deformation responses of a package by FE analyses, constitutive models incorporated in the analyses should be able to simulate the deformation and stress-strain behavior of the solder alloys. A realistic constitutive model has become an indispensable prerequisite for FE simulations of electronic packaging devices. A good constitutive model must be able to predict and extrapolate beyond the existing experimental measurements. This extrapolation encompasses three main segments: from simple test data to complex histories; from short-term tests to long-term service; and from a small number of test data to all of the temperatures and strain rates of interest. The success of the extrapolation pivots on the physical soundness of the models. The closer the phenomenological description reflects the actual physical processes involved, the further it can be extrapolated beyond the range of variables for which it was measured (Kocks, 1987).

Despite this physical soundness necessity, most currently used constitutive models are simple models, intriguing concern over the validity and the accuracy of the predicted results. Classical constitutive models of materials artificially separate the inelastic strain into various parts, including time-independent plastic strain, time-dependent creep strain and transient strain, each with its respective empirical equations. Even though it is simpler to implement and easier to understand with such

separation, there is a lack of physical bases for the postulate. Both the creep and plasticity are controlled by the similar mechanisms, such as diffusion, climb, dislocation and viscous glide (Miller, 1987). Hence, it is natural to represent both creep and plasticity with a single set of constitutive equations. Models with such approach are called unified constitutive models. There is an urgent need to develop and apply such unified models in future analyses to obtain reliable results.

The Anand model is one of the most widely used unified constitutive models for modeling solder alloy in the electronic packaging simulations. However, its popularity is due to the simplicity and availability of the model, rather than the suitability and accuracy of the prediction (Wang, 2001). As the Anand model is relatively simple, with only one scalar internal variable and nine material parameters, the model is preferred by many researchers to other unified constitutive models with intricate, and sometimes even formidable, evolution equations. For example, the full set of MATMOD-4V equations has 21 parameters and five complicated evolution equations (Miller, 1987). Furthermore, the Anand model is readily applied by the researchers, as the model is incorporated in commercial FE packages, such as ANSYS. This makes the model exceptionally attractive to packaging designers and engineers.

Notwithstanding its popularity, comprehensive studies on the suitability and validity of the Anand model in representing the viscoplastic constitutive behavior of solder materials are limited, if there is any. The Anand model was implemented prevalently in an *ad hoc* manner, without proper and systematical assessment of the accuracy of the prediction of the model, particularly when applied to the solder materials. The capability of the model to predict cyclic behavior is obscure. Hence,

prompt study to scrutinize the predictive capability of the Anand model is imperative to ascertain the accuracy and reliability of the FE analyses of electronic packages.

1.5 Objectives and Scopes of the Study

The objectives of this study are as follows:

1) To develop a unified inelastic strain model for solder materials.

2) To examine the model for mechanical responses of tin-lead solder alloys subjected to loading conditions of electronic components.

The scope of current study includes the followings.

1) Gathering of published experimental data on the tin-lead solder alloy, particularly eutectic solder. This information constitutes of mechanical properties and behavior of the material.

2) Formulation of the unified constitutive model based on the work of Anand (1985). The model is employed using Runge-Kutta integration scheme. Procedures to determine the model parameters are developed.

3) Establishment and validation of sets of model parameters for eutectic tin-lead solder alloys, based on monotonic loading data.

4) Examination of the predictive capability of the model for monotonic and cyclic response of the solder alloy. The capability of the model to handle variations in the reported data is assessed.

A few assumptions and constraints are imposed throughout this study. These assumptions are as follows.

1) The study is primarily on tin-lead near eutectic solder, with composition Sn63-Pb37 or Sn60-Pb40. Both compositions are assumed to have similar constitutive behavior.

2) The study is conducted under normal operating conditions of solder joints, with temperatures range from -55°C to 150°C and strain rates range from 1.0E-5/s to 1.0E-1/s. Even though the model can be applied for temperature and strain rate out of above range, the accuracy of the prediction is not critical and will not be investigated.

3) Von Mises yield criteria are assumed throughout the study. Shear test data are converted to tension data using the equations $\sigma = \tau\sqrt{3}$ and $\dot{\varepsilon} = \dot{\gamma} / \sqrt{3}$ for the comparison purposes.

4) The present study is confined to uniaxial loadings only.

1.6 Thesis Layout

Chapter 1 of the thesis describes the background and the necessity of the current study. The development of the surface mount technology is overviewed and the new arising concerns regarding the solder joint reliability are discussed. The importance of finite element analyses and lifetime predictions of solder joints is demonstrated. The need to implement physically sound unified constitutive models in solder material modeling is delineated. The necessity to conduct comprehensive study to assess the suitability and predictive capability of the Anand model in

representing the constitutive behavior of solder materials is coherently illustrated. The objectives and the scope of the study are unambiguously presented.

Chapter 2 reviews the types of solder materials currently in use, including the lead free solders. Physical properties of eutectic tin-lead solder are adequately reviewed, comparing data reported by various authors in the literature. The viscoplastic constitutive behavior of eutectic tin-lead solder is critically reviewed, building up the essential material database for the study. The diversities in the reported experimental data and possible factors contributing to such diversities are also discussed. The reviews of available constitutive models are presented, including the applications of the Anand model in the literature by various authors.

Chapter 3 formulates the unified constitutive model employed throughout the analyses in the study, based on the Anand model. Outlines of the study are presented and experimental data utilized in the analyses are summarized. The equations for the elastic moduli used in the analyses are derived. The flow and evolution equations in the Anand model are studied and procedures to determine the nine Anand model parameters are developed. The parameter sets obtained in the study are presented and compared with the reported values in the literature. Time integration schemes implemented in the analyses are discussed and the details of the integration are demonstrated.

Chapter 4 presents and discusses the simulation results of current studies, compared with the published data from the literature. To verify the model, predictions of the Anand model using the parameters obtained are compared with similar sets of experimental data from which the parameters are acquired. The

predictive capability of the Anand model under monotonic loading is assessed. Predictions of the Anand model under tensile loadings, strain rate jump tests, creep tests and stress relaxation tests are compared with the experimental data from the same authors. The capability of the model to extrapolate from the monotonic experimental data to the cyclic behavior is also evaluated. Ratcheting effects, low cycle fatigue and load-history dependence of the behavior of solder are simulated and compared with the experimental data. The capability of the model to handle variations in the reported experimental data is then examined. Several phenomena that the Anand model is not able to predict are presented. Interpretation of the Anand parameters to assess the underlying mechanisms is further discussed.

Chapter 5 concludes the finding of the study. The reported behavior of tin-lead eutectic solder is found to vary from one source to another, even under similar chemical composition, depending on its manufacturing processes and microstructures. The Anand model is capable to predict the behavior of solders under both monotonic and cyclic loadings, if the same experimental sets are considered. Significant discrepancies are found between the predictions and the experimental data in the directional hardening behavior, such as Bauschinger effects. The Anand model also fails to predict the diversity in reported experimental data. Various suggestions are proposed for the future improvement of the Anand model.

parameter may be developed to further represent the growth of grain size during temperature and cyclic loadings.

REFERENCE

Abtew, M and Selvaduray, G. (2000). Lead-Free Solders in Microelectronics. *Material Science and Engineering*. 27: 95 – 141.

Adams, P. J. (1986). *Thermal Fatigue of Solder Joints in Micro-Electronic Devices*. Massachusetts Institute of Technology. M.Sc. Thesis.

Amagai, M. (1999a). Characterization of Chip Scale Packaging Materials. *Microelectronics Reliability*. 39(9): 1365 – 1377.

Amagai, M. (1999b). Chip Scale Package (CSP) Solder Joint Reliability and Modeling. *Microelectronics Reliability*. 39(4): 463 – 477.

Amagai, M. (2002). Mechanical Reliability in Electronic Packaging. *Microelectronics Reliability*. 42(4-5): 607 – 627.

Amagai, M and Nakao, M. (1998). Ball Grid Array (BGA) with the Copper Core Solder Balls. *1998 Electronic Components and Technology Conference*. 25 – 28 May 1998. Seattle, WA: IEEE, 692 – 701.

Amagai, M., Watanabe, M., Omiya, M. Kishimoto, K. and Shibuya, T. (2002). Mechanical Characterization of Sn-Ag-Based Lead-Free Solders. *Microelectronics Reliability*. 42(6): 951 – 966.

Anand, L. (1985). Constitutive Equations for Hot Working of Metals. *Journal of Plasticity*. 1: 213 – 231.

Artaki, I., Jackson, A. M. and Vianco, P. T. (1994). Fine Pitch Surface Mount Assembly with Lead-Free, Low Residue Solder Paste. *Proceedings on Surface Mount Int. Conf. and Exosition.* 449 – 459.

Bailey, C., Lu, H., Glinski, G., Wheeler, D., Hamilton, P., Hendriksen, M. and Smith, B. (2001). Using Computer Models to Identify Optimal Conditions for Flip-Chip Assembly and Reliability. *Circuit World.* 28(1): 14 – 20.

Basaran, C. and Chandaroy, R. (1998). Mechanics of Pb40/Sn60 Near-Eutectic Solder Alloys Subjected to Vibrations. *Applied Mathematical Modelling.* 22: 601 – 627.

Basaran, C. and Chandaroy, R. (2000). Using Finite Element Analysis for Simulation of Reliability Tests on Solder Joints in Microelectronic Packaging. *Computers and Structures.* 74: 512 – 231.

Biglari, M. H., Oddy, M. Oud, M. A. and Davis, P. (2000). Pb-Free Solders Based on SnAgCu, SnAgBi and SnCu for Wave Soldering of Electronic Assemblies. *Proceedings of the Electronic Goes Green 2000+.* Sept 11 – 13. Berlin: 73 – 82.

Brown, S. B. (1987). *An Internal Variable Constitutive Model for the Hot Working of Metals.* Massachusetts Institute of Technology: Ph.D. Thesis.

Brown, M. D., Singh, S. B., Malshe, A. P., Gordon, M. H., Schmidt, W. F. and Brown, W. D. (1999). Thermal and Mechanical Analysis of high-power GaAs Flip-chips on CVD Diamond Substrates. *Diamond and Related Materials.* 8(10): 1927 – 1935.

Buechner, P. M., Stone, D. and Lakes, R. S. (1999). Viscoelastic Behavior of Superplastic 37 wt% Pb 63 wt% Sn over a Wide Range of Frequency and Time. *Scripta Materialia.* 41(5): 561 – 567.

Chandaroy, R. (1998). *Damage Mechanics of Microelectronic Packaging Under Combined Dynamic and Thermal Loading*. State University of New York at Buffalo: Ph.D. Thesis.

Chapra, S. C. and Canale, R. P. (2002) *Numerical Methods for Engineers: with Software Application and Programming*. 4th ed. Boston: McGraw Hill.

Chen, J. C. C. (2000). *Static and Cyclic Shear Deformation Response of Eutectic Sn-Pb Soldering Joints for Electronic Packaging*. University of Toronto: Ph.D. Thesis.

Cheng, Z., Chen, L., Wang, G., Xie, X. and Zhang, Q. (2000a). The Effects of Underfill and Its Material Models on Thermomechanical Behaviors of Flip Chip Package. *2000 Int'l Symp on Electronic Materials & Packaging*. Nov. 30 – Dec. 2, 2000. Hong Kong. IEEE, 232 – 239.

Cheng, Z. N., Wang, G. Z., Chen, L., Wilde, J. and Becker, K. (2000b). Viscoplastic Anand Model for Solder Alloys and its Application. *Soldering & Surface Mount Technology*. 12(2): 31 – 36.

Chiu, C. P., Maveety, J. G. and Tran, Q. A. (2002). Characterization of Solder Interfaces using Laser Flash Metrology. *Microelectronics Reliability*. 42(1): 93 – 100.

Choi, S., Bieler, T. R., Subramanian, K. N. and Lucas, J. P. (2001a). Effects of Pb Contamination on the Eutectic Sn-Ag Solder Joint. *Soldering & Surface Mount Technology*. 13(2): 26 – 29.

Choi, S., Lee, J. G., Guo, F., Bieler, T. R., Subramanian, K. N. and Lucas, J. P. (2001b). Creep Properties of Sn-Ag Solder Joints Containing Intermetallic Particles. *JOM*. 53(6): 22 – 26.

Ciappa, M. (2002). Selected Failure Mechanisms of Modern Power Modules. *Microelectronics Reliability*. 42(4-5): 653 – 667.

Courtney, T. H. (2000). *Mechanical Behavior of Materials*. 2nd Edition. New York: McGraw Hill.

Darveaux, R. (1997). Effect of Simulation Methodology on Solder Joint Crack Growth Correlation. *2000 Proceedings on the Electronic Components and Technology Conference.* 21 – 24 May, 2000. Las Vegas: IEEE, 1048 – 1058.

Darveaux, R. and Banerji, K. (1992). Constitutive Relations for Tin-Based Solder Joints. *IEEE Transactions on Components, Hybrids, and Manufacturing Technology.* 15(6): 1013 – 1024.

Darveaux, R., Banerji, K., Mawer, A. and Dody, G. (1995). Reliability of PBGA Assembly. In: Lau, J. H. (ed.) *Ball Grid Array Technology*. New York: McGraw-Hill. 379 – 395.

Desai C. S. and Whitenack, R. (2001) Review of Models and the Disturbed State Concept for Thermomechanical Analysis in Electronic Packaging. *Journal of Electronic Packaging.* 123: 19 – 33.

Dudek, R., Nylen, M., Schubert, A., Michel, B. and Reichl, H. (1997). An Efficient Approach to Predict Solder Fatigue Life and its Application to SM and Area Array Components. *Proceedings of the 1997 Electronic Components and Technology Conference.* 462 – 471.

Dunn, B. D. (1975). The Properties of Near-Eutectic Tin/Lead Solder Alloys Tested between +70°C and -60°C and the Use of Such Alloys in Spacecraft Electronics. European Space Agency, Technical Memorandum ESA TM-162 (ESTEC). Sept. 1975.

Engelmaier, W. (1992). Reliable Surface Mount Solder Attachments through Design and Quality Manufacturing. *Proceedings Int. Workshop SMT Rel. Manufact. Issues.* Zurich.

Enke, N. F., Kilinski, T. J., Schroeder, S. A. and Lesniak, J. R. (1989). Mechanical Behaviors of 60/40 Tin-Lead Solder Lap Joints. *IEEE Trans of Components, Hybrid, and Manufacturing Technology*. 12(4): 459 – 468.

European Parliament (2003a). *Directive 2002/96/EC of the European Parliament and of the Council on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RHS)*. Directive 2002/95/EC.

European Parliament (2003b). *Directive 2002/96/EC of the European Parliament and of the Council on Waste Electrical and Electronic Equipment*. Directive 2002/96/EC.

Frost, H. J., Howard, R. T., Lavery, P. R. and Lutender, S. D. (1988). Creep and Tensile Behavior of Lead-Rich, Lead-Tin Solder Alloys. *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*. 11(4): 371 – 379.

Frear, D. R., Jang, J. W., Lin, J. K. and Zhang, C. (2001). Pb-Free Solders for Flip-Chip Interconnects. *JOM*. 28 – 38.

Garofalo, F. (1963). An Emperical Relation Defining the Stress Dependence of Minimum Creep Rate in Metals. *Transactions on the AIME*. 227: 351 – 362.

Grossmann, G. (1999). The Deformation Behavior of Sn62Pb36Ag2 and Its Implications on the Design of Thermal Cycling Tests for Electronic Assemblies. *IEEE Transactions on Electronics Packaging Manufacturing*. 22(1): 71 – 79.

Grossmann, G., Weber, L. and Heiduschke, K. (1996). Metallurgical Considerations for Accelerated Testing of Soft Solder Joints. *1996 IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium*. 14 – 16 Oct. 1996. Austin, TX.: IEEE, 298 – 304.

Grusd, A. (1999). Connecting to Lead-Free Solders. *Circuits Assembly*. 32 – 38.

Gu, Y., Nakamura, T., Chen, W. T. and Cotterell, B. (2001). Interfacial Delamination Near Solder Bumps and UBM in Flip-Chip Packages. *Transactions of the ASME Journal of Electronic Packaging*. 123: 295 – 301.

Guo, Z. and Conrad, H. (1996). Effect of Microstructure Size on Deformation Kinetics and Thermo-Mechanical Fatigue of 63Sn37Pb Solder Joints. *Journal of Electronic Packaging*. 118: 49 – 54.

Guo, F., Lee, J., Lucas, J. P., Subramanian, K. N. and Bieler, T. R. (2001a). Creep Properties of Eutectic Sn-3.5Ag Solder Joints Reinforced with Mechanically Incorporated Ni Particles. *Journal of Electronic Materials*. 30(9): 1222 – 1227.

Guo, F., Lucas, J. P. and Subramanian, K. N. (2001b). Creep Behavior in Cu and Ag Particle-Reinforced Composite and Eutectic Sn-3.5Ag and Sn-4.0Ag-0.5Cu Non-Composite Solder Joints. *Journal of Material Science: Material in Electronics*. 12(1): 27 – 35.

Harrison, M. R., Vincent, J. H. and Steen, H. A. H. (2001). Lead-Free Reflow Soldering for Electronics Assembly. *Soldering & Surface Mount Technology*. 13(3): 21 – 38.

Hong, B. Z. (1997). Finite Element Modeling of Thermal Fatigue and Damage of Solder Joints in a Ceramic Ball Grid Array Package. *Journal of Electronic Materials*. 26(7): 814 – 820.

Hong, B. Z. (1998). Thermal Fatigue Analysis of a CBGA Package with Lead-Free Solder Fillets. *1998 ITHERM InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*. 27 – 30 May 1998. Seattle, WA.: IEEE, 205 – 211.

Huang, X., Lee, S. W. R., Yan, C. C. and Hui, S. (2001). Characterization and Analysis on the Solder Ball Shear Testing Conditions. *Proceedings of 2001*

Electronic Components and Technology Conference. 29 May – 1 June 2001. Orlando, FL.: IEEE, 1065 – 1071.

Hui, I. K. and Ralph, B. (1997). A Study of the Strength and Shape of Surface Mount Technology Leadless Chip Solder Joints. *Proc. Instn Mech. Engrs. Part B.* 211: 29 – 41.

Hwang, J. S., Guo, Z. and Koenigsmann, H. (2001). A High-Performance Lead-Free Solder – the Effects of In on 99.3Sn/0.7Cu. *Soldering & Surface Mount Technology.* 13(2): 7 – 13.

Igoshev, V. I. and Kleiman, J. I. (2000). Creep Phenomena in Lead-Free Solders. *Journal of Electronic Materials.* 29(2): 244 – 250.

Igoshev, V. I., Kleiman, J. I., Shangguan, D., Wong, S. and Michon, U. (2000). Fracture of Sn-3.5%Ag Solder Alloy Under Creep. *Journal of Electronic Materials.* 29(12): 1356 – 1361.

Ishikawa, H., Sasaki, K., and Ohguchi, K. (1996). Prediction of Fatigue Failure of 60Sn-40Pb Solder Using Constitutive Model for Cyclic Viscoplasticity. *Journal of Electronic Packaging.* 118: 164 – 169.

Jadhav, S. G., Bieler, T. R., Subramanian, K. N. and Lucas, J. P. (2001). Stress Relaxation Behavior of Composite and Eutectic En-Ag Solder Joints. *Journal of Electronic Materials.* 30(9): 1197 – 1205.

Jones, W. K., Liu, Y., Shah, M. and Clarke, R. (1998). Mechanical Properties of Pb/Sn, Pb/In and Sn-In Solders. *Soldering & Surface Mount Technology.* 10(1): 37 – 41.

Jonnalagadda, K. (2002). Reliability of Via-In-Pad Structures in Mechanical Cycling Fatigue. *Microelectronics Reliability.* 42(2): 253 – 258.

Kahsyap, B. P. and Murty, G. S. (1981). Experimental Constitutive Relations for the High Temperature Deformation of a Pb-Sn Eutectic Alloy. *Materials Science and Engineering*. 50: 205 – 213.

Kanchanomai, C., Yamamoto, S., Miyashita, Y, Mutoh, Y. and McEvily, A. J. (2002). Low Cycle Fatigue Test for Solders using Non-Contact Digital Image Measurement System. *International Journal of Fatigue*. 24: 57 – 67.

Kariya, Y., Williams, N., Gagg, C. and Plumbridge, W. (2001). Tin Pest in Sn-0.5 wt.% Cu Lead-Free Solder. *JOM*. 39 – 41.

Khan, S. and Molligan, D. J. (2001). Finite Element Modeling to Analyze Durability of BGA/CSP Connections during Thermal Shock. *Circuit World*. 27(4): 8 – 11.

Kocks, U. F. (1987). Constitutive Behavior Based on Crystal Plasticity. In: Miller, A. K. eds. *Unified Constitutive Equations for Creep and Plasticity*. London: Elsevier Applied Science. 1 – 88.

Korhonen, T. M. and Kivialhti, J. K. (1996). Thermodymamics of the Sn-In-Ag Solder System. *Journal of Electronic Materials*. 27(3): 149 – 158.

Kuang, J. H., Sheen, M. T., Chang, C. F. H., Chen, C. C., Wang, G. L. and Cheng, W. H. (2001). Effect of Temperature Cycling on Joint Strength of PbSn and AuSn Solders in Laser Packages. *IEEE Transactions on Advanced Packaging*. 24(4): 563 – 568.

Lau, J. H. ed. (1991). *Solder Joint Reliability: Theory and Applications*. New York: Van Nostrand Reinhold.

Lau, J. H. ed. (1996). *Flip Chip Technologies*. New York: McGraw-Hill.

Lau, J. H. (1998). Solder Joint Reliability of a Low Cost Chip Size Package – NuCSP. *Microelectronics Reliability*. 38: 1519 – 1529.

Lau, J. H. ed. (2000). *Low Cost Flip Chip Technologies: For DCA, WLCSP, and PBGA Assemblies*. New York: McGraw-Hill.

Lau, J. H. and Chang, C. (1999). TMA, DMA, DSC and TGA of Lead Free Solders. *Soldering & Surface Mount Technology*. 11(2): 17 – 24.

Lau, J. H. and Lee, S. W. R. eds. (1999). *Chip Scale Package (CSP): Design, Materials, Processes, Reliability, and Applications*. New York: McGraw-Hill.

Lau, J. H. and Pao, Y. H. eds. (1997). *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies*. New York: McGraw-Hill.

Lau, J. H., Dody, G., Chen, W., McShane, M., Rice, D., Erasmus, S. and Adamjee, W. (1992). Analytical and Experimental Studies of 208-Pin Fine Pitch (0.5mm) Quad Flat Pack Solder-Joint Reliability. *Circuit World*. 18(2): 13 – 19.

Lau, J. H., S. W. R. Lee and Chang, C. (2000). Solder Joint Reliability of Wafer Level Chip Scale Packages (WLCSP): A Time-Temperature Dependent Creep Analysis. *Transactions of the ASME Journal of Electronic Packaging*. 122: 311 – 316.

Lee, M. (2000). Finite Element Modelling of Printed Circuit Boards (PCSs) for Structural Analysis. *Circuit World*. 26(3): 24 – 29.

Lee, N. C. (1997). Getting Ready for Lead-Free Solders. *Soldering & Surface Mount Technology*. 9(2): 65 – 69.

Lee, N. C. (1998). A Thorough Look at Lead-Free Solder Alternatives. *Circuits Assembly*. 64 – 71.

Lee, S. W. R. and Huang, X. (2002). Analysis on Solder Ball Shear Testing Conditions with Simple Computational Model. *Soldering & Surface Mount Technology*. 14(1): 45 – 48.

Lee, S. W. R. and Lau, J. H. (2000). Solder Joint Reliability of Plastic Ball Grid Array with Solder Bumped Flip Chip. *Soldering & Surface Mount Technology*. 12(2): 16 – 23.

Lee, S. W. R. and Zhang, X. (1998). Sensitivity Study on Material Properties for the Fatigue Life Prediction of Solder Joints under Cyclic Thermal Loading. *Circuit World*. 24(3): 26 – 31.

Lee, T., Lee, J. and Jung, I. (1998). Finite Element Analysis for Solder Ball Failures in Chip Scale Package. *Microelectronics Reliability*. 38: 1941 – 1947.

Lee, W. W., Nguyen, L. T. and Selvaduray, G. S. (2000). Solder Joint Fatigue Models: Review and Applicability to Chip Scale Packages. *Microelectronics Reliability*. 40(): 231 – 244.

LeGall, C. A. (1996). *Thermomechanical Stress Analysis of Flip Chip Packages*. Georgia Institute of Technology: M.Sc. Thesis.

Li, L. and Müller, W. H. (2001). Computer Modeling of the Coarsening Process in Tin-Lead Solders. *Computational Materials Science*. 21: 159 – 184.

Lin, J. C. and Chiang, K. N. (2000). Thermal/Mechanical Analysis of Novel C-TSOP Using Nonlinear FEM Method. *IEEE 2000 Int'l Symp on Electronic Materials & Packaging*. Nov 30 – Dec 2, 2000. Hong Kong: IEEE, 371 – 377.

Lin, K. L. and Hsu, H. M. (2001). Sn-Zn-Al Pb-Free Solder – An Inherent Barrier Solder for Cu Contact. *Journal of Electronic Materials*. 30(9): 1068 – 1072.

Linteau, M. W. (1997). *Impression Creep in Near Eutectic Tin-Lead and Tin-Silver Solders*. University of Texas at Arlington: M.Sc. Thesis.

Liu, X., Xu, S., Lu, G. Q. and Dillard, D. (2001). Stacked Solder Bumping Technology for Improved Solder Joint Reliability. *Microelectronics Reliability*. 41(12): 1979 – 1992.

Logsdon, W. A., Liaw P. K. and Burke M. A. (1990) Fracture Behavior of 63Sn-37Pb Solder. *Engng Fracture Mech*. 36(2): 183-218.

Lu, H., Bailey, C. and Cross, M. (2000). Reliability Analysis of Flip Chip Designs Via Computer Simulation. *Transactions of the ASME Journal of Electronic Packaging*. 122: 214 – 219.

Lucas, J. P., Guo, F., McDougali, J., Bieler, T. R., Subramanian, K. N. and Park, J. K. (1999). Creep Deformation Behavior in Eutectic Sn-Ag Solder Joints Using a Novel Mapping Technique. *Journal of Electronic Materials*. 28(11): 1270 – 1275.

Ma, S., Qian, Y. Y., Liu, F. and Yoshida, H. (2001a). High Reliable Solder Joints Using Sn-Pb-La Solder Alloy. *Proceedings of 8th International Symposium on the Physical and Failure Analysis of Integrated Circuits*. 9 – 13 July 2001. Singapore: IEEE, 63 – 66.

Ma, X, Qian, Y. and Yoshida, F. (2001b). Effect of La on the Sn-rich Halo Formation in Sn60-Pb40 Alloy. *Journal of Alloys and Compounds*. 327: 263 – 266.

Marjamäki, P., Kivilahti, J. and Kouhia, R. (2001). Comparison of Two Classes of Integration Algorithms in Creep Analysis. *European Conference on Computational Mechanics*. 26 – 29 June 2001. Cracow, Poland: Cracow University of Technology, 1 – 11.

Mavoori, H., Chin, J., Vaynman, S., Moran, B., Keer, L. and Fine, M. (1997). Creep, Stress Relaxation, and Plastic Deformation in Sn-Ag and Sn-Zn Eutectic Solders. *Journal of Electronic Materials*. 26(7): 783 – 790.

McCabe, R. J. and Fine, M. E. (2000). The Creep Properties of Precipitation-Strengthened Tin-Based Alloys. *JOM*. 33 – 35.

McCluskey, F. P., Kweon, Y. D., Lee, H. J., Kim, J. W. and Jeon, H. S. (2000). Method for Assessing Remaining Life in Electronic Assemblies. *Microelectronics Reliability*. 40: 293 – 306.

McDougall, J. L. (1998). *An Analysis of Global and Localized Creep Strains and Creep Properties of Non-Composite and Composite Lead-Free Solders at Room and Elevated Temperatures.* Michigan State University: M.Sc. Thesis.

Michaelides, S. (1999). *Physical-Based Process Modeling, Reliability Prediction, and Design Guidelines for Flip-Chip Devices.* Georgia Institute of Technology: Ph.D. Thesis.

Miller, A. (1987). The MATMOD Equations. In: Miller, A. ed. *Unified Constitutive Equations for Creep and Plasticity.* London: Elsevier Applied Science. 139 – 219.

Minzhong, Z. and Liu, H. W. (1986). Fatigue Crack Growth under General Yielding Cyclic Loading. *Eng. Mater. Technol.* 108: 201 – 205.

Miric, A. Z. and Grusd, A. (1998). Lead-Free Alloys. *Soldering & Surface Mount Technology.* 10(1): 19 – 25.

Mishiro, K., Ishikawa, S., Abe, M., Kumai, T., Higashiguchi, Y. and Tsubone, K. (2002). *Microelectronics Reliability.* 42(1): 77 – 82.

Mitlin, D., Raeder, C. H. and Messler, R. W. Jr. (1999). Solid Solution Creep Behavior of Sn-xBi Alloys. *Metallurgical and Materials Transactions A.* 30A: 115 – 122.

Miyake, K., Yoshida, T., Baik, H. G. and Park, S. W. (2001). Viscoelastic Warpage Analysis of Surface Mount Package. *Journal of Electronic Packaging.* 123(2): 101 – 104.

Moore, T. D. and Jarvis, J. L. (2001). Improved Reliability in Small Multichip Ball Grid Arrays. *Microelectronics Reliability.* 41(3): 461 – 469.

Moore, T. D. and Jarvis, J. L. (2002). The Effects of In-Plane Orthotropic Properties in a Multi-Chip Ball Grid Array Assembly. *Microelectronics Reliability.* 42(6): 943 – 949.

Murty, K. L., Haggag, F. M. and Mahidhara, R. K. (1997). Tensile, Creep, and ABI Tests on Sn5%Sb Solder for Mechanical Property Evaluation. *Journal of Electronic Materials*. 26(7): 839 – 846.

Myers, R. H. (1990). *Classical and Modern Regression with Applications*. 2nd Edition. Boston: PWS-KENT Publishing Company.

Neu, R. W., Scott, D. T. and Woodmansee, M. W. (2001). Thermomechanical Behavior of 96Sn-4Ag and Castin Alloy. *Transactions of the ASME Journal of Electronic Packaging*. 123: 238 – 246.

Nowottnick, M., Scheel, W., Wittke, K. and Pape, U. (2000). Method of Rapid Testing of Thermo-Mechanical Characteristics of Solder Joints. *Microelectronics Reliability*. 42(7): 1135 – 1146.

Okura, J. H., Shetty, S., Ramakrishnan, B., Dasgupta, A, Caers, J. F. J. M. and Reinikainen, T. (2000). Guidelines to Select Underfills for Flip Chip on Board Assemblies and Compliant Interposers for Chip Scale Package Assemblies. *Microelectronics Reliability*. 40: 1173 – 1180.

Ozmat, B. (1990). A Nonlinear Thermal Stress Analysis of Surface Mount Solder Joints. IEEE, 959 – 972.

Palmer, M. A., Redmond, P. E. and Messler, R. W. Jr. (2000). Thermomechanical Fatigue Testing and Analysis of Solder Alloys. *Transactions of the ASME Journal of Electronic Packaging*. 122: 48 – 54.

Pang, H. L. J., Kwok, Y. T. ad Seetoh, C. W. (1997). Temperature Cycling Fatigue Analysis of Fine Pitch Solder Joints. *ASME Advanced Electronic Packagings*. 19(2): 1495 – 1500.

Pang, J. H. L., Seetoh, C. W. and Wang, Z. P. (2000). CBGA Solder Joint Reliability Evaluation Based on Elastic-Plastic-Creep Analysis. *Transactions of the ASME Journal of Electronic Packaging*. 122: 255 – 261.

Pang, J. H. L., Tan, K. H., Shi, X. and Wang, Z. P. (2001). Thermal Cycling Aging Effects on Microstructural and Mechanical Properties of a Single PBGA Solder Joint Specimen. *IEEE Transactions on Components and Packaging Technologies.* 24(1): 10 – 15.

Pang, H. L. J., Wang, Y. P., Shi, X. Q. and Wang, Z. P. (1998). Sensitivity Study of Temperature and Strain Rate Dependent Properties on Solder Joint Fatigue Life. *Proceedings on the 1998 IEEE/CPMT Electronics Packaging Technology Conference.* 8 – 12 Dec 1998. Singapore: IEEE, 184 – 189.

Pao, Y. H., Govila, R., Badgley, S. and Jih, E. (1993). An Experimental and Finite Element Study of Thermal Fatigue Fracture of PbSn Solder Joints. *Journal of Electronic Packaging.* 115: 1 – 8.

Pao, Y. S. (1992). A Fracture Mechanics Approach to Thermal Fatigue Life Prediction of Soldered Joints. *IEEE Trans. Comp., Hybrids, Manufact. Technol.* 15: 559 – 570.

Park, T. S. and Lee, S. B. (2001). Mechanical Fatigue Tests of Solder Joint under Mixed-Mode Loading Cases. *2001 Int'l Symposium on Electronic Materials and Packaging.* 19 – 22 Nov 2001. Jeju Island, South Korea: IEEE, 438 – 443.

Pitarresi, J. M., Sethuraman, S., Nandagopal, B. and Primavera, A. (2000). Reliability Modeling of Chip Scale Packages. *2000 IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium.* IEEE, 60 – 69.

Plumbridge, W. J. (1996). Solders in Electronics. *Journal of Materials Science.* 31: 2501-2514.

Plumbridge, W. J., Gagg, C. R. and Peters, S. (2001). The Creep of Lead-Free Solders at Elevated Temperatures. *Journal of Electronic Materials.* 30(9): 1178 – 1183.

Poech, M. H. and Eisele, R. (2000). A Modeling Approach to Assess the Creep Behavior of Large-Area Solder Joints. *Microelectronics Reliability*. 40: 1653 – 1658.

Popelar, S. F. (1997). A Parametric Study of Flip Chip Reliability Based on Solder Fatigue Modeling. *1997 IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium*. 13 – 15 Oct, 1997. Austin: IEEE, 299 – 307.

Rajib, R., Raghuram, V. P. and Suresh, K. S. (2000). *Thermal Cycle Guidelines for Automotive, Computer, Portable and Implantable Medical Device Application.* New York: ASME.

Ren, W. (2000). *Thermo-mechanical Properties of Packaging Materials and Their Applications to Reliability Evaluation for Electronic Packages*. Wayne State University: Ph.D. Thesis.

Reynolds, H. L., Kang, S. H. and Morris, J. W. Jr. (1999). The Creep Behavior of In-Ag Eutectic Solder Joints. *Journal of Electronic Materials*. 28(1): 69 – 75.

Rhode, R. W. and Swearengen, J. C. (1980). Deformation Modeling Applied to Stress Relaxation of Four Solder Alloys. *Journal of Engineering Materials and Technology*. 102: 207 – 214.

Ross, R. G. (1991). A Systems Approach to Solder Joint Fatigue in Spacecraft Electronic Packaging. *Journal of Electronic Packaging*. 113: 121 – 128.

Sakane, M. and Yamamoto, H. (2000). A Strain Rate Ratio Approach for Assessing Creep-Fatigue Life of 63Sn-37Pb Solder Under Shear Loading. *Proceedings of the 2000 IEEE Inter Society Conference on Thermal Phenomena*. IEEE, 187 – 192.

Sasaki, K., Ohguchi, K. and Ishikawa, H. (2001). Viscoplastic Deformation of 40Pb/60Sn Solder Alloys – Experiments and Constitutive Modeling. *Journal of Electronic Packaging*. 123: 379 – 387.

Satoh, R., Arakawa, K., Harada, M., and Matsui, K. (1991). Thermal Fatigue Life of Pb-Sn Alloy Interconnections. *IEEE Transactions on the Components, Hybrids, Manufacturing Technology*, 14(1): 224 – 231.

Schmidt, C. G. (1989). A Phenomenological Constitutive Model for Type Sn62 Solder Wire. *Proceedings on the Electronic Components Conference.* 22 – 24 May 1989. Houston: IEEE, 253 – 258.

Shangguan, D. (1999). Analysis of Crack Growth in Solder Joints. *Soldering & Surface Mount Technology.* 11(3): 27 – 32.

Shi, X. Q., Pang, H. L. J., Zhou, W. and Wang, Z. P. (2000). Low Cycle Fatigue Analysis of Temperature and Frequency Effects in Eutectic Solder Alloy. *International Journal of Fatigue.* 22: 217 – 228.

Skipor, A. F., Harren, S. V. and Botsis, J. (1995). The Effect of Mechanical Constraint on the Flow and Fracture of 63/37 Sn/Pb Eutectic Alloy. *Engineering Fracture Mechanics.* 52(4): 647 – 669.

Solomon, H. D. (1989). Strain-Life Behavior in 60/40 Solder. *Journal of Electronic Packaging*, 111: 75 – 82.

Solomon, H. D. and Tolksdorf, E. D. (1995a). Energy Approach to the Fatigue of 60/40 Solder: Part I-Influence of Temperature and Cycle Frequency. *Journal of Electronic Packaging.* 117: 130 – 135.

Solomon, H. D. and Tolksdolf, E. D. (1996). Energy Approach to the Fatigue of 60/40 Solder: Part II – Influence of Hold Time and Asymmetric Loading. *ASME Transactions of the Journal of Electronic Packaging.* 118: 67 – 71.

Soper, A., Pozza, G., Ignat, M. and Parat, G. (1997). Mechanical Response of Solder Joints in Flip-Chip Type Structures. *Microelectronics Reliability.* 37(10-12): 1783 – 1786.

Stephens, J. J. and Frear, D. R. (1999). Time-Dependent Deformation Behavior of Near-Eutectic 60Sn-40Pb Solder. *Metallurgical and Materials Transactions A.* 30A: 1301 – 1313.

Stolkarts, V., Keer, L. M. and Fine, M. E. (2001). Constitutive and Cyclic Damage Model of 63Sn-37Pb Solder. *Trans. on the Journal of Electronic Packaging.* 123: 351 – 355.

Su, P. (2001). *A Study on the Reliability of Flip Chip Solder Joints.* Cornell University: PhD Thesis.

Su, P., Rzepka, S., Korhonen, M. and Li, C. Y. (1999). The Effects of Underfill on the Reliability of Flip Chip Solder Joints. *Journal of Electronic Materials.* 26(9): 1017 – 1022.

Subbarayan, G. (1996). A Procedure for Automated Shape and Life Prediction in Flip-Chip and BG Solder Joints. *Journal of Electronic Packaging.* 118: 127 – 133.

Suganuma, K. (2001). Advances in Lead-Free Electronics Soldering. *Current Opinion in Solid State and Material Science.* 5: 55 – 64.

Suhling, J. C., Johnson, R. W., White, J. D., Matthai, K. W., Knight, R. W., Romanczuk, C. S. and Burcham, S. W. (1994). Solder Joint Reliability of Surface Mount Chip Resistors/Capacitors on Insulated Metal Substrates. IEEE, 465 – 473.

Tee, T. Y., Sivakumar, K. and Do-Bento-Vieira, A. (2000). Board Level Solder Joint Reliability Modeling of LFBGA Package. *Proceedings on the 2000 Int'l Symp. on Electronic Materials & Packaging.* IEEE, 51 – 54.

Tien, J. K. and Attarwala, A. I. (1991). Complications in Life Prediction Estimates at Elevated Temperatures in Lead/Tin Solders During Accelerated Cycling.

Proceedings on the Electronic Components and Technology Conference. 11 – 16 May 1991. Atlanta: IEEE, 667 – 670.

Tonapi, S. S. (1998). *Assembly and Reliability of Lead-Free Flip Chips.* State University of New York at Binghamton: M.Sc. Thesis.

Tribula, D., Grivas, D., Frear, D. R., Morris, J. W. Jr. (1989). Observations on the Mechanisms of Fatigue in Eutectic Pb-Sn Solder Joints. *ASME Journal of Electronic Packaging.* 111: 83 – 89.

Tsukada, Y., Tsuchida, S. and Mashimoto, Y. (1992). Surface Laminar Circuit Packaging. *Proceedings of the IEEE Electronic Components and Technology Conference.* May 18 – 20, 1992. San Diego, DA: IEEE, 22 – 27.

Vaynman, S. and McKeown, S. A. (1993). Energy-Based Methodology for Fatigue Life Prediction of Solder Materials. *IEEE Transactions on the Components, Hybrids, Manufacturing Technology*, 16: 317 – 322.

Vianco, P. T., Artake, I. and Jones, A. M. (1994). Reliability Studies of Surface Mount Boards Manufactured with Lead-Free Solders. *Proceedings on Surface Mount Int. Conf. and Exposition.* 437 – 448.

Vianco, P. T., Burchett, S. N., Neilsen, M. K., Rejent, J. A. and Frear, D. R. (1999). Coarsening of the Sn-Pb Solder Microstructure in Constitutive Model-Based Predictions of Solder Joint Thermal Mechanical Fatigue. *Journal of Electronic Materials.* 28(11): 1290 – 1298.

Vianco, P. T. and Frear, D. R. (1993). Issues in the Replacement of Lead-Bearing Solders. *JOM.* 45(7): 14 – 18.

Villain, J., Brueller, O. S. and Qasim, T. (2002). Creep Behavior of Lead Free and Lead Containing Solder Materials at High Homologous Temperatures with Regard to Small Solder Volumes. *Sensors and Actuators A.* 99(1-2): 194 – 197.

Wade, N., Akuzawa, T., Yamada, S., Sugiyama, D., Kim, I. S. and Miyahara, K. (1999). Effect of Microalloying on the Creep Strength and Microstructure of an Eutectic Sn-Pb Solder Alloy. *Journal of Electronic Materials*. 28(11): 1286 – 1289.

Wade, N., Wu, K., Kunii, J. Yamada, S. and Miyahara, K. (2001). Effects of Cu, Ag and Sb on the Creep-Rupture Strength of Lead-Free Solder Alloys. *Journal of Electronic Materials*. 30(9): 1228 – 1231.

Wang, G. Z., Cheng, Z. N., Becker, K. and Wilde, J. (2001). Applying Anand Model to Represent the Viscoplastic Deformation Behavior of Solder Alloys. *Journal of Electronic Packaging*. 123: 247 – 253.

Wang, J. Qian, Z., Zou, D. and Liu, S. (1998). Creep Behavior of a Flip-Chip Package by Both FEM Modeling and Real Time Moiré Interferometry. *Proceedings on the 1998 Electronic Components and Technology Conference*. IEEE, 1438 – 1445.

Wang, J., Zou, D., Lu, M., Ren, W. and Liu, S. (1999). Evaluation of Interfaical Fracture Toughness of a Flip-Chip Package and a Bimaterial System by a Compined Experimental and Numerical Method. *Engineering Fracture Mechanics*. 64: 781 – 797.

Wei, Y., Chow, C. L., Fang, H. E. and Neilsen, M. K. (2001). Characteristics of Creep Damage for 60 Sn-40 Pb Solder Material. *Transactions of the ASME Journal of Electronic Packaging*. 123: 278 – 283.

Wen, S. (2001). *Thermomechanical Fatigue Life Prediction for Several Solders*. Northwestern University: Ph.D. Thesis.

Wen, S., Keer, L. M. and Mavoori, H. (2001). Constitutive and Damage Model for a Lead-Free Solder. *Journal of Electronic Materials*. 30(9): 1190 – 1196.

Wen, S., Keer, L. M., Vaynman, S. and Lawson, L. R. (2002). A Constitutive Model for a High Lead Solder. *IEEE Trainsactions on Components and Packaging Technologies.* 25(1): 23 – 31.

Wiese, S., Feustel, F., Rzepka, S. and Meusel, E. (1999). Creep and Crack Propagation in Flip Chip SnPb37 Solder Joints. *Proceedings of the IEEE Electronic Components and Technology Conference.* June 1 – 4, 1999. San Diego, DA: IEEE, 1015 – 1020.

Wiese, S., Jakschik, S., Feustel, F. and Meusel, E. (2001a). Fracture Behavior of Flip Chip Solder Joints. *Proceedings of 2001 Electronic Components and Technology Conference.* 5 May – 1 June 2001. Orlando, FL: IEEE, 1299 – 1306.

Wiese, S., Rzepka, S. and Meusel, E. (2002). Time-Independent Plastic Behavior of Solders and Its Effect on FEM Simulations for Electronic Packages. *8th International Symposium on Advanced Packaging Materials.* IEEE: 104 – 111.

Wiese, S., Schubert, A., Walter, H., Dudek, R., Feustel, F., Meusel, E. and Michel, B. (2001b). Constitutive Behaviour of Lead-free Solders vs. Lead-containing Solders – Experiments on Bulk Specimens and Flip-Chip Joints. *Proceedings of the Electronic Components and Technology Conference.* May 29 – June 1, 2001. Orlando, FL: IEEE, 890 – 902.

Wilde, J. (2001). Design-for-Reliability in the Packaging of Sensors and Microsystems. *Tagungsband zum Kongreß Sensor 2001.* 8 – 10 May 2001. Nürnberg: Hrsg. AMA Service GmbH, Wunstorf, 263 – 268.

Wilde, J., Becker, K., Thoben, M., Blum, W., Jupitz, T., Wang, G. and Cheng, Z. (2000). Rate Dependent Constitutive Relations Based on Anand Model for 92.5Pb5Sn2.5Ag Solder. *IEEE Transactions on Advanced Packaging.* 23(3): 408 – 414.

Wilde, J., Cheng, Z. N. and Wang, G. Z. (1999). Influences of Packaging Materials on the Solder Joint Reliability of Chip Scale Package Assemblies. *International Symposium on Advanced Packaging Materials*. IEEE, 144 – 149.

Winter, P. R. and Wallach, E. R. (1997). Microstructural Modeling and Electronic Interconnect Reliability. *Soldering and Surface Mount Technology*. 26: 61 – 64.

Wojciechowski, D., Chan, M. and Martone, F. (2001). Lead-Free Plastic Area Arry BGA and Polymer Stud Grid Arrays™ Package Reliability. *Microelectronics Reliability*. 41: 1829 – 1839.

Woodmansee, M. and Neu, R. W. (2002). The Influence of Prior Strain Rate on Stress Relaxation in Solder Alloys. *Materials Science & Engineering A*. 322 (1-2): 79 – 88.

Wu, C. M. L., Lai, J. K. L. and Wu, Y. (1998). Thermal-Mechanical Interface Crack Behavior of a Surface Mount Solder Joint. *Finite Elements in Analysis and Design*. 30(1-2): 19 – 30.

Wu, J. D., Ho, S. H., Huang, C. Y., Liao, C. C., Zheng, P. J. and Hung, S. C. (2002). Board Level Reliability of a Stacked CSP Subjected to Cyclic Bending. *Microelectronics Reliability*. 42(3): 407 – 416.

Xie, D. J. (2000). A New Experimental Method to Evaluate Creep Fatigue Life of Flip-Chip Solder Joints with Underfill. *Microelectronics Reliability*. 40: 1191 – 1198.

Xie, D. J. and Wang, Z. P. (1998). Process Capability Study and Thermal Fatigue Life Prediction of Ceramic BGA Solder Joints. *Finite Elements in Analysis and Design*. 30: 31 – 45.

Yang, H. (1998). *Mechanical and Thermomechanical Stability Issues of 96.5Sn-3.5Ag Solder Joints in Microelectronic Packages*. North Carolina State University: Ph.D. Thesis.

Ye, H., Lin, M. and Basaran, C. (2002). Failure Modes and FEM Analysis of Power Electronic Packaging. *Finite Elements in Analysis and Design*. 38(7): 601 – 612.

Yi, S., Luo, G. and Chian, K. S. (2002a). A Viscoplastic Constitutive Model for 63Sn37Pb Eutectic Solders. *Journal of Electronic Packaging*. 94: 91 – 96.

Yi, S., Luo, G., Chian, K. S. and Chen, W. T. (2002b). A Viscoplastic Constitutive Model for 63Sn37Pb Eutectic Solders. *IEEE 2000 Int'l Symp on Electronics Materials & Packaging*. Nov. 30 – Dec. 2, 2000. Hong Kong: IEEE, 183 – 190.

Yoon, S. W., Park, C. J., Hong, S. H., Moon, J. T., Park, I S. and Chun, H. S. (2000). Interfacial Reaction and Solder Joint Reliability of Pb-Free Solders in Lead Frame Chip Scale Packages (LF-CSP). *Journal of Electronic Materials*. 29(10): 1233 – 1240.

Yu, Q. and Shiratori, M. (1997). Fatigue-Strength Prediction of Microelectronics Solder Joints under Thermal Cyclic Loading. *IEEE Transactions on Components, Packaging, and Manufacturing Technology – Part A*. 20(3): 266 – 273.

Zahn, B. A. (2002). Impact of Ball Via Configurations on Solder Joint Reliability in Tape-Based, Chip-Scale Packages. *2002 Electronic Components and Technology Conference*. IEEE, 1475 – 1483.

Zhang, L., Chee, S. S., Maheshwari, A. and Funcell, A. (2000). Experimental and Finite Element Analysis of Cavity Down BGA Package Solder Joint Reliability. *Proceedings on the 2000 IEEE Electronics Packaging Technology Conference*. 5 – 7 Dec, 2000. Singapore: IEEE, 391 – 397.

Zhang, X., Lee, S. W. R. and Pao, Y. H. (2000b). A Damage Evolution Model for Thermal Fatigue Analysis of Solder Joints. *Transactions of the ASME Journal of Electronic Packaging*. 122: 200 – 206.

Zhao, J., Miyashita, Y. and Mutoh, Y. (2000). Fatigue Crack Growth Behavior of 95Pb-5Sn Solder under Various Stress Ratios and Frequencies. *International Journal of Fatigue*. 22(8): 665 – 673.

Zhao, J., Miyashita, Y. and Mutoh, Y. (2001a). Fatigue Crack Growth Behavior of 96.5Sn-3.5ag Lead-Free Solder. *International Journal of Fatigue*. 23(8): 723 – 731.

Zhao, J., Mutoh, Y., Miyashita, Y., Ogawa, T. and McEvily, A. J. (2001b). Fatigue Crack Growth Behavior in 63Sn-37Pb and 95Pb-5Sn Solder Materials. *Journal of Electronic Materials*. 30(4): 415 – 421.

Zhuang, W. D., Chang, P. C., Chou, F. Y. and Shiue, R. K. (2001). Effect of Solder Creep on the Reliability of Large Area Die Attachment. *Microelectronics Reliability*. 41(12): 2011 – 2021.