DEVICE MODELLING OF ARCHIMEDEAN SPIRAL GRAPHENE NANOSCROLL FIELD-EFFECT-TRANSISTOR

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To my family, near and far

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ABSTRACT

For the past decades, researchers indicate that persistent scaling of conventional silicon Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) reaching its physical limit at 10nm, resulted in its performance degradation as the search continues for a low-power and high speed, density and reliability devices. The frailty due to the Short Channel Effects (SCE) has limited the device scaling. In addition, the emergence of Carbon Nanotube (CNT) in the past two decades has been a remarkable breakthrough in solving for transistor SCE; but there has also been a problem in controlling its band gap energy. Graphene Nanoscroll (GNS) is one of the carbon-based materials that inherit most likely similar electrical properties as CNT. But GNS possesses an advantage to modulate its properties by varying its carbon layer overlapping region owing to the open edge spiral, resulting in band gap variations. This study is to investigate the GNS carrier statistic against its geometry variation and its performance as a MOSFET. The carrier statistic such as the energy band gap, density of states, carrier density and intrinsic velocity were modeled and the results show strong relation to the overlapping region of GNS. The energy band gap exhibits an inverse relation to the overlapping region and metallic properties was restored when the overlap has reached certain limit. The carrier density also increases with the overlapping region as a sign of gap narrowing. Moreover, the intrinsic velocity increases with overlap region and remains constant as it reaches graphene Fermi velocity, signifying ballistic transport near Fermi point. The charge distribution in GNSFET was characterized based on the Landauer Buttiker's formalism. The output current shows good agreement with the experimental results at constant conductance and GNS structural parameters. Furthermore, the GNSFET demonstrated comparable performance to the CNTFET within ballistic limit. The GNSFET was also benchmarked with the latest 22nm MOSFET technology, which indicates faster switching capability due to enhancement in Subthreshold Swing (SS) and Drain Induced Barrier Lowering (DIBL).

ABSTRAK

Sejak beberapa dekad yang lalu, para pengkaji menyatakan pengecilan skala bagi peranti Logam-Oksida-Semikonduktor Transistor Medan Elektrik (MOSFET) secara berterusan hingga kepada had keupayaan fizikal panjang pengalir 10nm akan menyebabkan kebolehupayaannya merosot akibat daripada Kesan Pengalir Pendek (SCE). Kelangsungan kajian bagi menghasilkan peranti dengan penggunaan kuasa yang rendah dan berkelajuan tinggi dilaksanakan. Kemunculan *Carbon Nanotube* (CNT) dua dekad lalu didapati berupaya bagi menangani permasalahan ini; akan tetapi, ia mempunyai kesukaran dalam mengawal lebar jalur tenaganya. *Graphene Nanoscroll* (GNS) merupakan salah satu bahan berasaskan karbon yang mempunyai ciri-ciri elektrik yang hampir sama seperti CNT dengan kebolehan untuk mengawal jurang tenaganya melalui lapisan karbon yang bertindih, disebabkan oleh hujungnya yang terbuka pada bahagian sebelah tepi. Tujuan kajian ini dijalankan adalah untuk menyelidik statistik-pembawa GNS terhadap perubahan geometrinya dan kebolehupayaan sebagai MOSFET. Model matematik diterbitkan bagi ciri-ciri statistik cas pembawa seperti jurang tenaga, kadar ketumpatan keadaan kuantum, ketumpatan cas pembawa dan halaju intrinsik cas pembawa yang dipengaruhi oleh kawasan lapisan karbon yang bertindih. Kajian mendapati jurang tenaga berkadar songsang dengan lapisan bertindih karbon dalam GNS dan bersifat konduktor apabila penambahan lapisan bertindih mencapai had tertentu. Selain itu, halaju intrinsik meningkat dengan lapisan bertindih dan menjadi tepu pada halaju Fermi *Graphene*, menandakan pengangkutan balistik berhampiran titik Fermi. Pengagihan cas dalam GNS dihitung berdasarkan *Landauer Buttiker's Formalism*. Arus keluaran yang dikira menunjukkan perbandingan yang baik dengan hasil eksperimen dan prestasinya mampu menyaingi CNTFET dalam had balistik. Silikon MOSFET 22nm digunakan sebagai penanda aras, di mana GNSFET mempunyai daya penukaran suis lebih pantas serta meningkatkan Kecerunan Bawah-Ambang (SS) dan bagi Halangan-Merendah Longkang-Teraruh (DIBL).

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LIST OF ABBREVIATION

ACNT	-	Armchair carbon nanotube
AGNS	-	Armchair graphene nanoscroll
ALD	-	Atomic Layer Deposition
BTBT	-	Band-to-Band-Tunnelling
CVD	-	Chemical Vapour Deposition
CNT	-	Carbon nanotube
CNS	-	Carbon nanoscroll
CNTFET	-	Carbon nanotube Field-Effect-Transistor
DOS	-	Density of States
DIBL	-	Drain Induced Barrier Lowering
EBL	-	Electron-beam Lithography
GNSFET	-	Graphene nanoscroll Field-Effect-Transistor
GNR	-	Graphene nanoribbon
GAA	-	Gate-All-Around
gcd	-	Greatest common divisor
IPA	-	Isopropyl Alcohol
IBM	-	International Bussiness Machine
ITRS	-	International Technology Roadmap for Semiconductor
IC	-	Integrated Circuit
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect-Transistor
MFP	-	Mean free path
MDS	-	Molecular Dynamic Simulation
MWNT	-	Multi-walled carbon nanotube
NNTB	-	Nearest Neighbour Tight Binding
NEGF	-	Non-equilibrium Green’s Function

PTM	-	Predictive Technology Model
SB	-	Schottky-Barrier
SOI	-	Silicon-on-Insulator
SiP	-	System-in-Package
SS	-	Sub-threshold Swing
SWNT	-	Single-walled carbon nanotube
TEM	-	Thermionic Emission Microscope
VDW	-	Van der Waals interaction
ZCNT	-	Zig-zag carbon nanotube
ZGNS	-	Zig-zag graphene nanoscroll
1D	-	One-dimensional
2D	-	Two-dimensional
3D	-	Three-dimensional

LIST OF SYMBOLS

I_{on}	-	On-current
E_C	-	Conduction band
E_V	-	Valence band
E_F	-	Fermi level
$\vec{a}_1, \vec{a}_2$	-	Carbon lattice basis vector
a_{cc}	-	Carbon-carbon bond distances
t	-	Carbon-carbon bonding energy
$\vec{C}$	-	Chirality vector
$\vec{T}$	-	Translational vector
θ	-	Rolling angle
L_{CNT}	-	CNT circumferential length
d	-	Diameter
N_{cc}	-	Number of hexagons in the nanotube unit cell
$\vec{k}$	-	Momentum k-space quantized vector
k_x, k_y	-	Defining parallel line
υ	-	Number of Sub-bands
N_{turn}	-	GNS number of turns
r_{in}	-	GNS inner radius
d_{int}	-	GNS interlayer distance
ρ	-	GNS radius
L_{GNS}	-	GNS spiral length
d_{in}	-	Inner diameter
σ	-	Overlapping region
G	-	Conductance

M	-	Numbers of contributing channel
T	-	Transmission probability
G_o	-	$G_o = 2e^2/h$, Quantum conductance
h	-	$h = 4.136 \times 10^{-15}\ eV \cdot s$ Planck's constant
e	-	$e = 1.602 \times 10^{-19}$ C, Electron charge
$f(E)$	-	Fermi's distribution function
K_B	-	$K_B = 8.6173 \times 10^{-5}\ eV \cdot K^{-1}$, Boltzmann's constant
$\hbar$	-	$\hbar = h/2\pi$, Modified Planck's constant
m^*	-	Effective mass
λ_D	-	De-Broglie wavelength
E_{co}	-	Potential energy
ε	-	Confining energy
E_{G_GNS}	-	GNS band gap energy
N	-	Carrier density
N_{GNS}	-	GNS Effective density of states
E_{Fi}	-	Intrinsic Fermi level
n_i	-	Intrinsic carrier density
C_e	-	Electrostatic capacitance
C_q	-	Quantum capacitance
C_G	-	Gate capacitance
ε_o	-	$\varepsilon_o = 8.854 \times 10^{-12}\ F \cdot m^{-1}$, Vacuum permittivity
ε_r	-	Dielectric constant
C_{sub}	-	Substrate capacitance
U_{scf}	-	Self-consistent potential
C_d	-	Drain capacitance
C_s	-	Source capacitance
α_G	-	Gate fitting parameter
α_d	-	Drain fitting parameter
$\Im_i(\eta_F)$	-	Fermi-Dirac Integral

υ_i	-	Intrinsic velocity
υ_F	-	$\upsilon_F = 0.96 \times 10^{-5}\ ms^{-1}$, Fermi velocity
G_{ON}	-	ON-conductance
$R_{contact}$	-	Contact resistance
$R_{channel}$	-	Channel resistance
R_{nc}	-	Non-transparent resistance
R_Q	-	Quantum resistance
R_{ON}	-	On-resistance
m_o	-	$m_o = 9.0194 \times 10^{-31}\ Kg$, electron mass
g_m	-	Transconductance
υ_{inj}	-	Injection velocity
I_{off}	-	Off-current

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CHAPTER 1

INTRODUCTION

1.1 Introduction

It is well-known that transistor has become the most essential portion in the growth of such advanced technology nowadays, owing to its extensive usage during the 80s. The Moore's Law has been the guideline in device scaling for decades, which indicates that the density of the transistor is doubly increased in one and a half years and the size of a transistor is doubly decreased within 3 years. The International Business Machine (IBM) corporation has set the standard in device scaling that has constant electric field by a scaling factor of $k \approx 0.7$ or the so called Dennard's scaling law for a conventional planar Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET), which has led to a high processing compact system (Dennard et al., 2007).

However, in 2001, the classical scaling law based on a constant-filed scaling has come to a limit where it failed to scale certain parameter such as the threshold voltage, power consumption and sub-threshold current due to increase of electric fields as device dimension shrunk and put the Moore's Postulate into halt (Kuhn, 2009). This scaling limit has been underlined by the International Technology Roadmap for Semiconductor (ITRS) as the horizon of the classical Dennard's Scaling Law of the planar MOSFET (Kuhn, 2009).

Throughout the years, scientist and researchers have enhanced transistor capability to substantiate the continuation of Moore’s Law and today they are able to adapt and downscale the transistor dimension beyond 130nm technology node that is known as the horizon of Dennard’s classical scaling. In other words, we have entered the age of “post-CMOS classical scaling law” (ITRS, 2011). In this perspective, we had witnessed the employment of nanoscale technology instead of microelectronic for a high processing device. Subsequently, within the next decade, the possibility of manufacturing technology of less than 10nm node can be succeeded. Due to fast advancing technology, the industry is demanding more efficient device with smaller dimension, low power consumption and reduced leakage current of an integrated circuit (IC). Therefore, device diversification has been applied to compensate the size of the circuitry and have multiple functions within a System-in-Package (SiP). Device miniaturization is also one of the methods, by increasing the density of the transistor within a single IC, which is commonly utilized to realize the Moore’s Law.

Table 1.1 is the guideline from ITRS in achieving device miniaturization for higher device performance in the near future. It is the key challenge in device scaling over the next 14 years listed by ITRS. ITRS has been very crucial in keeping the long-term reliability of a device. Based on this table, one of the concerns has been the reliability of novel devices, structures, and materials. Such material, for example carbon-based material (carbon nanotube, graphene, carbon nanoscroll) has been introduced for future applications. In order to understand the mechanism of these novel materials, experimental and theoretical efforts have been done to investigate their behaviour.

Table 1.1 : ITRS 2011 guideline for long-term device scaling.

Long-Term 2019-2026	***Summary of Issues***
Implementing of advanced multi-gate structures	• Fabrication of advanced non-planar multi-gate MOSFET to below 10nm gate length • Control of short-Channel effects • source/drain engineering to control parasitic resistance • Strain enhanced thermal velocity and quasi-ballistic transport
Identification and implementation of new memory structure	• Scaling storage capacitor for DRAM • DRAM and SRAM replacement solutions • Cost effective installation of high density 3-D NAND (512 Gb – 4 Tb) • Implementing non-charge-storage type of NVM cost effectively • Low-cost, high-density, low-power, fast-latency memory for large systems
Reliability of novel devices, structures, and materials	• Understand and control the failure mechanisms associated with new materials and structures for both transistor and interconnect • Shift to system level reliability perspective with unreliable devices
Power scaling	• V_{dd} scaling • Controlling sub-threshold current or/and sub-threshold slope • Margin issues for low V_{dd}
Integration for functional diversification	• Integration of multiple functions onto Si CMOS platform 3-D integration

Due to the limitation of conventional silicon MOSFET, a new material which is more reliable in replacing silicon as a semiconductor for sub-micron channel has emerged. The carbon nanotube (CNT) has been eminently spoken of within the past two decades. Even now, numerous researches on CNT application is still on-going, owing to its remarkable electronic and mechanical properties. CNT was first discovered in 1991 by Sumio Iijima at the NEC Fundamental Research Laboratory in Tsukuba, Japan, and by Donald Bethune at IBM’s Almaden Research Centre in California. Unfortunately, the fabrication process for a high-quality CNT with controllable diameter to dictate the energy band gap is very difficult (ITRS, 2011).

On the contrary, in 2003, a group of scientist has come out with a novel structure of graphene which is less expensive to produce (Braga et al., 2004). It is called a carbon nanoscroll (CNS) (Viculis et al., 2003). CNS is a multilayer long tubular structure much like CNT, however CNS has an open edge along the translational axis. It is also described as the Archimedean type-spiral graphene due to its novel spiral structure. By considering the quantum confinement effect, CNS that has its diameter shrunk to a one dimensional (1D) structure is known as a graphene nanoscroll (GNS). Thus, GNS can be suitable for nanoscale application such as nanotransistor, and bio-sensoring devices. There have been very few researches regarding GNS, especially in terms of their application. Furthermore, it is expected that GNS inherits similar fundamental properties as CNT and graphene such as ballistic transport properties due to its symmetrical band structure (Zhou et al., 2011) long mean-free-path (MFP), and high mobility (Zheng et al., 2011). On the other hand, the electronic transport of GNS is affected by the interlayer interaction between inner and outer layer compared to the single-walled CNT; thereby, it is expected that GNS will exhibit higher on-current, I_{on} than the single-walled CNT for the same diameter (Schaper et al., 2011).

In order to investigate the carrier statistic and the output performances of the GNS, device modelling plays an important role in assessing those features. Modelling provides an early approximation as to what the device performance would deliver so that it can fit with the industrial demand. Therefore, accurate model with necessary considerations is required to provide a close estimation with the real device output.

1.2 Problem Statement

Further downscaling of the conventional planar MOSFET is not possible when it comes to control the short channel effects. The high channel doping MOSFET in obtaining an acceptable range of threshold voltage has resulted in band-to-band tunnelling (BTBT) making it vulnerable to high current leakage, mobility degradation, and severe threshold voltage roll-off due to high drain-induced barrier lowering (DIBL), which is impractical for high performance application. Thus, the conventional device modelling is no longer accurate due to the quantum effects in a nanoscale device. In order to counter this problem, ITRS has introduced with the reliability of novel devices, structures and materials as previously shown in Table 1.1.

CNTFET is one of the reliable novel devices that is capable of replacing the conventional MOSFETs. Furthermore, the researches regarding CNT-based devices have been widely conducted theoretically and experimentally. It has been the focus for more than two decades, to bridge the knowledge gap between MOSFET technologies into nanoscale carbon-based devices. Many researches, particularly in CNTFET performance within the nanoscale regime are still on-going until today. Even so, the limitations of the CNT have restricted its capability to certain extent as highlighted by the ITRS 2011 in Emerging Research Materials report, which are:

1. The ability to control band gap energy.
2. Positioning of the nanotubes in required locations and directions.
3. Control of the number of nanotube walls.
4. Control of charge carrier type and concentration.
5. Deposition of a gate dielectric.
6. Formation of low resistance electrical contacts.

All of these constraints have been widely discussed in the previous researches (Franklin et al., 2012; Chen et al., 2008; Zhang et al., 2007; Javey et al., 2005), while GNS could offer another way in resolving some of these constraints as to rectify the device performance and production, owing to its similarity in carrier transport with CNT and less complex fabrication process compared to a high-quality single-walled CNT. By using GNS, the overlapping region between the inner and the outer layer can be tuned over a broad range of size and the number of walls can be controlled; instead of closed tubular structure of CNT that limits its permeability compared to the GNS. Therefore, GNS could provide a better control range of the energy gap compared to its CNT counterpart due to the tuneable core size, which can possibly be the key for constraint (1) and (3). The energy gap of the CNT is very much influenced by its diameter and the problem would be to obtain a particular diameter size for an acceptable range of energy gap. On the other hand, GNS offers a better way in controlling the energy gap by tuning the overlapping regions of the spiral structure.

The 1D GNS is expected to exhibit both CNT and graphene characteristics. Besides its tuneable structure, GNS also exhibits some features that are related to its precursor (CNT and graphene) such as the symmetrical band structure, high mobility and ballistic transport, which will be thoroughly discussed in Chapter 2. Therefore, it is expected that the GNS is capable to compete with CNTFET as future MOSFET and to investigate the GNS potential as a nanotransistor within ballistic limit would be worthwhile. Since GNS is a confined 1D structure, quantum mechanical effects such as the quantum capacitance need to be considered in the modelling part due to its significant effects when subject to bias voltage.

With regards to the limitation in MOSFET and CNT, and considering to the performance expectation on GNS, the research problems can be summarized as follows:

1. The constraint in nanoscale conventional silicon MOSFET and CNTFET.
2. The GNS geometry effects on its carrier statistic and electronic properties.
3. The 1D GNS Field–Effect-Transistor (GNSFET) device performances compared to the CNTFET and the conventional silicon MOSFET.

1.3 Research Objectives

The followings are the objectives of this project:

1. To analytically model and investigate the 1D Archimedean type-spiral GNS carrier statistics and electronic properties.

2. To assessed the performance between GNSFET and CNTFET devices for high speed application.
3. To benchmark the GNSFET with the 22nm conventional silicon MOSFET.

1.4 Research Scopes

The scopes of this research cover the modelling of the carrier statistics and the carrier transport for 1D GNS, including device performance analysis. A literature review was performed to understand the physical overview of the 1D GNS referring to its Archimedean spiral structure and the effect on its electronic properties. Subsequently, by understanding these features, the dispersion relation to that includes the concept of sub-band and the Archimedean spiral parameters is modelled. This will become the contributing factors to other carrier statistic parameters. As a sequence to these carrier statistics, ballistic carrier transport was modelled by using the Landauer Buttiker's expression. In this carrier transport model, the non-ideality effect such as the non-ohmic contact was included to obtain better comparison with experimental data and the phonon scattering effects were excluded since very little attention has been given on GNS scattering. The GNSFET was compared with the experimental data at high conductance and its performance against CNTFET at a quantum conductance limit is assessed. Benchmarking was also performed against the 22nm node technology MOSFET.

1.5 Research Contributions

CNTFET has been providing the scaling opportunity within the nanoscale regime for MOSFET application. However, the emergence of GNS that offers more flexibility in terms of energy band control and material production can contribute to much better device scaling and fabrication.

In this research, the developed analytical model is based on the 1D quantum confinement effect of the Fermi-Dirac distribution in computing the GNS carrier statistics. The Archimedean type-spiral parameter was included in these models to understand the geometry effects on its carrier statistic that associated with the mobile charge; in order to provide the insight on its mobile charge carrier transport and its performance through changing its spiral parameter. Comparison was made with the experimental or published data to validate the modelling work that will help to characterize and predict the charge behaviour in GNSFET.

Moreover, the preliminary analysis in this research could provide the understanding of its ballistic carrier transport between both CNTFET and GNSFET. In this context, the distinction between both structures that influence their device performance was determined and further enhancement for GNSFET is discussed based from previous researches in terms of the device structure. In addition, this research also discussed the performance between GNSFET with the recent 22nm MOSFET technology. The 22nm MOSFET technology has been made as the standard benchmark for GNSFET, to justify the relevance of using GNSFET as the nanotransistor. The performances and device enhancement for GNSFET are also included in this discussion. Although this research only emphasizes on device level analysis, it may still contribute by offering insight on the performance of GNSFET.

1.6 Thesis Outline

The introduction of this work is discussed in Chapter 1. It also includes the guideline of the research which consists of the problem statement, the research objective, the scope of the work, and the contributions of the research. Chapter 2 is a broad overview about GNS that discusses the band structure of the GNS as the initial step to understand the device properties through the application of the nearest neighbour tight binding (NNTB) graphene model. Also, some description of the GNS fabrication process and its electronic properties; and the modelling of the carrier transport are briefly discussed. The methodology of this work is summarized within Chapter 3, which explains the sequences of this work that also include the simulation step. All the analysis and discussion regarding the performance of the GNS are discussed in Chapter 4. Chapter 5 is the summarization of the research on the capability of GNS as a future semiconductor channel and future recommendation for research enhancement.

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