SYSTEMATIC TUNING PROCEDURE FOR ANALOG DESIGN REUSE METHODOLOGY

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To my dearest family, friends, colleagues and Muslim brothers and sisters

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ABSTRACT

Shrinking transistor is undeniably important especially to reduce fabrication cost and to increase power efficiency of electronic devices. However, as fabrication technology progresses into deep submicron process, analog circuit design complexity grows significantly together with the increase in design time due to complex behaviour of short-channel Metal-Oxide-Semiconductor (MOS) transistor. Current scaling rules are incapable of maintaining circuit performance as design technology moves to deep submicron process. This research carries out a study on the effects of fabrication process migration on analog design reuse approach and offers a complementary design solution. In order to prove the concept, two-stage Operational Transconductance Amplifiers (OTA) have been designed using Silterra 0.18 μm Complimentary-MOS (CMOS) fabrication process and were later migrated to Silterra 0.13 μm. Existing scaling rules were adopted in the study in order to maintain the original circuit performance in 0.18 μm process. The performance degradation problems due to the migration into a deep submicron process were observed. Then, a solid-state systematic transistor tuning procedure based on Direct Current (DC) output scaling rule was proposed and applied to rectify the performance degradation problem due to design migration. Result shows that it improves the accuracy of the analog design scaling and can be applied to both short-channel and long-channel designs. On a Miller amplifier test circuit, the proposed tuning stage results in an additional voltage gain up to 16 dB and twice faster settling time compared to a single-stage scaling alone, and approximately 33% less power consumption and 28% smaller silicon area when compared to the original design on 0.18 μm process. The research is expected to contribute to current development of analog design reuse methodology.

ABSTRAK

Pengecutan transistor adalah perkara mustahak yang tidak dapat dinafikan terutamanya untuk mengurangkan kos fabrikasi dan untuk meningkatkan kecekapan kuasa dalam peranti elektronik. Walau bagaimanapun, seiring dengan teknologi fabrikasi yang bergerak menuju kawasan submikron mendalam, kerumitan mereka cipta litar analog dan masa yang terlibat meningkat dengan drastik disebabkan kelakuan transistor Logam-Oksida-Separa pengalir (MOS) bersaluran-pendek yang kompleks. Peraturan penskalaan analog kini tidak berupaya untuk mengekalkan prestasi litar ketika menuju proses submikron mendalam. Penyelidikan ini mengkaji kesan penghijrahan proses fabrikasi ke atas pendekatan penggunaan semula litar analog, dan menawarkan satu penyelesaian yang melengkapi. Untuk membuktikan konsep tersebut, litar Amplifier Operasi Transkonduksi (OTA) dua-peringkat direka menggunakan proses fabrikasi Pelengkap-MOS (CMOS) Silterra 0.18 μm dan kemudian dihijrahkan kepada Silterra 0.13 μm. Peraturan penskalaan yang sedia ada digunapakai dalam kajian ini untuk mengekalkan prestasi litar asal pada proses 0.18 μm. Masalah kemerosotan prestasi disebabkan penghijrahan kepada proses submikron mendalam diperhatikan. Kemudian, satu kaedah baru prosedur talaan transistor yang sistematik berdasarkan peraturan penskalaan output Arus Terus (DC) telah diusulkan dan digunakan bagi menyelesaikan masalah kemerosotan prestasi tersebut. Keputusan menunjukkan ia mampu meningkatkan ketepatan penskalaan rekaan analog dan boleh digunakan untuk kedua-dua rekaan saluran-pendek dan saluran-panjang. Pada litar ujian sebuah amplifier Miller, satu peringkat talaan usulan meningkatkan gandaan voltan amplifier sehingga 16 dB dan mencapai dua kali kepantasan masa penyelesaian apabila dibandingkan dengan penskalaan satu peringkat sahaja, dan dengan anggaran 33% lebih rendah penggunaan kuasa dan 28% luas silikon yang lebih kecil apabila dibandingkan dengan rekaan asal pada proses 0.18 μm. Penyelidikan ini dijangka dapat menyumbang kepada pembangunan metodologi penggunaan-semula rekaan analog.

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LIST OF ABBREVIATIONS

AC	-	Alternating Current
ADC	-	Analog-to-Digital Converter
AMS	-	Analog Mixed Signal
BSIM	-	Berkeley Short-channel IGFET Model
CEDEC	-	Collaborative Microelectronic Design Excellence Centre
CMOS	-	Complementary Metal Oxide Semicodictor
COMDIAC	-	Compilateur de Dispositifs Actifs
DC	-	Direct Current
DIBL	-	Drain Induced Barrier Lowering
EDA	-	Electronic Design Aided
ESD	-	Electrostatic Discharge
FF	-	Fast-PMOS Fast-NMOS
GBW	-	Gain-Bandwidth
I/O	-	Input-Output
IC	-	Integrated Circuit
MOS	-	Metal-Oxide-Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NML	-	Non-Minimum Length
NMOS	-	N-type Metal Oxide Semiconductor
n-MOSFET	-	N-type MOSFET
OTA	-	Output Transconductance Amplifier
PMOS	-	P-type Metal Oxide Semiconductor
p-MOSFET	-	P-type MOSFET
SCE	-	Short-Channel Effect
SI	-	Strong Inversion
SoC	-	System-on-Chip
SPICE	-	Simulation Program for Integrated Circuits Emphasis
SS	-	Slow-PMOS Slow-NMOS

TT	-	Typical-PMOS Typical-NMOS
USM	-	Universiti Sains Malaysia
Vpp	-	Voltage peak-to-peak
W/L	-	Width-to-Length
WI	-	Weak Inversion

LIST OF SYMBOLS

W	–	Width of transistor
L	–	Length of transistor
I_D, I_{DS}	–	Transistor drain-to-source current
V_{DD}	–	Power supply voltage
V_{DS}	–	Transistor drain-to-source voltage
V_{GS}	–	Transistor gate-to-source voltage
V_{EG}	–	Effective gate voltage
V_{Th}	–	Transistor threshold voltage
g_m	–	Transconductance of transistor
P	–	Power consumption
t_{ox}	–	Transistor oxide thickness
g_{ds}	–	Transistor drain-to-source transconductance
A, A_V	–	Voltage gain
r_{ds}	–	Transistor drain-to-source resistance
f_T	–	Transition frequency
C_{gs}	–	Transistor gate-to-source capacitance
C_{ox}	–	Transistor oxide capacitance
C_C	–	Compensation capacitor
C_L	–	Load capacitor
V_E	–	Early voltage
μ	–	Electron mobility
K_L	–	Gate length scaling parameter
K_W	–	Width scaling parameter
K_{wN}	–	Width scaling parameter for n-MOSFET
K_{wP}	–	Width scaling parameter for p-MOSFET
K_V	–	Power supply scaling parameter
K_{ox}	–	Oxide capacitance scaling parameter

K_{oxN}	–	Oxide capacitance scaling parameter for n-MOSFET
K_{oxP}	–	Oxide capacitance scaling parameter for p-MOSFET
K_E	–	Early voltage scaling parameter
K_μ	–	Electron mobility scaling parameter
$K_{\mu N}$	–	Electron mobility scaling parameter for n-MOSFET
$K_{\mu P}$	–	Electron mobility scaling parameter for p-MOSFET
K_n	–	Slope scaling parameter
K_C	–	Load capacitance scaling parameter
K_I	–	Current scaling parameter
i_f	–	Forward inversion level
i_r	–	Reverse inversion level
ϵ_{ox}	–	Oxide relative permittivity
W_f	–	Finger width of transistor
n_f	–	Number of finger of transistor
λ	–	Channel modulation parameter
σ	–	Standard deviation

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CHAPTER 1

INTRODUCTION

This research work studies the issues and challenges of analog CMOS design reuse methodology. The main objective is to formulate an analog design reuse methodology which is compatible with short-channel CMOS design. This work proposes a second-stage tuning methodology for analog design reuse to increase the accuracy in maintaining the original analog circuit performance for short-channel device. Silterra CMOS 0.18 μm and 0.13 μm fabrication processes are used in the study. The study is divided into two parts. The first part is to study the impact of process scaling on analog and mixed-signal designs. The second part is to formulate an extension of existing analog design reuse methodology for short-channel analog design application, and to rectify gain degradation problem which is usually associated with short-channel transistor.

1.1 Scaling Rules and Design Reuse

Scaling rules are used to provide new transistor sizing while maintaining the original circuit performance during process migration. The performance of an analog circuit is highly dependent on process parameters. Therefore, it is important to study the relationship between process parameters and circuit performance to facilitate analog design reusability in various fabrication processes. The significant advantage of having systematic analog design reuse methodology is the shorter time needed for circuit rescaling compared to complete circuit redesign to meet the original specification.

Systematic analog design reuse methodology can assist designer in maintaining analog circuit performance in different processes. Digital circuits are easier to scale and usually can be done by automation, thus much less complex migration process

involved compared to analog circuits. As the analog design complexity keep growing, systematic reuse methodology for analog circuits can help to reduce the design time. Existing scaling rules for analog design reuse have to sacrifice some performance matrics in order to maintain the more important matrics [1, 2, 3, 4, 5]. Furthermore, the scaling rules were tested to MOS field effect transistors (MOSFETs) with the gate-length equal to few micrometers [2, 4]. Therefore, this research proposes a tuning procedure to increase the accuracy of the design scaling, and it is compatible with short-channel design.

Emerging short-channel effects and leakage current contribute to the latest analog design challenges in deep submicron process [6]. Moreover, power supply scaling is the biggest challenge [7]. These design issues also contribute to the problems of the analog circuit performance when migrating into deep submicron process such as:

- Reduction in transistor intrinsic gain due to velocity saturation [8, 6]
- Reduction in signal to noise ratio as a result of using low supply voltage and ultra thin gate oxide [6]
- Higher signal distortion for transistor operating in weak inversion [8]

Due to high design sensitivity in deep submicron process, designer is now relying even more on simulator program and accurate device modeling [8]. Hundreds of parameters are defined to describe short-channel transistor behaviour in various biasing points, making hand calculation even more complex, time consuming and less reliable. The growing design complexity reflects growing analog design time which affect the time-to-market.

1.2 Problem Statement

When one design migrates to a smaller process compared to its original size, it is expected that the performance of the design will be preserved if not better. However, previous works have proven that preserving all design specifications in a migrated design is not a straightforward process. Many reports [2, 3, 4, 5, 9, 10, 11] have highlighted that one may be able to preserve some of the specifications but not all. This issue is further aggravates when it involves migration to the deep submicron region.

Scaling rules can maintain gain-bandwidth and dynamic range of an operational amplifier during migration [1, 2]. However, the power consumption may doubled or the silicon area can be much larger compared to the original design [1, 2]. Another work with modified scaling rules and a follow-on automatic tuning stage result in significant power reduction but at a cost of few times bigger silicon area compared to the original design [3, 4].

Channel-scaling rules derived from the MOSFET level-1 current equation [5, 11] resulted in lower power consumption and smaller area while maintaining the gain, bandwidth and phase margin. However, in the smallest fabrication process tested (0.12 micron), the amplifier gain is degraded [5]. Besides, all earlier works [1, 2, 5, 11] were tested on considerable long-channel MOSFET. As technology progresses into the deep submicron technology, consideration of short-channel MOSFET in analog design migration must be taken into account.

The degradation of transistor intrinsic gain is one of the prominent design problems in short-channel analog design [8]. Amplifier gain which is widely considered as the most important performance in any analog amplifier is directly related to the intrinsic gain. This research aims to rectify the amplifier gain degradation problem in analog design migration which becomes more significance for migration into deep submicron process. Hence, the design reuse methodology is further enhanced by extending the compatibility of the scaling process with the short-channel analog design.

1.3 Objectives

Based on the problem statement, this research work aims to achieve the following objectives:

i. To propose a tuning procedure for analog design reuse which can be applied to both short-channel and long-channel MOSFETs. The tuning procedure can compliment existing scaling works which are more suitable for long-channel transistors.

ii. To preserve the operational amplifier performance (gain, bandwidth and phase margin) during process migration at reduced power consumption and silicon area.

1.4 Scope of Work

This research aims to upgrade existing scaling rules with the proposed tuning procedure. The proposed tuning procedure is compatible with both long-channel and short-channel analog designs and able to maintain circuit performance during the process migration. Operational transconductance amplifier (OTA) circuits are used as the test circuits. The circuits are designed and characterized by using Cadence electronic design automation (EDA) on Silterra 0.18 μm process. Using scaling rules proposed in [5], the designs are migrated to 0.13 μm Silterra process. The proposed tuning procedure is then applied to the migrated designs. The significant of the tuning procedure is presented by tables and graphs generated by Matlab software. Selected designs are sent for fabrication at Silterra Malaysia and the IC is characterized using on-wafer test by Collaborative Microelectronic Design Excellence Centre (CEDEC) of Universiti Sains Malaysia (USM). Next, the IC is packaged, a test circuit is constructed using off-chip components and characterized using Agilent test and measurement instruments.

1.5 Methodology

This research is divided into three phases as shown in Figure 1.1. The first phase is the background study of scaling rules and analog scaling challenges. Then, problem statement is constructed based on the study.

The second phase started with a case study to formulate the design reuse methodology. Based on preliminary results from a case study, this research decided to propose a tuning procedure to achieve the objectives. The idea of preserving the output swing during design migration is translated into equations which guide the entire tuning process. This phase involves the circuit design and design migration stages. During these stages, operational amplifier circuits are designed on 0.18 μm and then characterized. Then the same designs are migrated to 0.13 μm process and characterized. Performance degradation of the migrated design in the 0.13 μm especially on short-channel design leads to the construction of tuning methodology stage. In this stage, a DC output voltage scaling is proposed and related equations are derived to adjust the output voltage of the two-stage analog amplifier. The last stage is testing the methodology on another amplifier designs to evaluate the performance of the proposed tuning procedure. Corner analysis and Monte Carlo simulation are used

to measure the reliability of the designs.

In the second phase, similar OTA circuits used in previous literature [1, 2, 3, 4, 5, 11] are adopted as the test circuits. They are constructed using short-channel or long-channel MOSFETs to represent two cases along with Miller compensation circuit to realize high output gain. Five key performance indicators are considered to be maintained during the design migration: voltage gain, bandwidth, phase margin, power consumption, and silicon area. The proposed tuning procedure aims to maintain the key performance during the process migration from 0.18 μm to 0.13 μm processes at a minimal trade-off. In addition, amplifier circuits with multi-finger and split-length transistors are used to verify the methodology.

The third phase of the research is to fabricate the design and characterized the physical IC. The layout from the selected design is prepared for fabrication by Silterra Malaysia using 0.18 μm CMOS process. The physical design is then characterized using on-wafer test and breadboard test. The related problems and limitations are discussed and analyzed in Chapter 4.

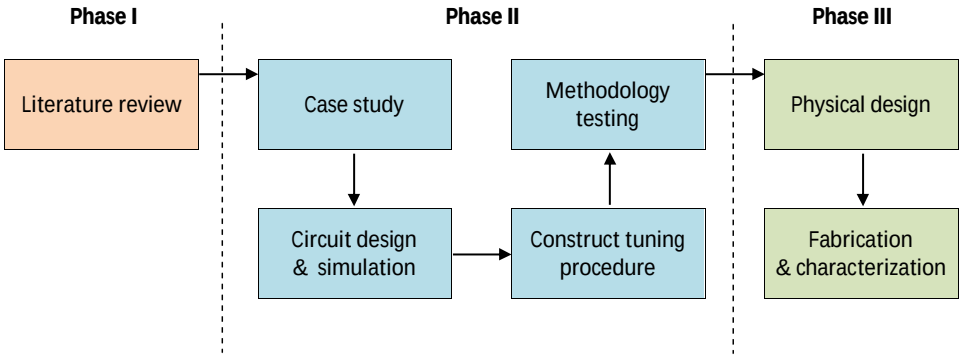

Figure 1.1: Flowchart of the research methodology.

1.6 Contributions

This research work contributes on an improved design reuse methodology that is suitable for both long- and short-channels transistors. Specifically, the contribution of the research are as follow:

i. The preservation of the output swing is taken into consideration which leads to the tuning procedure based on the scaled value of DC output voltage. This helps maintain the voltage gain and phase margin.

ii. Instead of tuning both width and length of the transistor, this thesis proposes the tuning of the width to adjust the DC output voltage. This is to ensure the transistor threshold voltage is maintained. Another advantage of scaling the width is to avoid short-channel effects (SCE) and drain-induced barrier lowering (DIBL) from being significantly modified.

1.7 Structure of Thesis

The thesis is organized into five chapters. The rest of the chapters are as follow.

Chapter 2 discusses the analog design migration challenges into deep submicron technology and existing scaling rules and its theories, advantages and limitations.

Chapter 3 presents the design scaling and the proposed tuning procedure based on DC output scaling. It is divided into four sections: the preliminary experiment, the design scaling, the proposed tuning procedure and the proposed tuning for multi-finger transistors.

Chapter 4 presents the performance analysis of the proposed tuning procedure for all circuit examples and the result of the physical design characterization.

Finally, conclusion and suggestions for future works are presented in Chapter 5.

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