NETWORK-ON-CHIP FAULT DETECTION AND ROUTER SELF-TEST

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NETWORK-ON-CHIP FAULT DETECTION AND ROUTER SELF-TEST

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A project report submitted in partial fulfilment of the
requirements for the award of the degree of
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Dedicated, in thankful appreciation for support and encouragement to my beloved wife Nabilah, my daughter Aleesya, my parents, families and friends.

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ABSTRACT

Network-on-Chip (NoC) router is an entity that facilitates communication between subsystem or IP cores on an integrated circuit. Faults such as permanent fault, transient fault and random fault are commonly observed on a NoC router. They may severely impact the functionality of an NoC router if not handled appropriately. This project proposes a mechanism to identify error and perform self-testing in NOC router by enhancing the Register Transfer Level (RTL) design of CONNECT NoC Baseline Router with error detection mechanism, as well as devising a built in self-test mode for NOC router. Both proposed error detection mechanism and built in self-test mode have been successfully implemented using System Verilog. The work presented in this project shows possible enhancement to NoC router architecture to detect erroneous packets. NoC router is able to detect faults through proposed error dection tecchniques. This allows router self-test in order to sustain the functionality of a system in the presence of faults. Simulation results show that additional logics do not affect NoC router performance.

ABSTRAK

Rangkaian-pada-Chip (NoC) router adalah entiti yang memudahkan komunikasi antara subsistem atau IP teras pada litar bersepadu. Kerosakan seperti kerosakan kekal, sementara dan rawak biasanya terjadinya pada router NoC. Kerosakan ini boleh memberi kesan teruk kepada fungsi sesuatu router NOC jika tidak ditangani dengan sewajarnya. Projek ini mencadangkan satu mekanisme untuk mengenal pasti kesilapan dan melakukan ujian diri dalam NoC router dengan meningkatkan Tahap Daftar Pemindahan (RTL) reka bentuk NoC Router dengan mekanisme pengesanan ralat, serta merangka terbina dalam mod ujian diri untuk NoC router. Kedua-dua mekanisme pengesanan ralat dicadangkan dan dibina dalam mod ujian diri telah berjaya dilaksanakan dengan menggunakan Sistem Verilog. Kerja-kerja yang dibentangkan dalam projek ini menunjukkan peningkatan mungkin untuk seni bina router NoC untuk mengesan paket salah. NoC router mampu mengesan kesalahan melalui dicadangkan tecchniques ralat dection. Ini membolehkan router sendiri ujian-bagi mengekalkan fungsi sistem yang di hadapan-dosa. Keputusan simulasi menunjukkan bahawa Logika tambahan tidak menjejaskan prestasi router NoC.

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LIST OF ABBREVIATIONS

ASM	-	Arithmetic State Machine
ASM	-	Automated Repeat Request
BIST	-	Built-In-Self-Test
CDD	-	Code Disjoint Detection
cpd	-	critical path delay
CONNECT	-	Configurable Network Creation Tool
CRC	-	Cyclic Redundancy Clock
NoC	-	Networks-on-Chip
PL	-	Packet Logging
RTL	-	Register Transfer Level
SOTA	-	state-of-the-art

CHAPTER 1

INTRODUCTION

1.1 Overview

Network-on-Chip (NoC) router is an entity that facilitates communication between subsystem or IP cores on an integrated circuit. Faults such as permanent fault, transient fault and random fault are commonly observed on a NoC router. NoC and interconnection networks have been subjects of research since early days of computing. Since the year 2005 [1], the field of NoC has begun due to the beginning of multi-core CPUs and the foreseeable tendency towards massively integrated many-core architectures. Networks-on-Chip (NoC) by far constitute the largest subsystem in many core architectures. Compared to bus subsystems, they offer reduced hardware overhead, better scalability, and higher data throughput. By adjusting design parameters, such as NoC network topology, IP allocation algorithm and flow control mechanism, NoCs can be flexibly adapted to application requirements.

Within the next 10 years, continued scaling will enable thousands of cores to be integrated with NoCs as the central backbone. As NoCs provide inherently redundant communication pathways, they are potentially robust against partial failure [2]. To exploit this property, adequate choices of fault models, error detection, diagnosis procedures, fault tolerance and reconfiguration have to be investigated on all layers of the network. Error detection and faults tolerance in NoC can be consider as a good field to study in order to optimize the performance and functionality of NoC network. Since current NoC does not have capailities of fault tolerance, NoC performance cannot achieved 100% accuracy.

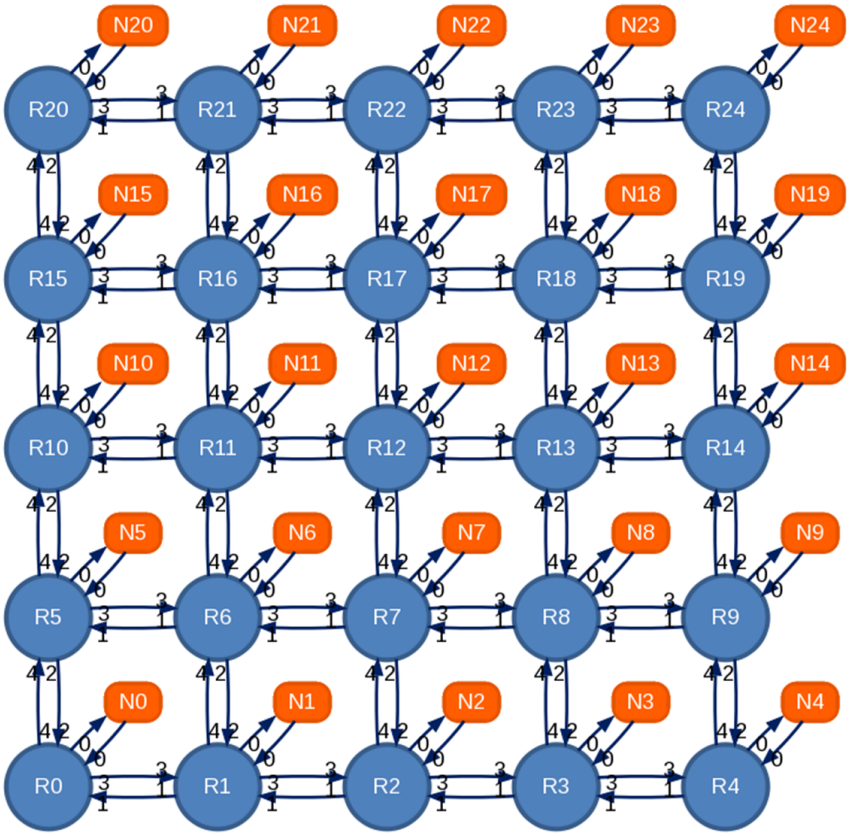

Figure 1.1: Example of NoC network with 5×5 mesh topology.

1.2 Faults on Network on Chip Router

Faults in NoC router can be classified as permanent fault, transient fault and random fault [3]. Permanent fault in router means that some of faults that cannot be recover or permanently there after continous packets had been injected on the same router. Based on researched, there are few factors that can be lead faults in NoC. Figure 1.2 shows the summary on faulty in Network On Chip Router.

1.3 Problem Statement

Baseline NoC design such as CONNECT cannot detect errorneous in NoC such as permanent fault, transient fault and random fault. In order to overcome this, error detection, fault tolerance and router reconfiguration have to be investigated on all layer of the network in order to come out a solution to handle faults and error in NOC router.

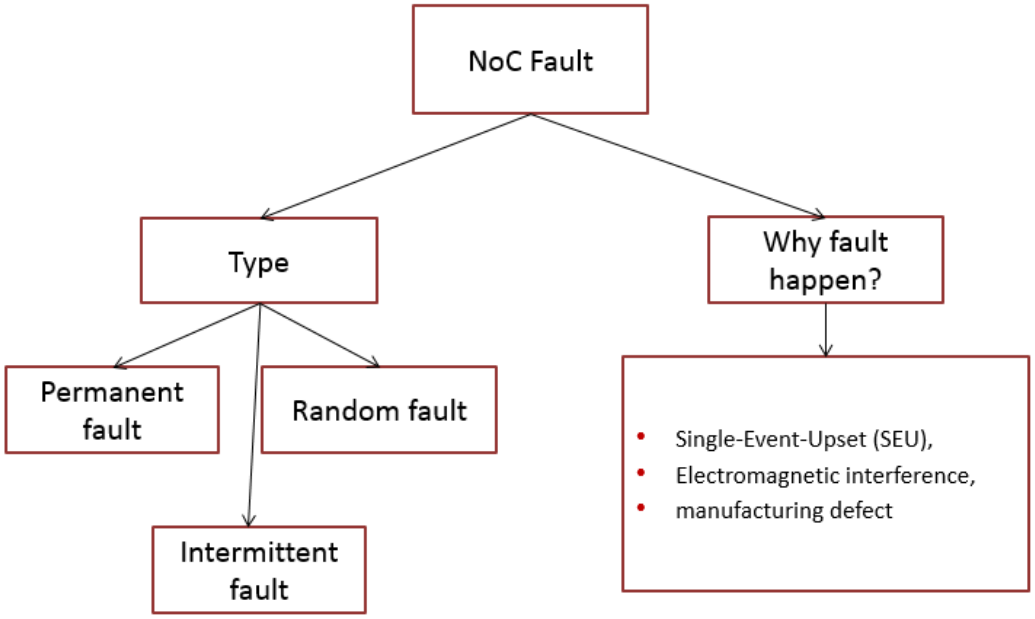

Figure 1.2: Types of NoC fault and factors.

By enhancing basic NoC design with error detection in order mitigate errors and faults. Actions can be taken to maintain NoC operation in order to keep the functionality of the router, enhancement on router self-test also need to be focus in this research.

Several works had been proposed for these two enhancements, but some techniques uses high logic resources and this lowers the performance of the NoC routers itself. Code Disjoint Detection (CDD) [4] by Grecu and Wrapper for router scan-chains attached to each router by Abady [5] were proposed in order to handle the fault tolerance in NoC router. These techniques require external circuits to perform error detection and router testing which can reduce the performance of NoC router itself.

By improving these ideas, a solution that can perform error detection mechanism by comparing Cyclic Redundancy Cycle (CRC) on input and output packet of each router and enabling router self-testing mode can be used to detect errorneous and faulty packets in NoC.

1.4 Objective and Scope

The goal of this research is to enhance basline CONNECT NoC router with enabling mechanism for online fault detection on NoC. Specifically the objectives of this project report are:

1. To enhance the RTL Design of CONNECT NoC Router with packet detection mechanism by comparing Cyclic Redundancy Cycle (CRC) on input and output packets of the First In First Out (FIFO) of every router memory to allow errorneous packets detection.
2. To propose a built in self-test mode mechanism on NoC router by implement pre-identify test vector that had been hardcoded in logic register in the router design hence to clarify the faulty router.

Network On Chip Router designed by using CONNECT router network RTL system as a baseline router architecture on 4×4 Mesh topology router network with x-y adaptive routing mechanism. First enhancement is enable packet logging mechanism into every NoC router by modifying CONNECT Router design. This is done by creating subs module in the RTL by adding error detection and error counter into the design. Next is to enable Router self-test mode with enabling pre-identify tests pattern into every single router in the system. This scope is more focus on adding extra state in network system which is called "*Router under test mode*". For this project, the system is totally designed in software and a test bench is use to validate both mechanism and mode on Network-on-Chip router design as discussed. Both RTL design and test bench are in Verilog and System Verilog using Altera Quartus II and Modelsim-Altera CAD tool as logic synthesizing tool and hardware simulation tool.

1.5 Report Organization

This project report consists of six chapters. The rest of this report are organized as follows.

Chapter 2 covers the literature review and discuss about the research of the fault tolerance and self-test for existing NoC router.

Chapter 3 covers the system overview of this project. It describes the various modules development and basic operation of each module. Two modules enhancement will be described briefly in this chapter.

The elaboration of the system development and methodology will be discussed in Chapter 4. All method and option used for this project will be described briefly in this chapter. The result system effectiveness is also discussed in this chapter.

Chapter 5 explains the testing and result of each module. The result system effectiveness is also discussed in this chapter.

Chapter 6 summarizes the project outcome. A few suggestions are proposed to enhance the design in the future.

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