

CNTFET-BASED TERNARY LOGIC DESIGN AND ARITHMETIC CIRCUIT  
SIMULATION USING HSPICE

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CNTFET-BASED DESIGN TERNARY LOGIC DESIGN AND ARITHMETIC  
CIRCUIT SIMULATION USING HSPICE

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*Specially dedicated to my beloved family, lecturers and friends  
For the guidance, encouragement and inspiration  
Throughout my journey of education*

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## ABSTRACT

This project report focuses on the multiple-value logic (MVL) or commonly known as ternary logic gates by using carbon nanotube (CNT) FETs devices (CNTFETs). It is shown ternary logic has promising future in CNTFETs when compare to conventional binary logic design, due to its simplicity and energy efficiency in digital design reduced circuit overhead such as chip area and interconnection. In this research, existing CNTFET-based binary inverter and standard ternary inverter with resistive-load (STI-R) for comparison with the other three types of inverter are proposed - Complementary Standard Ternary Inverter (CSTI); Standard Ternary Inverter with 1 resistor and 3 NCNTFET (NSTI-R); Standard Ternary Inverter with 1 resistor and 3 PCNTFET (PSTI-R) to analysis the performance, structure design and application. In addition, the research covers all the basic logic Ternary NAND gate and Ternary NOR gate for further benchmarking. All simulation results using SPICE are obtained and analyzed in the Direct Current (DC) setting and verified using half adder. Further study behavior of ternary logic includes the implementation of partial binary design into the ternary design and performance benchmarking. The result shows the CSTI have advantage on low power design with low leakage while NSTI-R has advantage on high-speed design inverter. In addition, partial binary design in the arithmetic circuit ternary design with CSTI shows added advantage in a low power design.

## ABSTRAK

Projek ini berfokus multi nilai logik atau dikenal pasti sebagai gate logik pertigaan dengan menggunakan “tiub nano karbon peranti kesan sirip transistor (CNTFETs)” logik pertigaan telah menunjukkan masa depan yang cerah dan menyakinkan dari segi kemudahan and penjimatan tenaga dari kajian apabila dibandingkan dengan logik binari dari segi penggunaan jumlah kawasan chip dan hubungan antara transistor. Pada kajian ini, CNTFET-based binari penyongsang dan ternari penyongsang jenis beban resistor akan dibanding dengan tiga jenis invertor yang dicadangkan - Pelengkap Standard pertigaan Penyongsang (CSTI); Standard pertigaan penyongsang dengan 1 perintang dan tiga NCNTFET (NSTI-R); Standard pertigaan penyongsang dengan 1 perintang dan tiga PCNTFET (PSTI-R) untuk mengkaji prestasi, stuktur bina dan penggunaan. Semua keputusan simulasi dikaji dengan menggunakan SPICE untuk menentu prestasi arus terus dengan pengesahan penggunaan litar aritmetik panambah separuh untuk mengenalpasti prestasi logik pertigaan. Kajian mengenalkan sebahagian reka binari digunakan ke atas rekaan logik pertigaan dengan memerhatikan prestasinya. Keseluruhannya, CSTI menunjukkan kelebihan dalam litar kuasa rendah dengan kebocoran tenaga rendah dan NSTI-R menunjukan pantasannya pada litar laju. Manakala, pengenalan reka binary ke dalam litar aritmetik ternari dengan menggunakan CSTI lagi menunjukkan kelebihan pada litar kuasa rendah.

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## LIST OF ABBREVIATIONS

CMOS	-	Complementary Metal–Oxide–Semiconductor
MOSFET	-	Metal–Oxide–Semiconductor Field-Effect Transistor
R	-	Resistor
L	-	Inductor
C	-	Capacitor
W	-	Width
L	-	Length
NMOS	-	N-channel Metal-Oxide-Semiconductor
PMOS	-	P-channel Metal-Oxide-Semiconductor
FET	-	Field Effect Transistor
CNTFET	-	Carbon Nano Tube Field Effect Transistor
NCNTFET	-	N-type Carbon Nano Tube Field Effect Transistor
PCNTFET	-	N-type Carbon Nano Tube Field Effect Transistor
$V_{th}$	-	Threshold Voltage
STI	-	Standard Ternary Inverter
PTI	-	Positive Ternary Inverter
NTI	-	Negative Ternary Inverter
STI-R	-	Standard Ternary Inverter With resistor load
NSTI-R	-	Standard Ternary Inverter with 1 resistor and 3 NCNTFET
PSTI-R	-	Standard Ternary Inverter with 1 resistor and 3 PCNTFET
CSTI	-	Complimentary Standard Ternary Inverter
TI	-	Ternary Inverter
T-NAND	-	Ternary NAND Gate Logic
T-NOR	-	Ternary NOR Gate Logic
CT-NAND	-	Complimentary Ternary NAND Gate Logic
NT-NAND-R	-	Ternary NAND Gate Logic with NSTI-R inserted
T-HA	-	Ternary Half Adder
SOC	-	System on Chip

SSD	-	Solid State Devices
SWNT	-	Single Wall Nano Tube
MWNT	-	Multi Wall Nano Tube
VLSI	-	Very Large Scale Integration
VTC	-	Voltage Transfer Curve
DC	-	Direct Current
SPICE	-	Simulation Program with Integrated Circuit Emphasis
PDP	-	Power Delay Product
EDP	-	Energy Delay Product

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# CHAPTER 1

## INTRODUCTION

### 1.1 History of Transistor

According to the popular Moore's Law, the number of transistors that can be placed on a single die doubled every two years [1]. Based on this assumption, it is predicted that in 2018, the end of complementary metal-oxide semiconductor (CMOS) era is imminent. Thus, new material and technique of fabrication or design system have been proposed and tested in many of the semiconductors manufacturing industries.

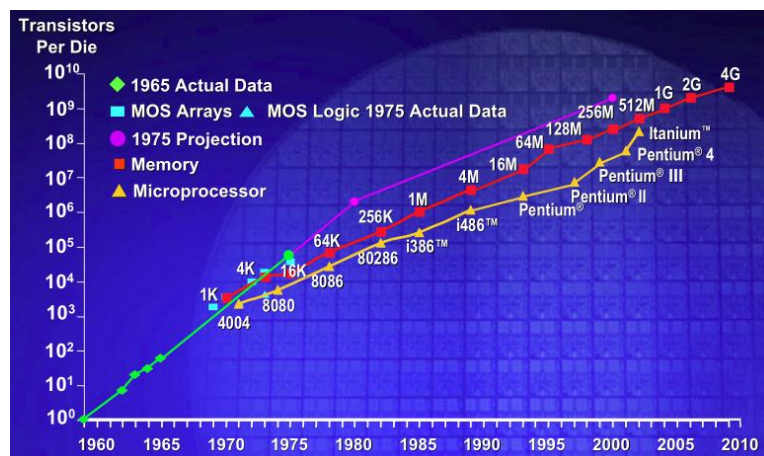


Figure 1.1 Moore's Law [2]



This is very promising when the number of transistors is increasing that allow more features in a system-on-chip (SOC) and more transistor in the same die size. Technology node and their respective physical gate length from 2007 to 2014 is tabulated in Table 1.1

**Table 1.1 :** Technology node versus gate length [3]

<b>Year</b>	<b>Technology node (nm)</b>	<b>Physical gate length (nm)</b>
<b>2007</b>	45	32/29
<b>2009</b>	32	27/24
<b>2011-2012</b>	22	22/20
<b>2013-2014</b>	16	18/16

When downscaling is done to increase the gate count and high switching rate, it introduces a high leakage current ratio due to the limitation of conventional CMOS. Thus, new materials such as carbon nanotube, silicon nanowire and graphene are introduced to overcome this problem. In this research, carbon nanotube FET (CNTFET) in digital circuit simulation is explored. In other words, this project is focused on the simulation of Carbon Nanotube Field-Effect Transistors (CNTFET) with the ternary design and benchmark with binary design. Ternary logic design later to be verified the performance and correctness using arithmetic circuit.

Since digital logic is introduced, digital computation is only performed on two-valued logic (0 or 1, TRUE or FALSE) in the Boolean space. Multiple-valued logic (MVL) replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic [4] or fuzzy logic [5]. Ternary logic (or three-valued logic) has attracted considerable interests due to its potential advantages over binary logic for designing digital systems. For example, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area. Furthermore, serial and serial-parallel arithmetic operations can be faster if the ternary logic is employed. Besides

resistive load design, ternary logic using CMOS can be found in the technical literature [6-7]. Chip area and power dissipation is reduced by more than 50 percent using an efficient MVL implementation for a signed 32-bits multiplier compared to its fastest binary counterpart [8]. MVL modules have been inserted into binary logic ICs to enhance the performance of CMOS technologies [9].

There are two kinds of MVL circuits based on MOS technology, namely the current-mode MVL circuits and the voltage mode MVL circuits. Voltage-mode MVL circuits have been achieved in multithreshold CMOS design [10]. The carbon nanotube (CNT) FET (CNTFET) is a promising alternative to the bulk silicon transistor for low-power and high-performance design due to its ballistic transport and low OFF-current properties [11-15]. A multithreshold CMOS design relies on body effects using different bias voltages to the base or the bulk terminal of the transistors. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Therefore, a multithreshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs. A resistive-load CNTFET-based ternary logic design has been proposed in Ref. [8]. However, in this configuration, large OFF-chip resistors (of at least 100M $\Omega$  values) are needed due to the current requirement of the CNTFETs. The design technique proposed in this paper base on Ref. [16] to eliminate the large resistors by employing active load with p-type CNTFETs in the ternary logic gates. In this paper, the multivalued logic design based on multithreshold CNTFETs is assessed and compared with existing multivalued logic designs based on CNTFETs.

In this research, designs of basic ternary gates/operators inverter is described in details namely ternary inverters (TI), ternary NAND (T-NAND), and ternary NOR (T-NOR). Beside resistive load inverter, another three type of inverter is used to benchmark performance. Ternary half adder (T-HA) is used for the reference to verify and analysis are presented as examples of the application of these ternary gates design technique.

For the arithmetic circuit design, a modified ternary logic circuit design technique is used to speed up and reduce power consumption of the circuits. The modified ternary logic design uses both ternary logic gates and binary logic gates based on the previous ternary logic design structures to take advantage of the two logic design styles' merits. The ternary logic gates are a good candidate for decoding block since it requires less number of gates while binary logic gates are a good candidate for fast computation. In this report, the modified ternary logic design method is proposed to achieve gate count reduction. Figure 1.2 is another solid proof that at CMOS design, Samsung already produce Solid State Device using 3-Bit V-NAND Technology and it proof the ternary can be very useful to handle the massive data. System on Chip (SOC) become main stream design, data handling become more heavy and most probably ternary design can be the replace binary design in some application .

## Samsung Unveils Solid State Drives Using Its New 3-Bit V-NAND Storage Technology

BY FARHAN · 2 DAYS AGO · 4 COMMENTS · 2.1K VIEWS



**Figure 1.2** Samsung unveil SSD using its new 3-bit V-NAND storage technology

[17]

## 1.2 Problem Statements

Silicon (Si) MOSFET has reached its limits as the technology is scaling down. Unlike Si MOSFET, CNTFET is favorable [8] due to its ballistic transport and low OFF current properties. This research addressed the following issues: How many type of Ternary inverter can be proposed for CNTFET-based design? What type of application can be applied on these few type of ternary inverter? What is the performance of ternary logic in CNTFET versus Binary logic in CNTFET? What is the maximum number of CNT can be placed in the channel to obtain the optimum performance of the device? How to model the 3 bits input for the ternary design using HSPICE?

## 1.3 Objectives

Since the Silicon based MOSFET is reaching the end of roadmap, this project is based on SPICE circuit-simulation of a type of multi-level logic gate design using Carbon Nanotube Field Effect Transistor (CNTFET). The objectives are:

1. To compare CNTFET-based binary inverter and standard ternary inverter with resistive-load (STI-R) with other three type of inverter is proposed - Complementary Standard Ternary Inverter (CSTI); Standard Ternary Inverter with 1 resistor and 3 NCNTFET (NSTI-R); Standard Ternary Inverter with 1 resistor and 3 PCNTFET (PSTI-R) to analysis the performance
2. To extend the ternary logic design to arithmetic ternary design and analyze the performance.
3. To study the combination of ternary design and binary design hence benchmark it performance.

## 1.4 Scope of Work

The main scope of this project is to study and simulate four types of inverter ternary design using CNTFET where the SPICE model is obtained from Stanford University. Four types ternary Inverter design is further analysis and benchmarks with Binary design to evaluate the performance. Arithmetic circuit used to verify the correctness from the ternary design. In addition, combination of ternary design and binary design in the ternary arithmetic is studied and simulated to improve the performance. HSPICE is used alongside Cosmoscope to perform digital circuit simulation. 3 bits input from the HSPICE model is introduced for ternary design and used for all ternary design simulation. Arithmetic circuit is used to simulate and study the energy efficiency and benchmarked with binary logic CNTFET design.

## 1.5 Significance of Study

This project has several important outcomes, which are

1. A new design of inverter is propose into the ternary design and identify the performance in several application.
2. Ternary design shown is state of art at the future to handle massive data processing and storage.
3. Tolerance of ternary input is identify with imperfect three levels (logic 0, 1 and 2) of square wave.

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