

ADAPTIVE LOOK-AHEAD ROUTING FOR LOW LATENCY
NETWORK-ON-CHIP

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"Specially dedicate to my Father's Spirit, and beloved Mama for her support and encouragement throughout my education."

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ABSTRACT

Network-on-chipsto employ simple oblivious routing algorithms, such as dimension order routing (DOR). While such oblivious routing algorithms are easy to implement in hardware, they often inefficient job of balancing the load across the links. Adaptive routing algorithms offer the ability to avoid congestion by supporting multiple paths between a source and destination. However, supporting adaptive routing for low latency routers is a challenge due to the computation of routing algorithm in one router in advanced (look-ahead routing). In this work we present an RTL architecture for adding adaptive look-ahead routing algorithm to a recently proposed low latency, virtual channel wormhole NoC router. In our proposed design each router pre-compute the preferred output port based on its local congestion and transfer the preferred output ports to the neighbor routers. These preferred output ports are used in the look-ahead routing. We compared our propose adaptive routing architecture with the reference design look-ahead routing XY routing algorithm under Transpose traffic and obtained 15 % improvement in average latency per hop. Our proposed routing algorithm has negligible influence in area overhead (12%) while has no influence on maximum operation frequency.

ABSTRAK

Rangkaian-atas-cip menggunakan algoritma laluan sedar, seperti laluan mengikut dimensi. Walaupun algoritma laluan sedar mudah untuk diaplikasi pada perkakasan, ianya tidak efisien dalam mengimbangi beban pada keseluruhan pautan. Algoritma laluan adaptif menawarkan keupayaan untuk mengelakkan kesesakan dengan menyokong pelbagai laluan antara sumber dan destinasi. Walau bagaimanapun, menyokong laluan adaptif bagi penghala kependaman rendah adalah satu cabaran kerana pengiraan algoritma laluan bagi satu-satu penghala termaju laluan pandang-kehadapan. Dalam projek ini kami membentangkan senibina RTL untuk menambah algoritma laluan adaptif pandang-kehadapan bagi penghala yang dicadangkan dengan kependaman rendah, saluran lubang cecacing maya di laluan NoC. Dalam rekabentuk yang dicadangkan, setiap penghala laluan prakira pilihan keluaran berdasarkan kesesakan tempatan dan memindahkan laluan pilihan pada laluan keluaran berbanding pada laluan jiran. Dalam rekabentuk yang dicadangkan, setiap penghala laluan prakira pilihan keluaran berdasarkan kesesakan tempatan dan memindahkan laluan pilihan pada laluan keluaran berbanding pada laluan jiran. Laluan keluaran pilihan digunakan dalam laluan pandang-kehadapan. Kami membandingkan senibina laluan adaptif yang dicadangkan dengan rujukan rekabentuk penghala pandang-kehadapan algoritma laluan XY di bawah trafik alihan dan memperolehi peningkatan 15% dalam kependaman purata setiap hop. Laluan algoritma yang dicadangkan mempengaruhi penggunaan sumber (12%) dan tidak mempengaruhi frekuensi operasi maksimum.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	x
	LIST OF FIGURES	xi
	LIST OF ABBREVIATIONS	xiii
1	INTRODUCTION	1
	1.1 Background Study	1
	1.2 Problem Statements	1
	1.3 Project Objectives	2
	1.4 Scope of work	2
	1.5 Report Organization	2
2	LITERATURE REVIEW	3
	2.1 Introduction	3
	2.2 Why Network on Chip ?	3
	2.3 Network Topologies	4
	2.3.1 A mesh-shaped	4
	2.4 Flow Control Techniques	5
	2.4.1 Store-and-Forward Routing	5
	2.4.2 Virtual Cut-Through Routing	5
	2.4.3 Wormhole routing	5
	2.4.4 Problems on Routing	6
	2.5 Routing on NoC	7
	2.5.1 Oblivious Routing Algorithms	7

	2.5.1.1	Dimension Order XY routing	7
	2.5.1.2	Pseudo Adaptive XY Routing	8
	2.5.1.3	Surrounding XY Routing	9
	2.5.1.4	Deterministic Routing Algorithms	10
	2.5.1.5	Shortest Path Routing	10
	2.5.1.6	Source Routing	10
	2.5.2	Partial Routing algorithms	11
	2.5.2.1	Turn Models	11
	2.5.2.2	West-first Routing	11
	2.5.2.3	North-last Routing	12
2.6		Adaptive Routing Algorithms	12
	2.6.1	Fully Adaptive Routing	12
2.7		Router Architectures	13
	2.7.1	Oblivious Routers	13
	2.7.1.1	Virtual Channel Router	13
	2.7.2	Adaptive Routers	15
	2.7.2.1	DyAD	15
	2.7.2.2	SPIN	15
	2.7.3	Related work	18
2.8		Chapter Summary	19
3		METHODOLOGY & IMPLEMENTATION	20
	3.1	Introduction	20
	3.2	Research Procedure	21
	3.3	Tools Used	22
	3.4	Reference routing model	27
	3.4.1	Conventional Router Architecture	28
	3.4.2	Look-ahead NoC router	30
	3.5	Proposed adaptive router	31
	3.5.1	Turn Models	31
	3.5.2	West-first	32
	3.6	Comparison between XY, look ahead XY, and adaptive look ahead routing algorithm	33
	3.7	Design a new adaptive look-ahead routing module based on network traffic.	36
	3.8	Chapter Summary	39

4	RESULT & DISCUSSION	40
4.1	Introduction	40
4.2	Router Verification	40
4.3	Performance Evaluation	41
4.4	Simulation Results	42
4.5	Result Analysis	44
4.6	Result Discussion	45
4.7	Chapter Summary	45
5	CONCLUSION AND FUTUREWORKS	46
5.1	Conclusion	46
5.2	Futureworks	47
	REFERENCES	48

LIST OF TABLES

TABLE NO.	TITLE	PAGE
2.1	Related work	18
2.2	Related work	19
3.1	The number and size of arbiters used in conventional allocators	29
3.2	Path selection 1	37
3.3	Path selection 2	37
4.1	Simulation results	44

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
2.1	Network on Chip	4
2.2	Routing on NoC	7
2.3	XY routing from router A to router B	8
2.4	Surrounding XY routing in SH-XY and SV-XY modes. There are 2 optional directions in SV-XY state	9
2.5	Allowed turns in west-first, north-last and negative first routing algorithms	12
2.6	A virtual channel router with 5 ports and 4 virtual channels	14
2.7	virtual channel router with simplified arbitration	14
2.8	DyAD router	16
2.9	RSPIN router used in SPIN systems	17
3.1	Structure flow	21
3.2	Tool Interface use in this project	22
3.3	Routers and IP cores in a 4x4 mesh network	24
3.4	Example of Deterministic Routing with congested path	25
3.5	Example of Adaptive Routing to solve congested	26
3.6	(a)Adaptive Routing with Deadlock case (b)Adaptive Routing support more than 1 turn to avoid Deadlock	27
3.7	The functional block diagram of the proposed NoC router	29
3.8	The functional block diagram of the proposed NoC router	30
3.9	A worm deadlock involving four routers and four packets in two-dimensional mesh	32
3.10	West-first	33
3.11	XY routing algorithm	33
3.12	Look ahead XY routing algorithm	34
3.13	Adaptive Look ahead routing algorithm	35
3.14	RTL Architecture	39
4.1	Average latency per hops under uniform traffic.	42
4.2	Performance of the algorithms under the uniform traffic.	43
4.3	Performance of the algorithms under the transpose traffic.	43

4.4	Average latency per hops under transpse traffic.	44
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LIST OF ABBREVIATIONS

AU	-	arbitration unit
BE	-	Best Effort
DyAD	-	Dynamically adaptive and deterministic
GT	-	Guaranteed Throughput
MPSoC	-	Multiprocessor system on chip
NoC	-	Extensible Markup Language
SoC	-	System-on-Chip
SPIN	-	Architecture is a scalable
VCR	-	Virtual channel router

CHAPTER 1

INTRODUCTION

1.1 Background Study

Due to the increasing complexity of system-on-chip (SoC) architectures, interconnections are becoming serious constraints in meeting performance and power consumption costs of the chip design. It indicated that up to 77% of the delay is due to the interconnect [1]. NoC is a chip communication networks address the challenges and risks of increasing interconnect complexity [2].

One of the important criteria for efficient NoC architecture is routing [3]. Earlier NoC designs used dimension order routing because because of its simplicity; however, deadlock is not avoidable. The traditional networks have complicated routing algorithms and protocols that provide traffic topologies and handle congestion. The advantage of traditional networks over the dimension order routing is that it limits the overhead when implementing such kind of design design [2].

1.2 Problem Statements

There is low performance in congested NoC, considering for example, deterministic routing, such as look-ahead XY routing [4]. Increasing its performance using adaptive routing is vital in NoC. Implementing adaptive look-ahead by using partial routing algorithms is a challenge since it requires the neighbouring routers traffic status. This results in a higher hardware cost, more complex design but high performance with low latency router design compared to look-ahead XY routing [4].

1.3 Project Objectives

In this study, we present a low-latency, two-stage router architecture suitable for NoC designs. The router architecture uses a strategy that is based on look-ahead information obtained from the nearby routers. The significant the proposed design is its low latency feature. This feature makes the look-ahead information more representative than many existing router architectures [4] with higher latencies. Precisely, the project proposes the following

1. To design RTL architecture for an adaptive look-ahead NoC routing module by optimizing the area of the existing low latency NoC [4].
2. To analyze the performance and the trade-off between our adaptive look-ahead routing and look-ahead X-Y routing algorithms.

1.4 Scope of work

This project focuses on adaptive routing to maintain low latency NoC interconnection. The basic design of this work is a two clock cycle latency router currently developed [4]. This work is carried out using Verilog hardware description language (HDL) on Quartus II compiler, and verified using Modelsim Altera version. Verification of the NoC topology is limited to a mesh topology using predefined NoC traffic. This project does not involve FPGA prototyping.

1.5 Report Organization

The rest of this report is organized as follows. Chapter 2 briefly explains existing works in literature on NoC routing. This includes some reviews of previous works and related topics. Chapter 3 presents the methodology and the Implementation carried out in realizing this project. Chapter 4 presents the results and discussion on project findings. Finally Chapter 5 concludes and recommends method of enhancement.

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