ADAPTIVE LOOK-AHEAD ROUTING FOR LOW LATENCY NETWORK–ON-CHIP

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A project report submitted in partial fulfilment of the
requirements for the award of the degree of
A Master of Engineering (Electrical - Electronics and Telecommunications)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JUNE 2014

"Specially dedicate to my Father’s Spirit, and beloved Mama for her support and encouragement throughout my education."

ACKNOWLEDGEMENT

In the name of Almighty Allah, the most Gracious, the most Merciful, for giving me the determination and will to complete my master project.

My deepest gratitude goes to my supervisor Dr. Muhammad Nadzir Marsono for his valuable and close supervision, guidance, comments, resources, encouragement, motivation, inspirations and friendship rendered throughout the study. I am also very grateful to my colleagues at FKE for their help, valuable advice, guidance and motivation. Without their continued support and interest, this report would not have been the same as presented here.

My heartiest and utmost gratitude goes to my dear father, mother, uncle and all my family for their patience, sacrifices, understanding, constant concern, moral support and prayers during the course of my study.

I am grateful for the help of my best friends. Among these are Abdullah Abdulhameed, Saddam Ali and Salem Mohammed

ABSTRACT

Network-on-chipsto employ simple oblivious routing algorithms, such as dimension order routing (DOR). While such oblivious routing algorithms are easy to implement in hardware, they often inefficient job of balancing the load across the links. Adaptive routing algorithms offer the ability to avoid congestion by supporting multiple paths between a source and destination. However, supporting adaptive routing for low latency routers is a challenge due to the computation of routing algorithm in one router in advanced (look-ahead routing). In this work we present an RTL architecture for adding adaptive look-ahead routing algorithm to a recently proposed low latency, virtual channel wormhole NoC router. In our proposed design each router pre-compute the preferred output port based on its local congestion and transfer the preferred output ports to the neighbor routers. These preferred output ports are used in the look-ahead routing. We compared our propose adaptive routing architecture with the reference design look-ahead routing XY routing algorithm under Transpose traffic and obtained 15 % improvement in average latency per hop. Our proposed routing algorithm has negligible influence in area overhead (12%) while has no influence on maximum operation frequency.

ABSTRAK

Rangkaian-atas-cip menggunapakai algoritma laluan sedar, seperti laluan mengikut dimensi. Walaupun algoritma laluan sedar mudah untuk diaplikasi pada perkakasan, ianya tidak efisyen dalam mengimbangi beban pada keseluruhan pautan. Algoritma laluan adaptif menawarkan keupayaan untuk mengelakkan kesesakan dengan menyokong pelbagai laluan antara sumber dan destinasi. Walau bagaimanapun, menyokong laluan adaptif bagi penghala kependaman rendah adalah satu cabaran kerana pengiraan algoritma laluan bagi satu-satu penghala termaju laluan pandang-kehadapan. Dalam projek ini kami membentangkan senibina RTL untuk menambah algoritma laluan adaptif pandang-kehadapan bagi penghala yang dicadangkan dengan kependaman rendah, saluran lubang cecacing maya di laluan NoC. Dalam rekabentuk yang dicadangkan, setiap penghala laluan prakira pilihan keluaran berdasarkan kesesakan tempatan dan memindahkan laluan pilihan pada laluan keluaran berbanding pada laluan jiran. Dalam rekabentuk yang dicadangkan, setiap penghala laluan prakira pilihan keluaran berdasarkan kesesakan tempatan dan memindahkan laluan pilihan pada laluan keluaran berbanding pada laluan jiran. Laluan keluaran pilihan digunakan dalam laluan pandang-kehadapan. Kami membandingkan senibina laluan adaptif yang dicadangkan dengan rujukan rekabentuk penghala pandang-kehadapan algoritma laluan XY di bawah trafik alihan dan memperolehi peningkatan 15% dalam kependaman purata setiap hop. Laluan algoritma yang dicadangkan mempengaruhi penggunaan sumber (12%) dan tidak mempengaruhi frekuensi operasi maksimum.

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LIST OF ABBREVIATIONS

AU	-	arbitration unit
BE	-	Best Effort
DyAD	-	Dynamically adaptive and deterministic
GT	-	Guaranteed Throughput
MPSoC	-	Multiprocessor system on chip
NoC	-	Extensible Markup Language
SoC	-	System-on-Chip
SPIN	-	Architecture is a scalable
VCR	-	Virtual channel router

CHAPTER 1

INTRODUCTION

1.1 Background Study

Due to the increasing complexity of system-on-chip (SoC) architectures, interconnections are becoming serious constraints in meeting performance and power consumption costs of the chip design. It indicated that up to 77% of the delay is due to the interconnect [1]. NoC is a chip communication networks address the challenges and risks of increasing interconnect complexity [2].

One of the important criteria for efficient NoC architecture is routing [3]. Earlier NoC designs used dimension order routing because because of its simplicity; however, deadlock is not avoidable. The traditional networks have complicated routing algorithms and protocols that provide traffic topologies and handle congestion.The advantage of traditional networks over the dimension order routing is that it limits the overhead when implementing such kind of design design [2].

1.2 Problem Statements

There is low performance in congested NoC, considering for example, deterministic routing, such as look-ahead XY routing [4]. Increasing its performance using adaptive routing is vital in NoC. Implementing adaptive look-ahead by using partial routing algorithms is a challenge since it requires the neighbouring routers traffic status. This results in a higher hardware cost, more complex design but high performance with low latency router design compared to look-ahead XY routing [4].

1.3 Project Objectives

In this study, we present a low-latency, two-stage router architecture suitable for NoC designs. The router architecture uses a strategy that is based on look-ahead information obtained from the nearby routers. The significant the proposed design is its low latency feature. This feature makes the look-ahead information more representative than many existing router architectures [4] with higher latencies. Precisely, the project proposes the following

1. To design RTL architecture for an adaptive look-ahead NoC routing module by optimizing the area of the existing low latency NoC [4].
2. To analyze the performance and the trade-off between our adaptive look-ahead routing and look-ahead X-Y routing algorithms.

1.4 Scope of work

This project focuses on adaptive routing to maintain low latency NoC interconnection. The basic design of this work is a two clock cycle latency router currently developed [4]. This work is carried out out using Verilog hardware description language (HDL) on Quartus II compiler, and verified using Modelsim Altera version. Verification of the NoC topology is limited to a mesh topology using predefined NoC traffic. This project does not involve FPGA prototyping.

1.5 Report Organization

The rest of this report is organized as follows. Chapter 2 briefly explains existing works in literature on NoC routing. This includes some reviews of previous works and related topics. Chapter 3 presents the methodology and the Implementation carried out in realizing this project. Chapter 4 presents the results and discussion on project findings. Finally Chapter 5 concludes and recommends method of enhancement.

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