

DESIGN OF ANALOG MODULES USING CARBON NANOTUBE FIELD
EFFECT TRANSISTOR (CNFET)

LEE LIH SHIUAN

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Universiti Teknologi Malaysia

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Specially dedicated to my beloved parents

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ABSTRACT

Carbon Nanotube Field Effect Transistor (CNFET) with its unique electrical properties has the potential of becoming a future alternative technology. Currently, research on CNFET circuit design is at the initial stage and it is challenging compared to conventional CMOS. In CMOS design, the I_d current equation is utilised to estimate the transistor size; whereas for CNFET, discussion on analog circuit design is limited. In addition, there are some CNFET parameters which are different from CMOS parameters need to be studied from design perspective. Therefore, a design technique has to be developed. In this project, challenges of CNFET design and differences with CMOS are identified. Various CNFET parameters are studied, which include diameter, channel length, pitch and number of tubes. Besides, the effects of CNFET parameters on circuit performance are explored and consequently the governing parameters are identified. In addition, the design approach is implemented in analog cells which include general purpose op amp. A considerable amount of HSPICE simulation using Stanford CNFET model has been performed to verify the proposed method. It is hope that the design approach developed in this project can be used as a guideline for circuit designer.

ABSTRAK

Tiub nano karbon kesan medan transistor (CNFET) yang mempunyai keunikan elektrik berpotensi menjadi teknologi alternatif masa depan. Kebelakangan ini, penyelidikan mengenai rekabentuk litar CNFET berada di peringkat awal dan ia lebih mencabangkan berbanding dengan CMOS konvensional. Dalam rekabentuk litar CMOS, Id formula digunakan untuk menganggarkan saiz transistor; manakala bagi CNFET, pengajian berkaitan dengan kaedah rekabentuk litar analog adalah terhad. Di samping itu, terdapat beberapa parameter CNFET yang berbeza daripada parameter CMOS perlu diterokai dari rekabentuk litar perspektif. Oleh itu, teknik rekabentuk litar analog CNFET perlu dibina. Dalam projek ini, cabaran CNFET dan perbezaan dengan CMOS dari rekabentuk litar perspektif dianalisis. Pelbagai parameter CNFET diterokai, termasuk diameter, panjang saluran, jarak tiub dan bilangan tiub. Di samping itu, kesan parameter CNFET pada prestasi litar dieksplorasi dan parameter utama diidentifikasi. Selain itu, kaedah reka bentuk litar diimplementasi dalam litar analog termasuk kegunaan umum op amp. Sebilangan simulasi HSPICE dengan menggunakan Stanford CNFET model dilaksanakan untuk mengesahkan kaedah tersebut. Adalah diharapkan bahawa pembangunan projek ini dalam kaedah rekabentuk litar analog CNFET boleh digunakan sebagai panduan kepada pereka litar.

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LIST OF ABBREVIATIONS

CMOS	- Complementary Metal Oxide Semiconductor
CMRR	- Common Mode Rejection Ratio
CNFET	- Carbon Nanotube Field Effect Transistor
CNT	- Carbon NanoTube
GBP	- Gain Bandwidth Product
HSPICE	- H-Simulation Program with Integrated Circuit Emphasis
IC	- Integrated Circuit
ITRS	- International Technology Roadmap for Semiconductors
MOSFET	- Metal Oxide Semiconductor Field Effect Transistor
OPAMP	- Operational Amplifier
PSRR	- Power Supply Rejection Ratio
SR	- Slew Rate
SWNT	- Single-Walled carbon NanoTube

LIST OF SYMBOLS

A_v	- Voltage gain
C_{gc}	- Gate-to-channel capacitance
C_{gtg}	- Gate-to-gate capacitance
C_{of}	- Outer fringe capacitance
D_{cnt}	- Diameter of carbon nanotube
f_{-3dB}	- Cut-off frequency
g_{ds}	- Output conductance
g_m	- Transconductance
g_m/g_{ds}	- Intrinsic gain
g_m/i_d	- Transconductance efficiency
I_D	- Drain current
L_{ch}	- Channel length
N_{cnt}	- Number of carbon nanotube
r_{out}	- Output resistance
S	- Pitch
V_{DS}	- Drain-source voltage
V_{GS}	- Gate-source voltage
V_T	- Threshold voltage
W_g	- Gate width

CHAPTER 1

INTRODUCTION

1.1 Background

As CMOS technology approaches the end of scaling, new structures and materials are discovered for alternative solution to Silicon. Carbon Nanotube Field Effect Transistor (CNFET) becomes one of the potential candidates for future IC technology. There has been a rapid progress on CNFET research since the discovery of carbon nanotube (CNT) due to its unique structure and electrical properties.

According to ITRS [1], CNFET technology is yet to mature for there are amount of process challenges which includes control of CNT purity, position/direction of CNT, CNT doping/carrier concentration, gate dielectric interface and contact formation. However, CNFET has better overall performance than CMOS because of its high drive current due to its high mobility of electrons movement near ballistic transport which leads to promising results. Considering the prospect of CNFET technology, there is a need to evaluate its performance on circuit level, yet researches on CNFET circuit design in digital and analog applications are few and limited [2,3,4,5].

Owing to the lack of literature on analog CNFET design, this project investigates the design issues of analog circuit using CNFET technology. CNFET parameters which are different from CMOS parameters need to be studied from design perspective. Therefore, a design technique has to be developed.

1.2 Problem Statement

CNFET is one of the potential choices in the future IC technology, yet references on CNFET circuit design are limited. The CNFET-based circuit design is different from conventional CMOS, whereby the design starts with transistor size estimation from I_D current equation, $I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$ for first-cut design using Level 1 model. On the other hand, in CNFET, there are a few parameters which include diameter, channel length, pitch and number of tubes. Having more parameters seems to have more options for circuit designer, yet blindly tune without understanding may cause difficulties in the design process. Therefore, it is necessary to study the CNFET parameters from design perspective. This project explores the CNFET parameters and its effects on circuit performance, consequently identifies the governing parameters. In addition, design approach is developed with the hope that it can be used as a guideline for others.

1.3 Objectives

The objectives of this project are:

- i. To study CNFET parameters from design perspective;
- ii. To apply knowledge gained from part i above in design approach of analog cells which include general purpose op amp.

1.4 Scope of Work

The scope of work encompasses the following areas:

- i. Study CNFET structure and Stanford CNFET model;
- ii. Identify major differences between CNFET and CMOS from design perspective;
- iii. Explore CNFET parameters and perform simulation in HSPICE;
- iv. Demonstrate design procedure in general purpose op amp.

1.5 Outline of Report

This report starts from Chapter 1 that gives the background on the project which identifies the area of research, the objective and the scope of work. Chapter 2 presents the literature review. It reviews papers which are relevant to CNFET circuit design. Chapter 3 is the research methodology. It outlines the process of designing CNFET-based analog circuit. Chapter 4 presents the results of basic analog blocks which are resistive load inverting amplifier, current source load inverting amplifier, push-pull inverting amplifier and cascode amplifier. Chapter 5 presents the results of design work on differential amplifier and general purpose op amp. The outcome of the project is discussed in this chapter. Finally, Chapter 6 is the conclusion of the project.

REFERENCES

- [1] International Technology Roadmap for Semiconductors 2013 Edition - Emerging Research Material, <http://www.itrs.net/Links/2013ITRS/2013Chapters/2013ERM.pdf>
- [2] Wei Wang, Zhiyuan Yu and Ken Choi, High SNM 6T CNFET SRAM Cell Design Considering Nanotube Diameter and Transistor Ratio, *IEEE International Conference on Electro/Information Technology (EIT)*, 15-17 May 2011, pp.1-4.
- [3] Hoque M.N.F., Ahmad H., Reza A.K., Mominuzzaman S.M. and Harun-Ur-Rashid A.B.M., Design Optimization of High Frequency Op Amp Using 32nm CNFET, *6th International Conference on Electrical and Computer Engineering (ICECE)*, 18-20 Dec 2010, pp.230-234.
- [4] Kim, Young Bok, Yong-Bin Kim and Fabrizio Lombardi, A Novel Design Methodology to Optimize the Speed and Power of the CNTFET Circuits, *2009 MWSCAS'09 52nd IEEE International Midwest Symposium on Circuits and Systems*, 2009, pp. 1130-1133.
- [5] Tanísia Possani and Alessandro Girardi, Design Methodology of Analog Integrated Circuits Using Carbon Nanotube Transistors, *Federal University of Pampa – UNIPAMPA, Alegrete - RS – Brazil*, 2011.
- [6] Jie Deng and H.S.Philip Wong, A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region, *IEEE Transactions on Electron Devices*, December 2007, 54(12), pp. 3186-3194.
- [7] Jie Deng and H.S.Philip Wong, A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full

Device Model and Circuit Performance Benchmarking, *IEEE Transactions on Electron Devices*, December 2007, 54(12), pp. 3195-3204.

[8] A Quick User Guide on Stanford University Carbon Nanotube Field Transistors (CNFET) HSPICE Model v.2.2.1

[9] Hoque M.N.F., Ahmad H., Reza A.K., Mominuzzaman S.M. and Harun-Ur-Rashid A.B.M., Design Optimization of High Frequency Op Amp Using 32nm CNFET, *6th International Conference on Electrical and Computer Engineering (ICECE)*, 18-20 Dec.2010, pp.230-234.

[10] Rahman F., Zaidi A.M., Anam N. and Akter A., Performance Evaluation of a 32-nm CNT-OPAMP: Design, Characteristic Optimization and Comparison with CMOS Technology, *Proceedings of 14th International Conference on Computer and Information Technology*, 22-24 Dec.2011, pp.583-588.

[11] Rahman F., Zaidi A.M., Anam N. and Akter A., Faiz R., A Study on the Performance Evaluation of a CNT-OPAMP by Variation of SWNTs in the CNFET-Channel Region, *IEEE Regional Symposium on Micro and Nanoelectronics (RSM)*, 28-30 Sep. 2011, pp.278-281.

[12] Fatema, Niger, Ikram Ilyas, Refaya Taskin Shama, and Fahim Rahman. Performance Evaluation of 8-Transistor and 9-Transistor, 32-nm CNT-OPAMPs in Designing and Comparing Non-Inverting Amplifiers, *Proceedings of the Global Engineering, Science and Technology Conference*, 28-29 Dec.2012.

[13] Polimetla M. and Mahapatra R., Analysis of Current Mirror in 32nm MOSFET and CNFET Technologies, *World Academy of Science, Engineering and Technology*, 2011, pp.806-809.

[14] Usmani F.A., Alam N. and Hasan M., Performance Comparison of Class AB Operational Amplifiers at 32nm in Technologies Beyond CMOS, *Proceedings of the 3rd National Conference INDIACom Computing for Nation Development*, 26-27 Feb.2009.

- [15] Usmani F.A. and Hasan M., Design and Parametric Analysis of 32nm OPAMP in CMOS and CNFET Technologies for Optimum Performance, *Proceedings of the Argentine School of Micro-Nanoelectronics, Technology and Applications (EAMTA)*, 1-2 Oct.2009, pp.87-92.
- [16] Sankar, P.A.G. and Kumar, K.U., Design and Analysis of Two Stage Operational Amplifier Based on Emerging sub-32nm Technology, *2013 International Conference on Advanced Nanomaterials and Emerging Engineering Technologies (ICANMEET)*, 24-26 July 2013, pp.587-591.
- [17] Tanísia Possani and Alessandro Girardi, Design Methodology Of Analog Integrated Circuits Using Carbon Nanotube Transistors, *Federal University of Pampa - UNIPAMPA, Alegrete RS Brazil*, 2011.
- [18] W. Makni, M. Najari, H. Samet, and M. Masmoudi, Operational Amplifier Circuit Design Using Carbon Nanotube Transistors, *Nanoscience & Nanotechnology-Asia*, 2013, 3(1), pp.106-113.
- [19] Raychowdhury, Arijit, Saibal Mukhopadhyay, and Kaushik Roy, A circuit-compatible model of ballistic carbon nanotube field-effect transistors, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2004, 23(10), pp.1411-1420.
- [20] Usmani F.A. and Hasan M., Novel hybrid CMOS and CNFET Inverting Amplifier Design for Area, Power and Performance Optimization, *IEDST'09 2nd International Workshop on Electron Devices and Semiconductor Technology*, IEEE, 2009, pp. 1-5.
- [21] Loan, Sajad A., M. Nizamuddin, Faisal Bashir, Humyra Shabir, Asim M. Murshid, Abdul Rahman Alamoud, and Shuja A. Abbasi, Design of a Novel High Gain Carbon Nanotube based Operational Transconductance Amplifier, *Proceedings of the International MultiConference of Engineers and Computer Scientists*, vol. 2. 2014.

[22] Jie Deng, and H. S. Wong, Modeling and Analysis of Planar-Gate Electrostatic Capacitance of 1-D FET with Multiple Cylindrical Conducting Channels, *IEEE Transactions on Electron Devices*, 2007, 54(9), pp.2377-2385.

[23] Jie Deng, *Device Modeling and Circuit Performance Evaluation for Nanoscale Devices: Silicon Technology beyond 45 nm Node and Carbon Nanotube Field Effect Transistors*, Ph.D. Dissertation, Stanford University, 2007.

[24] Akinwande D., Liang J., Chong S., Nishi Y. and Wong, H.S.P, Analytical Ballistic Theory of Carbon Nanotube Transistors: Experimental Validation, Device Physics, Parameter Extraction, and Performance Projection, *Journal of Applied Physics*, 2008, 104 (12), pp.124514-1-4.

[25] Tanísia Possani and Alessandro Girardi, Analysis of Electrical Characteristics of Carbon Nanotube Associations of Transistors and Comparison with CMOS Technology, *Federal University of Pampa - UNIPAMPA*, Alegrete RS Brazil, 2010.

[26] Hayat, Khizar, Hammad M. Cheema, and Atif Shamim, Potential of Carbon Nanotube Field Effect Transistors for Analogue Circuits, *The Journal of Engineering*, 2013, 1(1).

[27] Pregaldiny, Fabien, J. Kammerer, and Christophe Lallement, Compact Modeling and Applications of CNTFETs for Analog and Digital Circuit Design, *ICECS'06 13th IEEE International Conference on Electronics, Circuits and Systems*, IEEE, 2006, pp. 1030-1033.

[28] Ajit, Janardhanan S., Yong-Bin Kim, and Minsu Choi, Performance Assessment of Analog Circuits with Carbon Nanotube FET (CNFET), *Proceedings of the 20th Symposium on Great Lakes Symposium on VLSI*, ACM, 2010, pp.163-166.

[29] Jespers Paul, *The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches*. Vol.29, Springer, 2009.