DESIGN OF ANALOG MODULES USING CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNFET)

LEE LIH SHIUAN

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical - Computer & Microelectronics System)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JUNE 2014

Specially dedicated to my beloved parents

ACKNOWLEDGEMENT

Sincere appreciation to Prof. Dr. Abu Khari for his invaluable dedication of precious time and effort in supervising this project. Also, thanks to Stanford University for the CNFET model.

ABSTRACT

Carbon Nanotube Field Effect Transistor (CNFET) with its unique electrical properties has the potential of becoming a future alternative technology. Currently, research on CNFET circuit design is at the initial stage and it is challenging compared to conventional CMOS. In CMOS design, the Id current equation is utilised to estimate the transistor size; whereas for CNFET, discussion on analog circuit design is limited. In addition, there are some CNFET parameters which are different from CMOS parameters need to be studied from design perspective. Therefore, a design technique has to be developed. In this project, challenges of CNFET design and differences with CMOS are identified. Various CNFET parameters are studied, which include diameter, channel length, pitch and number of tubes. Besides, the effects of CNFET parameters on circuit performance are explored and consequently the governing parameters are identified. In addition, the design approach is implemented in analog cells which include general purpose op amp. A considerable amount of HSPICE simulation using Stanford CNFET model has been performed to verify the proposed method. It is hope that the design approach developed in this project can be used as a guideline for circuit designer.

ABSTRAK

Tiub nano karbon kesan medan transistor (CNFET) yang mempunyai keunikan elektrik berpotensi menjadi teknologi alternatif masa depan. Kebelakangan ini, penyelidikan mengenai rekabentuk litar CNFET berada di peringkat awal dan ia lebih mencabarkan berbanding dengan CMOS konvensional. Dalam rekabentuk litar CMOS, Id formula digunakan untuk menganggarkan saiz transistor; manakala bagi CNFET, pengajian berkaitan dengan kaedah rekabentuk litar analog adalah terhad. Di samping itu, terdapat beberapa parameter CNFET yang berbeza daripada parameter CMOS perlu diterokai dari rekabentuk litar perspektif. Oleh itu, teknik rekabentuk litar analog CNFET perlu dibina. Dalam projek ini , cabaran CNFET dan perbezaan dengan CMOS dari rekabentuk litar perspektif dianalisis. Pelbagai parameter CNFET diterokai, termasuk diameter, panjang saluran, jarak tiub dan bilangan tiub. Di samping itu, kesan parameter CNFET pada prestasi litar dieksplorasi dan parameter utama diidentifikasi. Selain itu, kaedah reka bentuk litar diimplementasi dalam litar analog termasuk kegunaan umum op amp. Sebilangan simulasi HSPICE dengan menggunakan Stanford CNFET model dilaksanakan untuk mengesahkan kaedah tersebut. Adalah diharapkan bahawa pembangunan projek ini dalam kaedah rekabentuk litar analog CNFET boleh digunakan sebagai panduan kepada pereka litar.

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LIST OF ABBREVIATIONS

CMOS	- Complementary Metal Oxide Semiconductor
CMRR	- Common Mode Rejection Ratio
CNFET	- Carbon Nanotube Field Effect Transistor
CNT	- Carbon NanoTube
GBP	- Gain Bandwidth Product
HSPICE	- H-Simulation Program with Integrated Circuit Emphasis
IC	- Integrated Circuit
ITRS	- International Technology Roadmap for Semiconductors
MOSFET	- Metal Oxide Semiconductor Field Effect Transistor
OPAMP	- Operational Amplifier
PSRR	- Power Supply Rejection Ratio
SR	- Slew Rate
SWNT	- Single-Walled carbon NanoTube

LIST OF SYMBOLS

Av - Voltage gain

Cgc - Gate-to-channel capacitance

Cgtg - Gate-to-gate capacitance

Cof - Outer fringe capacitance

Dcnt - Diameter of carbon nanotube

f_{-3dB} - Cut-off frequency

gds - Output conductance

gm - Transconductance

gm/gds - Intrinsic gain

gm/id - Transconductance efficiency

I_D - Drain current

Lch - Channel length

Ncnt - Number of carbon nanotube

rout - Output resistance

S - Pitch

V_{DS} - Drain-source voltage

V_{GS} - Gate-source voltage

V_T - Threshold voltage

Wg - Gate width

CHAPTER 1

INTRODUCTION

1.1 Background

As CMOS technology approaches the end of scaling, new structures and materials are discovered for alternative solution to Silicon. Carbon Nanotube Field Effect Transistor (CNFET) becomes one of the potential candidates for future IC technology. There has been a rapid progress on CNFET research since the discovery of carbon nanotube (CNT) due to its unique structure and electrical properties.

According to ITRS [1], CNFET technology is yet to mature for there are amount of process challenges which includes control of CNT purity, position/direction of CNT, CNT doping/carrier concentration, gate dielectric interface and contact formation. However, CNFET has better overall performance than CMOS because of its high drive current due to its high mobility of electrons movement near ballistic transport which leads to promising results. Considering the prospect of CNFET technology, there is a need to evaluate its performance on circuit level, yet researches on CNFET circuit design in digital and analog applications are few and limited [2,3,4,5].

Owing to the lack of literature on analog CNFET design, this project investigates the design issues of analog circuit using CNFET technology. CNFET parameters which are different from CMOS parameters need to be studied from design perspective. Therefore, a design technique has to be developed.

1.2 Problem Statement

CNFET is one of the potential choices in the future IC technology, yet references on CNFET circuit design are limited. The CNFET-based circuit design is different from conventional CMOS, whereby the design starts with transistor size estimation from Id current equation, $I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_T)^2(1+\lambda V_{DS})$ for first-cut design using Level 1 model. On the other hand, in CNFET, there are a few parameters which include diameter, channel length, pitch and number of tubes. Having more parameters seems to have more options for circuit designer, yet blindly tune without understanding may cause difficulties in the design process. Therefore, it is necessary to study the CNFET parameters from design perspective. This project explores the CNFET parameters and its effects on circuit performance, consequently identifies the governing parameters. In addition, design approach is developed with the hope that it can be used as a guideline for others.

1.3 Objectives

The objectives of this project are:

i. To study CNFET parameters from design perspective;
ii. To apply knowledge gained from part i above in design approach of analog cells which include general purpose op amp.

1.4 Scope of Work

The scope of work encompasses the following areas:

i. Study CNFET structure and Stanford CNFET model;
ii. Identify major differences between CNFET and CMOS from design perspective;
iii. Explore CNFET parameters and perform simulation in HSPICE;
iv. Demonstrate design procedure in general purpose op amp.

1.5 Outline of Report

This report starts from Chapter 1 that gives the background on the project which identifies the area of research, the objective and the scope of work. Chapter 2 presents the literature review. It reviews papers which are relevant to CNFET circuit design. Chapter 3 is the research methodology. It outlines the process of designing CNFET-based analog circuit. Chapter 4 presents the results of basic analog blocks which are resistive load inverting amplifier, current source load inverting amplifier, push-pull inverting amplifier and cascode amplifier. Chapter 5 presents the results of design work on differential amplifier and general purpose op amp. The outcome of the project is discussed in this chapter. Finally, Chapter 6 is the conclusion of the project.

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